

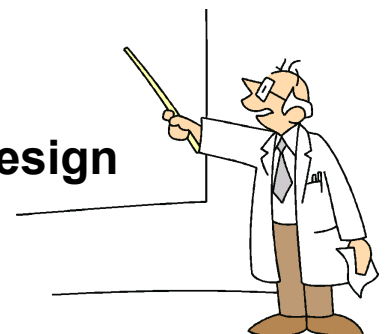
APS-IP Introduction for Altera



Ideal for embedded storage !

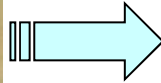
Agenda

- **PCIe SSD Overview**
 - SSD Trends
 - Merit of PCIe SSD for embedded system
- **APS-IP Introduction**
 - Summary
 - Function
 - User Interface
 - Performance and Size
 - Development Environment/Reference Design
- **Application**



SSD Trends

- **SATA interface is now performance bottle neck**
 - SSD Read/Write speed is limited to 600MB/sec SATA bandwidth
- **Move to PCI Express for faster speed**
 - PCIe GEN3 x4lane can provide 4GB/sec transfer speed
- **M.2 form factor suitable for compact product application**
 - Width=22mm, Lenth=20/42/80/120mm, DIMM-like very small outline



Current 2.5" SATA SSD

Latest M.2 type PCIe SSD

Merit of PCIe SSD for Embedded System 1

- **High Bandwidth: 1.5GB/s for Read, 1GB/s for Write**
- **Cost effective: Cost difference from SATA SSD is small**

Kingston Digital HyperX Predator 480 GB PCIe Gen2 x4 M.2 Solid State Drive 3.5-Inch SHPM2280P2/480G from Kingston

★ ★ ★ ★ ★ 46 customer reviews

List Price: \$764.00
Price: **\$439.99 & FREE Shipping**. Details
You Save: \$324.01 (42%)

Only 7 left in stock (more on the way).
Ships from and sold by Amazon.com. Gift-wrap available.

Want it Thursday, Oct. 15? Order within 1 hr 22 mins and choose Two-Day Shipping at checkout. Details

Size: 480GB M.2

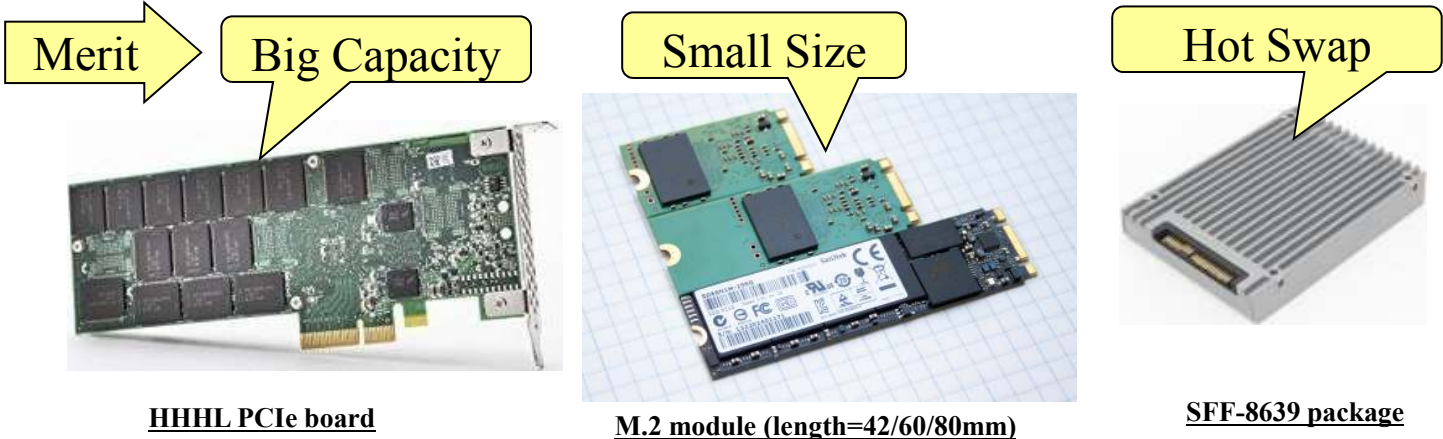
	Read [MB/s]	Write [MB/s]
Seq Q32TI	1563	990.7
4K Q32TI	373.5	273.5
Seq	653.4	966.8
512K	1076	965.8
4K	85.11	110.9

(<http://www.bjorn3d.com/2015/03/480gb-hyperx-predator-m-2-pcie-ssd-shpm2280p2480g/6/>)

Cost and Performance of M.2 PCIe SSD (Kingston 480GB)

Merit of PCIe SSD for Embedded System 2

- Various form factor
 - HHHL(Half-Height,Half-Length) general PCIe board
 - M.2 cost saving module
 - SFF-8639 of 2.5” drive compatible size



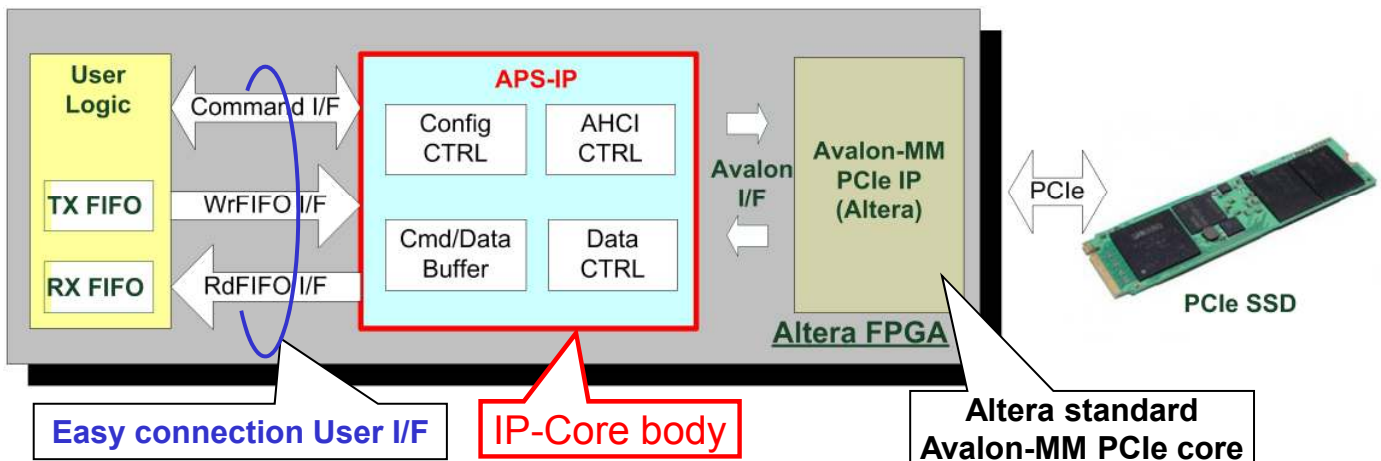
HHHL PCIe board

M.2 module (length=42/60/80mm)

SFF-8639 package

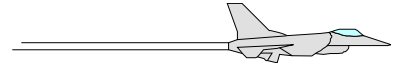
What's APS-IP

- What's APS-IP? -> Reduction of AHCI PCIe SSD IP Core
- Function? -> PCIe Root with full automatic SSD R/W function
- How to use? -> Just connect with user logic, no need CPU&F/W
- User Merit? -> Can develop Storage Application in short period



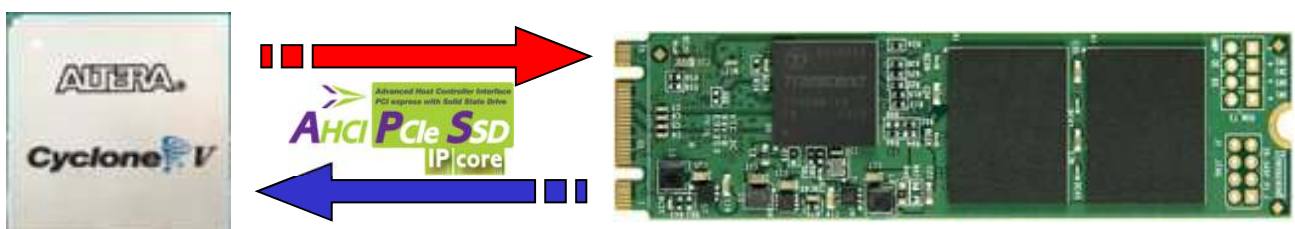
APS-IP Merit

1. **Function: Full automatic access to PCIe SSD**
 - No CPU and firmware necessary, just wired logic is enough
2. **Interface: Simple and easy connection**
 - Direct connection to Altera standard Avalon-MM PCIe core
 - User I/F control is parameter with pulse, data is simple FIFO
3. **High Performance and Compact size**
 - **Write speed=929MB/s, Read speed=859MB/s** (measured speed in real board)
 - Core size=580ALM, 880DFF
4. **Environment: Full reference design project**
 - Full design project with real board operation in the package



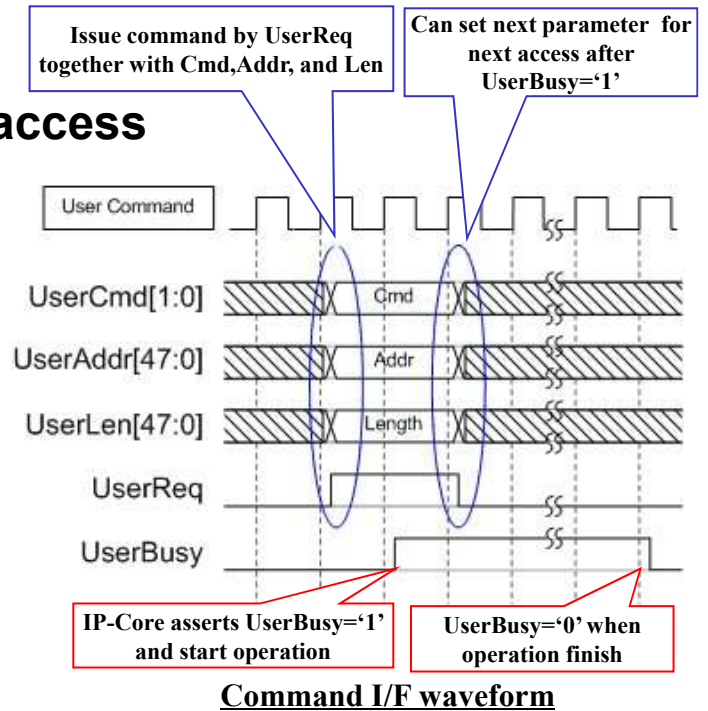
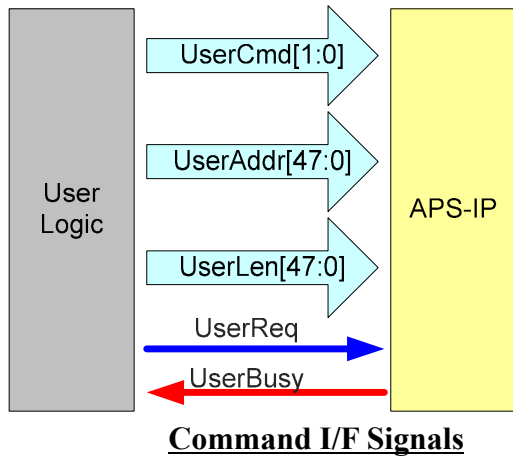
APS-IP Merit 1: Function

- **Special PCIe Root port function for SSD control**
 - PCIe Initialization: BAR Init./MSI Interrupt set/Master mode set
 - SSD Status Monitor: Intr./Status automatic check
- **AHCI Read/Write function**
 - Control AHCI register by user R/W request and execute access
 - Data transfer and flow control between PCIe and FIFO



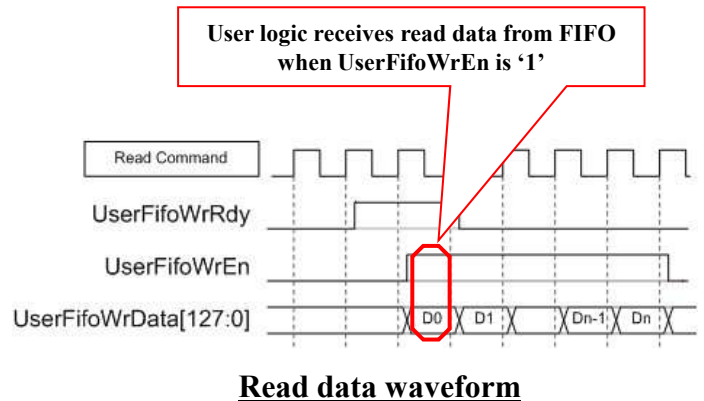
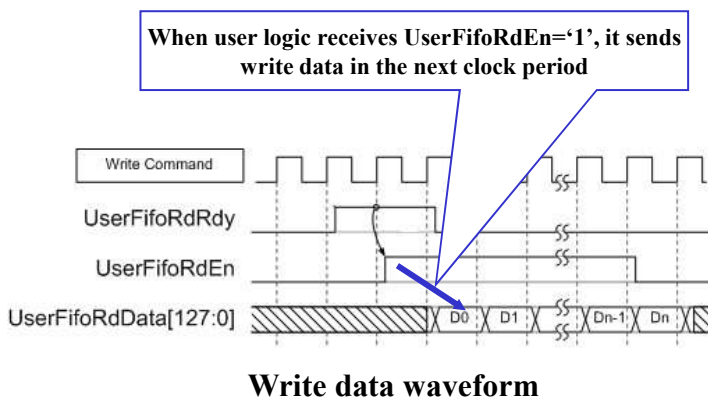
APS-IP Merit2: Command I/F

- **Easy Connection User I/F**
 - Set Command/Address/Length
 - Issue UserReq pulse
- **Full Automatic control for SSD access**
 - User only can wait UserBusy negation



APS-IP Merit2: Data I/F

- **Simple 128bit FIFO for each of read and write**
 - User Logic sends write data by UserFifoRdEn from IP-Core
 - User Logic gets read data with UserFifoWrEn from IP-Core



APS-IP Merit3: Performance

- Automatic PCIe SSD access by pure hard-wired logic
 - Intelligent state machine for complete read/write command execution
 - Minimum over head and best performance by synchronized circuit

Performance Evaluation Result

(SSD: Samsung MZ-HPV2560)

APS-IP Merit3: Compact Size

- Optimized size with minimum resource consumption
 - Includes necessary control logic and temporary buffer only
 - Data FIFO is not in IP-Core so user can select FIFO size
 - 580ALM, 890DFF

Family	Example Device	Fmax (MHz)	Logic utilization (ALMs)	Registers ¹	Design Tools
ArriaV GX	5AGXFB3H4F35C4	125	576	891	QuartusII 14.0
ArriaV ST	5ASTFD5K3F40I3	125	578	861	QuartusII 14.0

Notes: 1) Actual logic resource dependent on percentage of unrelated logic
 (Note: Altera Avalon-MM PCIe core and data FIFO is not included in this result)

APS-IP Core resource usage

APS-IP Merit4: Environment

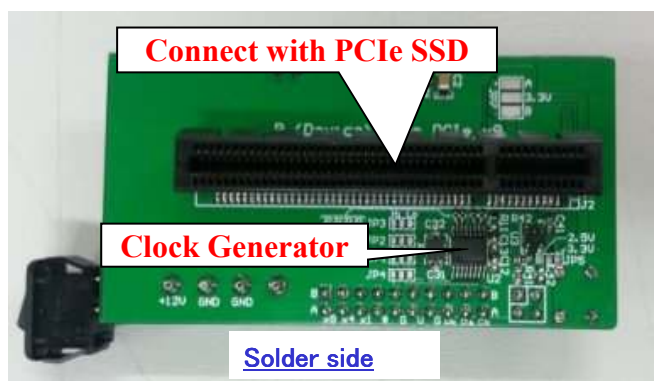
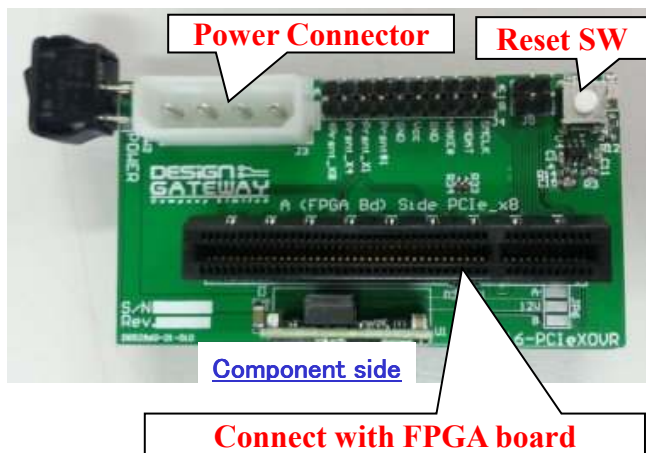
- Real operation check with Altera evaluation board
- Free sof-file for evaluation before IP-core purchase



IP-Core evaluation environment using ArriaV GX Starter Kit

APS-IP Merit4: Development Tool

- Adapter board for FPGA board evaluation (Part#: AB16-PCIeXOVR)
- Connect FPGA board to PCIe socket on component side
- Connect PCIe SSD to PCIe socket on solder side
- SSD R/W access via adapter board from APS-IP in FPGA



APS-IP Merit4: Reference Design

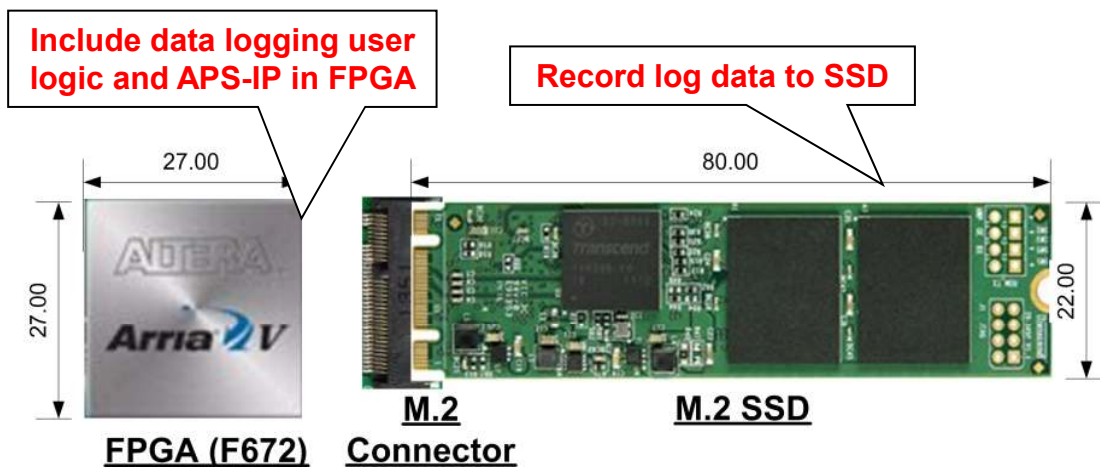
- Vivado project is attached with APS-IP deliverables
- Full source code (VHDL) except IP core
- Can save user system development duration
 - Confirm real board operation by original reference design.
 - Then modify a little to approach final user product.
 - Check real operation in each modification step.



Short-term development is possible without big turn back

APS-IP Application Example

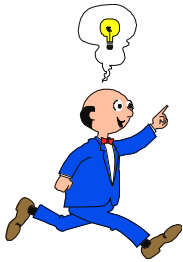
- Space-Saving FPGA data logging system
 - Latest FPGA + M.2 SSD



System space image by F672 package FPGA and M.2 SSD (unit: mm)

For more detail

- Detailed technical information available on the web site.
 - http://www.dgway.com/APS-IP_A_E.html
- Contact
 - Design Gateway Co., Ltd.
 - sales@design-gateway.com
 - FAX: +66-2-261-2290



The Expert of IP Core & Embedded

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AHCI PCI express SSD IP core PCIeSSD Can Directly Connect To FPGA!!

AHCI PCI express SSD IP core (APS-IP) is ideal to access AHCI PCIe SSD without CPU and external memory such as DDR3 requirement. It is recommended to use in the application which require high capacity storage at very high-speed performance. Small size system can be also designed by M.2 storage which uses PCIe protocol standard. The IP core license includes the reference design for Altera FPGA boards. It is useful for your development time more shoat.

Features

- Implement application layer to access AHCI PCIe SSD card by using NCQ command
- Simple user control I/F and FIFO interface for data port
- Small logic utilization and no need for CPU and external memory (DDR)
- Support three ATA commands, i.e. IDENTIFY DEVICE, WRITE FPDMA QUEUED, and READ FPDMA QUEUED
- Reference design with AB16-PCIeXOVR adapter board available on Altera FPGA boards

Revision History

Rev.	Date	Description
1.0E	12-Jan-16	English Version 1st release
1.1E	23-Feb-16	Support ArriaV ST (SoC)