FAT32-IP for SATA reference design manual

Rev1.0 4-Oct-17

1. Introduction

In the hardware system, data stream can be stored to the disk by using raw data or file system. Using raw data, the data is allocated in the disk through physical address. If there are many data types in one disk, the user will need to assign different address for each data group. The disadvantage of raw data is the new users who do not know the memory map of data group in the disk. Therefore, they cannot understand the data in the disk and which area is available to write the additional data.

As a result, file system is created to manage data in the disk by setting up the table to be an index for data that is written to the disk. The data is separated into many groups, each group is called a “file”. For system flexibility, one file has some information to represent itself such as file name, file type, file size, and physical address of data in the file. So, the user can search the data to read the disk and can identify where the free space in the disk available to write new data.

FAT32 is one of the most popular file systems to use in the storage device and file structure is not complicated to build by pure logic. The limitation of FAT32 is maximum partition size is 2 TB and maximum file size is 4 GB.

Generally, when the system accesses the data in the disk through file system, the data transfer speed is lower than raw data. To access file system, it has the overhead time to read the file structure to know the physical address of the data in each file. Also, sometimes the data in one file is split into many parts which store in different physical address. Using file system makes the system more convenient and more flexible, but the performance to write or read the data is reduced, comparing to raw data.

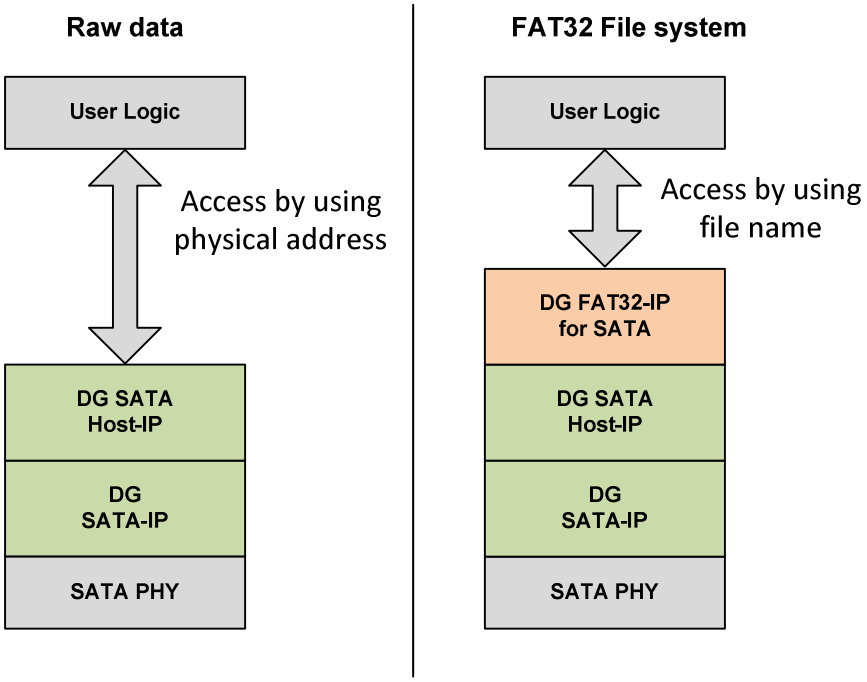

Figure 1-1 Hardware system for Raw data and File system

DG FAT32-IP for SATA implements FAT32 file system by pure-hardware logic which achieve same write and read speed similar to raw data system. As shown in Figure 1-1, raw data system is designed by connecting DG SATA Host-IP, DG SATA-IP, and SATA PHY to transfer high speed data with SATA device. The user interface to access the data of DG SATA Host-IP is physical address.

In order to use FAT32 file system, DG FAT32-IP for SATA is additional block to interface between user logic and DG SATA Host-IP. Instead of using physical address, user can access the data in SATA device by using file name.

More details of FAT32-IP for SATA reference design are described in the next topic.

2. Hardware overview

The reference design of DG FAT32-IP for SATA is modified from SATA Host-IP reference design by adding DG FAT32-IP to Host-IP block, as shown in Figure 2-1

Please see more details of SATA Host-IP reference design from following document.
http://www.dgway.com/products/IP/SATA-IP/Altera/dg_satahostip_refdesign_alt_en.pdf
http://www.dgway.com/products/IP/SATA-IP/Altera/dg_satahostip_instruction_alt_en.pdf

This document describes the modification part from SATA Host-IP reference design.

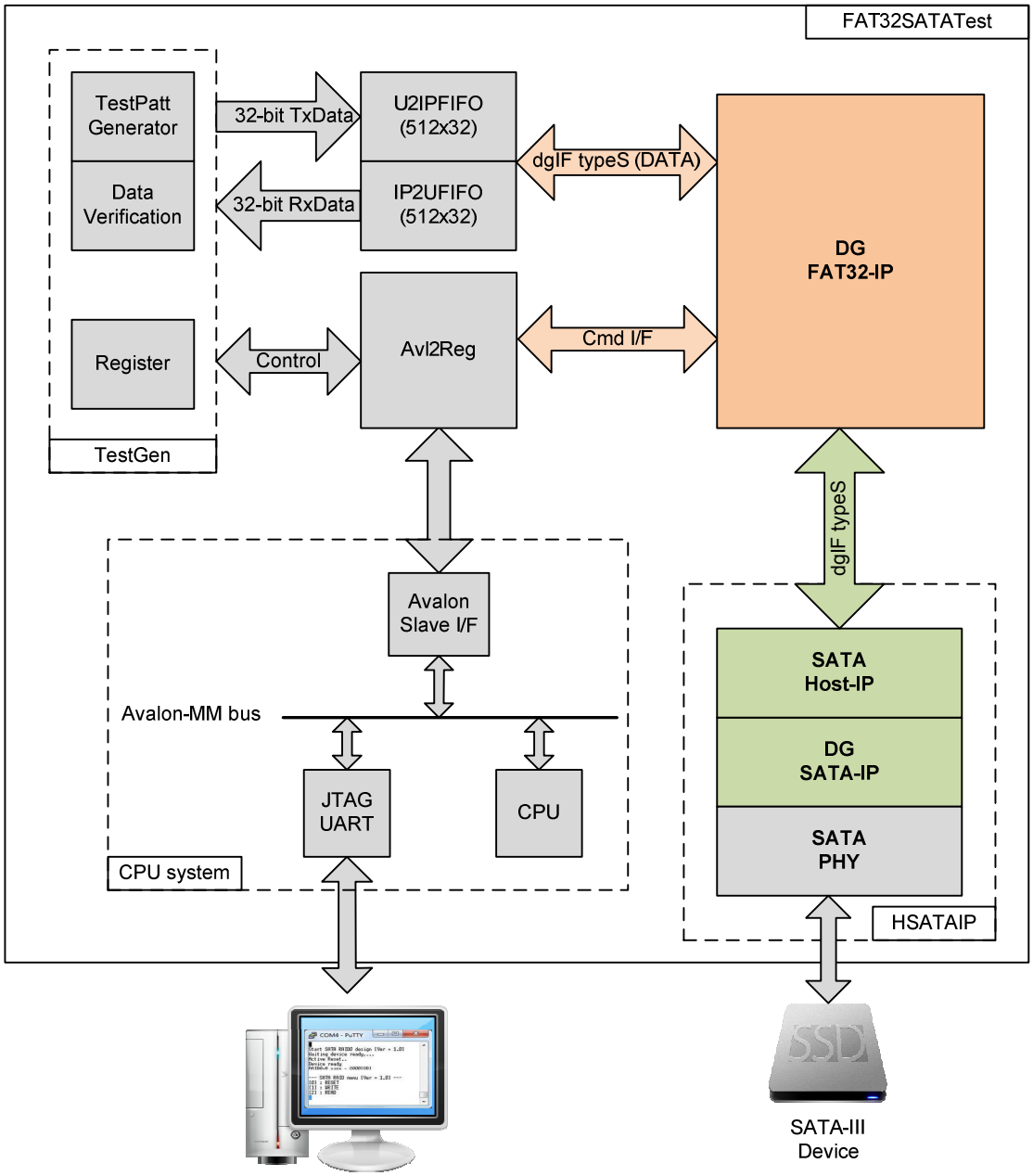

Figure 2-1 FAT32-IP for SATA Demo System

Comparing to SATA Host-IP reference design, the command interface of DG FAT32-IP is file name and numbers of file instead of physical address and length. Data path of DG FAT32-IP still uses dgIF typeS interface. So, TestGen and two FIFOs in test module are same design as SATA Host-IP reference design. Register map within Avl2Reg module is modified to change the parameter inputs from physical layer to be file system.

CPU firmware is designed to receive user command through JTAG UART. There are three menus for three commands, i.e. format, write file, and read file. Transfer performance by using FAT32-IP for SATA is same as performance by using SATA Host-IP. The final performance in the demo depends on the limitation of SATA device.

3. CPU

CPU system in FAT32 for SATA demo is same as SATA Host-IP reference design. But register map for user interface is changed from physical address for raw data access to be file system parameters for file system access. More details are shown in
Table 1.

The details of FAT32-IP for SATA signals are described in the datasheet.
http://www.dgway.com/products/IP/SATA-IP/Altera/dg_sata_host_ip_datasheet_alt_en.pdf

Table 1 Register Map

Address Rd/Wr	Register Name (Label in the "fat32satatest.c")	Description
BA+0x00 Wr	User File Name Reg (USERFNAME_REG)	[15:0]: Input to be UserFName of FAT32-IP for SATA
BA+0x04 Wr	User File Length Reg (USERFLEN_REG)	[15:0]: Input to be UserFLen of FAT32-IP for SATA
BA+0x08 Wr	File Size Reg (FSIZE_REG)	[2:0]: Input to be FSize of FAT32-IP for SATA
BA+0x0C Wr	File Time Reg (DATETIME_REG)	[4:0]: Input to be FTimeS of FAT32-IP for SATA [10:5]: Input to be FTimeM of FAT32-IP for SATA [15:11]: Input to be FTimeH of FAT32-IP for SATA [20:16]: Input to be FDateD of FAT32-IP for SATA [24:21]: Input to be FDateM of FAT32-IP for SATA [31:25]: Input to be FDateY of FAT32-IP for SATA
BA+0x10 Wr	User Command Reg (USERCMD_REG)	[1:0]: Input to be UserCmd of FAT32-IP for SATA When this register is written, the design generates UserReq (command request) to FAT32-IP for SATA to start new command operation.
BA+0x14 Wr	Pattern Select Reg (PATTSEL_REG)	[2:0]: Test pattern select "000"-Increment, "001"-Decrement, "010"-All 0, "011"-All 1, "100"-LFSR
BA+0x1C Wr	User Reset Reg (RESET_REG)	[0]: '1'-Reset test system, '0'-Release reset
BA+0x100 Rd	User Status Reg (USRSTS_REG)	[0]: Mapped to UserBusy of FAT32-IP for SATA [1]: Mapped to UserError of FAT32-IP for SATA [2]: Data verification fail ('0': Normal, '1': Error) [4:3]: SATA speed from SATA-IP "00": No linkup, "01": SATA Gen1 (Not supported for all designs), "10": SATA Gen2 (Not supported for KCU105), "11": SATA Gen3
BA+0x104 Rd	Total file capacity Reg (TOTALFCAP_REG)	[15:0]: Mapped to TotalFCap of FAT32-IP for SATA
BA+0x108 Rd	User Error Type Reg (USRERRTYPE_REG)	[31:0]: Mapped to UserErrorType of FAT32-IP for SATA
BA+0x10C Rd	FAT32-IP Test pin (Low) Reg (TESTPINL_REG)	[31:0]: Mapped to TestPin[31:0] of FAT32-IP for SATA
BA+0x110 Rd	FAT32-IP Test pin (High) Reg (TESTPINH_REG)	[31:0]: Mapped to TestPin[63:32] of FAT32-IP for SATA
BA+0x180 Rd	Failure Byte Address Reg (FAILADDR_REG)	[31:0]: Failure data address in the file
BA+0x184 Rd	Failure File Name Reg (FAILFNAME_REG)	[15:0]: Failure file name
BA+0x190 Rd	Expected value Word0 Reg (EXPPATW0_REG)	[31:0]: Expected data [31:0] of failure address.
BA+0x1A0 Rd	Read value Word0 Reg (RDPATW0_REG)	[31:0]: Read data [31:0] of failure address.
BA+0x1B0 Rd	Current test byte (Low) Reg (CURTESTSIZEL_REG)	[31:0]: Current test data size of TestGen module in byte unit (bit[31:0])
BA+0x1B4 Rd	Current test byte (High) Reg (CURTESTSIZEH_REG)	[7:0]: Current test data size of TestGen module in byte unit (bit[39:32])

CPU firmware is designed to control and set parameters to user interface of FAT32-IP for SATA. The parameters are received from user through JTAG UART. CPU firmware sequence are described as follows.

3.1 Initialization

1) After system boot up, CPU monitors UserBusy flag (USRSTS_REG[0]). CPU waits until FAT32-IP for SATA completes initialization sequence (UserBusy='0').
2) CPU displays maximum numbers of file which can store in this disk by reading TOTALFCAP_REG. This value is calculated by setting file size to be 32 MB (FSIZE_REG="000). User can select "Change file size" menu to update usage file size and TOTALFCAP_REG.
3) Go to main menu to wait the new command from user.

3.2 Format

1) Set USERCMD_REG="00" to format the disk. UserReq to FAT32-IP for SATA is asserted to '1' to start the operation. UserBusy is asserted to '1' by FAT32-IP during formatting.
2) CPU monitors UserBusy flag (USRSTS_REG[0]). CPU goes to next step when UserBusy is de-asserted to '0' (operation is completed) or UserError flag (USRSTS_REG[1]) is asserted to '1'.
3) If the operation is completed without error, CPU will display maximum numbers of file which can store in the disk (TOTALFCAP_REG) to the NiosII terminal.
   If the error is found, error message will be displayed instead.

3.3 Write file or read file

1) Receive the parameters from user (the 1st File name, total numbers of file to transfer, and test pattern format) through the NiosII terminal. If some inputs are invalid, the operation will be cancelled.
   In case of write file operation, user can select to change created date and time of the file or use current value. The created date and time value are set to DATETIME_REG.
2) Set the inputs from user to internal registers (USERFNAME_REG, USERFLEN_REG, and PATTSEL_REG). After that, CPU sets USERCMD_REG="10" or "11" to start write file or read file operation.
3) During operating, CPU displays total transfer size (CURTESTSIZE_REG) to the NiosII terminal every second.
   In case of read file operation, Data failed flag (USRSTS_REG[2]) is monitored. If data failed flag is asserted to '1', warning message will show failure data position (FAILADDR, FILENAME), expected test data (EXPPATW0_REG), and read data (RDPATW0_REG) to the NiosII terminal. User can press some keys to cancel the operation.
4) The operation is stopped when UserBusy is de-asserted to '0' (operation is completed) or UserError flag (USRSTS_REG[1]) is asserted to '1'.
   If operation is completed, total transfer speed will be displayed on the NiosII terminal.
   If the error is found, error message will be displayed instead.

3.4 Change File size

1) Receive new file size value from user through NiosII terminal. If the input is valid and UserBusy='0', the new value will be set to FSIZE_REG.
2) CPU displays maximum numbers of file which can store in the disk by reading TOTALFCAP_REG. Warning message is also displayed to format the disk when file size is changed.

4. Avl2Reg and TestGen

Hardware block of both modules are same as SATA Host-IP reference design. Please see more details of SATA Host-IP reference design.

The different point from SATA Host-IP is the register map of UserReg module inside Avl2Reg. The new register is mapped following Table 1.

5. Example Test Result

The example test result when running demo system by using 256 GB Samsung 850 Pro is shown in Figure 5-1.

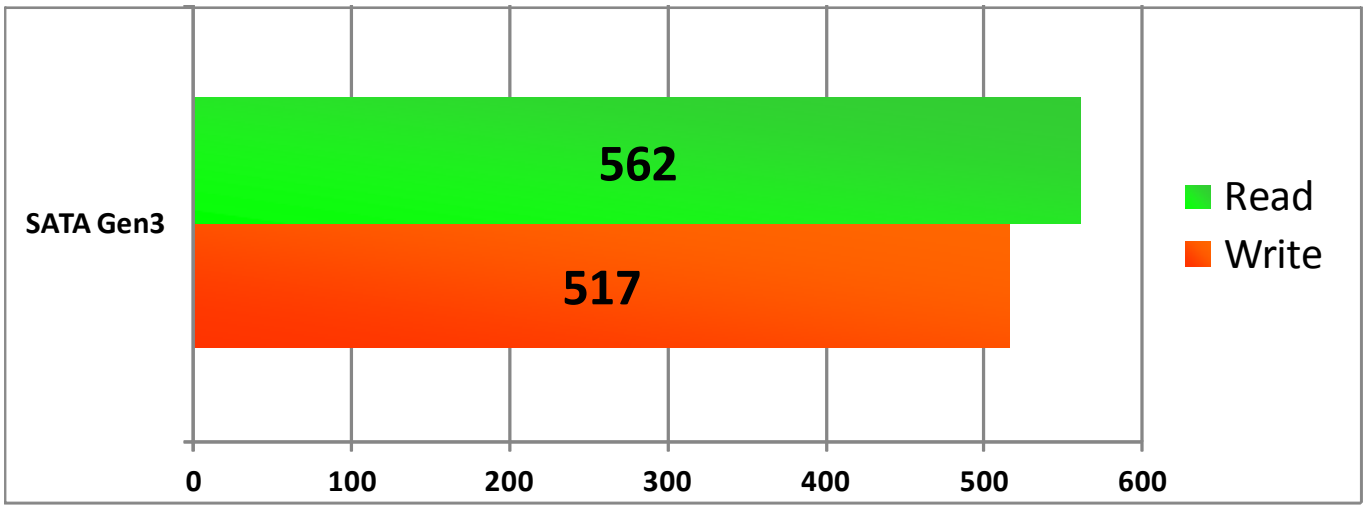

Figure 5-1 Test Performance of FAT32-IP demo by using Samsung 850 Pro SSD

By using SATA Gen3 on Arria10 SoC board, write performance is about 517 Mbyte/sec and read performance is about 562 Mbyte/sec.

6. Revision History

Revision	Date	Description
1.0	4-Oct-17	Initial Release