

HCTL-IP Demo Instruction

Rev1.3 6-Jul-23

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HCTL-IP Demo Instruction

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This document describes the instruction to run SATA HCTL-IP demo on FPGA development board using AB09-FMCRAID/AB12-HSMCRAID adaptor board. The demo is designed to write/verify data with SATA-III device. User controls test operation through NiosII command shell.

1 Environment Setup

To run the demo on IntelFPGA board, please prepare following environment.

- 1) IntelFPGA board:
 - ArriaV GX Starter board
 - Arria10 SoC Development board
 - Alaric board from Reflex
 - Arria10 GX Development board
- 2) PC with QuartusII programmer and NiosII command shell software
- 3) SATA adapter board
 a) AB09-FMCRAID: For Arria10 SoC board/Arria10 GX board/Alaric board
 b) AB12-HSMCRAID: For ArriaV GX board
- 4) SATA-III device
- 5) Power adapter for FPGA board and ATX power supply for SSD
- 6) USB cable for FPGA programming and NiosII command shell, connecting between FPGA board and PC
 - a) micro USB cable: For Arria10 SoC/Arria10 GX board/Alaric board
 - b) USB A-B cable: For ArriaV GX Starter board







Figure 1-2 HCTL-IP Demo Environment Setup on Arria10 SoC Development Board



Figure 1-3 HCTL-IP Demo Environment Setup on Alaric board





DG

 $dg_satahctlip_instruction_intel_en$

2 Demo setup

- 1) Power off system.
- 2) Setup board option.
 - i) For ArriaV GX Starter board only, set bit1 of SW4 to OFF position.



Figure 2-1 Set SW to select clock input for ArriaV GX Starter board

- 3) Setup SATA adapter board
 - i) For Arria 10 SoC Development board/Arria10 GX Development board/Alaric board: Connect AB09-FMCRAID to FMC#A

For ArriaV GX Starter board: Connect AB12-HSMCRAID to HSMC

- ii) Connect SATA-III device to CN0 on AB09/AB12.
- iii) Connect power to power connector on AB09/AB12.



Figure 2-2 AB09/AB12 connection to FPGA board



4) Connect USB cable from FPGA board to PC for JTAG programming and JTAG UART.



- 5) Power on FPGA development board and power supply for SATA device.
- 6) Only ArriaV GX Starter board, open "Clock Control" application to program 150 MHz clock, as shown in Figure 2-4. Select 1st tab (U4), set CLK0 frequency = 150 MHz, and click "Set New Frequency" button.

U4 X1								
F_vco: 000MHz Desisters Executency (MHz) Disable all								
CLK0 - CLK0 150.00 Disable CLK0								
CLK1 - CLK1 150.00 Disable CLK1								
CLK2 - CLK2 150.00 Disable CLK2								
CLK3 - CLK3 150.00 Disable CLK3								
read Default Set New Frequency								
Messages /USB-BlasterII on localhost (USB-1)/5M(1270ZF324 2210Z) EPM221002								



7) Open QuartusII Programmer to program "HSataIPTest.sof" file, as shown in Figure 2-5.

<u>E</u> dit <u>V</u> iew P <u>r</u>	ocessing <u>T</u> ools <u>W</u> indow <u>H</u> el;	P 9			Search	altera.com	
Hardware Setup	USB-Blasterii [USB-1]	Mode: JTAG		Progress:	100%	6 (Success	ful)
Enable real-time ISP	to allow background programming w	vhen available					
▶ [™] Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank
Mi Stop	D:/SATA-IP/HostIP/HSataIPTest.sof	5AGXFB3H4F35	04979C38	04979C38			
Auto Datast	<none></none>	5M2210Z	00000000	<none></none>			1
Y Delete							
		111					
Add File Change File Save File		ADTERA					
Add File Change File Save File Add Device							
Add File Change File Save File Add Device							
Add File Change File Save File Add Device TUD Down All	TDI SAGXFB3H4F35 TDO Control Control Contro			Eind	Find Next	ŧ	
Add File Change File Change File Save File Add Device Tup Up Up Up Coven All O 209061	TDI SAGXFB3H4F35 TDO SAGXFB3H4F35 TDO Message Ended Programmer oper	5M2210Z	Oct 28 15:3	Eind 1:08 2016	e Find Next	ł	

Figure 2-5 Programmed by QuartusII Programmer

8) Open NiosII Command Shell and run nios2-terminal command. Boot message is displayed.

"Waiting device ready" is displayed during system initialization.

"SATA Gen3 Device Detect" is displayed after initialization is completed.

Finally, Main menu is displayed to receive command from user.

/cygdrive/c/altera/16.0	- • •
++++ Stant SOTOHost-IP Test design [llen = 1 3] ++++	<u>^</u>
Waiting device ready Wait SATA Linkup	
SATA Gen3 Device Detect SATA Speed = Gen3	
Main menu [Ver = 1.3] [0] : Identify Device [1] : Write SSD [2] : Read SSD [3] : Security Erase	
	-
▲ III	► La

Figure 2-6 NiosII Terminal



9) Check LED status on FPGA board. The description of LED is shown as follows. <u>Note</u>: LED [3] is not available on Alaric board. There are three LEDs on the board.

GPIO LED	ON	OFF							
0	Normal operation	System is in reset condition							
1	System is busy	Idle status							
2	Error detect	Normal operation							
3	Data verification fail	Normal operation							

Tabla	1		Dofinition
Table		LED	Delinition





Figure 2-7 LED Status after initialization complete

10)After programming completely, LED[0] and LED[1] are ON during SATA initialization process. LED[1] is OFF after SATA HCTL-IP completes initialization process and system is ready to receive command from user.



Figure 2-8 LED status after program configuration file and SATA initialization complete



3 Test Menu

3.1 Identify Device

Select '0' to send Identify device command to SATA device. When the command operation is completed, the information of SATA device is displayed on the console.

♦: User input♦: User output								
0 +++ Identifu Deuice selected +++	Device model number							
Model Number : Samsung SSD 850 PRO 256G Security feature set is supported Normal Erase Mode Time=2 minutes	B Security Erase supported and erase time							
SSD Gapacity= 2561GB1	SATA Device capacity							
Main menu [Ver = 1.3] [0] : Identify Device [1] : Write SSD [2] : Read SSD [3] : Security Erase								
Figure 3-1 Result from Identify	Device menu							

- 1) Device Model number: Show the SATA device model number connected to the board.
- 2) Security feature set: Supported or not supported. If the device is not supported, user must not run menu 3: Security erase command.
- 3) Normal Erase Mode Time: This is the estimation time to complete Security erase command. Minimum valid value is 2 minutes. This information is displayed when the device supports Security feature set.
- 4) Device capacity which is the output from HCTL-IP.



3.2 Write SSD

	♦: User input
	♦: User output
1 +++ Write data selected +++ Enter Start LBA : 0 - 0x1DCF32AF Enter Sector Count : 1 - 0x1DCF32I Selected Pattern [0]Inc32 [1]Dec32 517.787 MB 1.036 GB	=> 0 Input from user 80 => 0x1000000 2 [2]All_0 [3]All_1 [4]LFSR=> 4
7.261 GB 7.781 GB 8.299 GB	Output performance
Iotal = 8[GB] , Time = 16[s] , Tra	ansfer speed = 518[MB/s]
Main menu [Ver = 1.3] [0] : Identify Device [1] : Write SSD [2] : Read SSD [3] : Security Erase	
Figure 3-2 Input and resi	ult of Write SSD menu

Select '1' to send Write command to SATA device. Three inputs are required for this menu.

- 1) Start LBA: Input start address of SATA device in 512-byte unit. The input is decimal unit when input only digit number. User can add "0x" as a prefix for hexadecimal input.
- 2) Sector Count: Input total transfer size in 512-byte unit. The input is decimal unit when input only digit number. User can add "0x" as a prefix for hexadecimal input.
- 3) Test pattern: Select test pattern of test data for writing to SATA device. Five patterns can be selected, i.e., 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

As shown in Figure 3-2, if all inputs are valid, the operation is run. While operating Write command, the console displays the current amount of transferred data to indicate that the system is running. Finally, test performance, total size, and total time usage are displayed on the console as a test result.



<─64-bit header of each sector →								\leftarrow	64-bi	it hea	der	of ea	ich s	ecto	\rightarrow																	
	48	-bit L	BA	Addr	ess		0x00	000		3	32-bi	t incr	eme	nt da	ata		48	3-bit	LBA	Addr	ess		0x0	000			32-b	it LF	SR p	atter	m	
Offset	0	1	2	3	4	5	6	7	8	9	A	В	C	D	Е	F	0	1	2	3	4	5	6	7	8	9	A	в	с	Þ	E	F
0000000000	00	00	00	00	00	00	00	00	02	00	00	00	03	00	00	00	00	00	00	00	00	00	00	00	01	00	00	00	02	00	00	00
0000000010	04	00	00	00	05	00	00	00	06	00	00	00	07	00	00	00	04	00	00	00	09	00	00	00	12	00	00	00	24	00	00	00
0000000020	08	00	00	00	09	00	00	00	0A	00	00	00	OB	00	00	00	49	00	00	00	92	00	00	00	24	01	00	00	49	02	00	00
000000030	0C	00	00	00	OD	00	00	00	0E	00	00	00	OF	00	00	00	92	04	00	00	24	09	00	00	49	12	00	00	92	24	00	00
0000000040	10	00	00	00	11	00	00	00	12	00	00	00	13	00	00	00	24	49	00	00	49	92	00	00	92	24	01	00	24	49	02	00
0000000050	14	00	00	00	15	00	00	00	16	00	00	00	17	00	00	00	49	92	04	00	92	24	09	00	24	49	12	00	49	92	24	00
0000000060	18	00	00	00	19	00	00	00	1A	00	00	00	1B	00	00	00	93	24	49	00	27	49	92	00	4F	92	24	01	9E	24	49	02
0000000070	1C	00	00	00	1D	00	00	00	1E	00	00	00	1F	00	00	00	3C	49	92	04	79	92	24	09	FЗ	24	49	12	E7	49	92	24
000000080	20	00	00	00	21	00	00	00	22	00	00	00	23	00	00	00	CF	93	24	49	9E	27	49	92	ЗD	4F	92	24	7A	9E	24	49
0000000090	24	00	00	00	25	00	00	00	26	00	00	00	27	00	00	00	F5	3C	49	92	EB	79	92	24	D7	FЗ	24	49	AE	E7	49	92
0A000000A0	28	00	00	00	29	00	00	00	2A	00	00	00	2B	00	00	00	5D	CF	93	24	BA	9E	27	49	75	ЗD	4F	92	EB	7A	9E	24
0000000B0	2C	00	00	00	2D	00	00	00	2E	00	00	00	2F	00	00	00	D7	F5	3C	49	ΑE	EB	79	92	5C	D7	F3	24	B8	AE	E7	49
000000000000000000000000000000000000000	30	00	00	00	31	00	00	00	32	00	00	00	33	00	00	00	70	5D	CF	93	ΕO	BA	9E	27	C1	75	ЗD	4F	83	EB	7A	9E
00000000D0	34	00	00	00	35	00	00	00	36	00	00	00	37	00	00	00	07	D7	F5	3C	OE	AE	EB	79	1D	5C	D7	FЗ	ЗB	B8	ΑE	E7
00000000E0	38	00	00	00	39	00	00	00	ЗA	00	00	00	3B	00	00	00	77	70	5D	CF	EE	ΕO	BA	9E	DC	C1	75	ЗD	B8	83	EB	7A
00000000F0	3C	00	00	00	3D	00	00	00	3E	00	00	00	ЗF	00	00	00	70	07	D7	F5	ΕO	OE	AE	EB	C1	1D	5C	D7	83	ЗB	B8	ÀΕ
0000000100	40	00	00	00	41	00	00	00	42	00	00	00	43	00	00	00	07	77	70	5D	0E	EE	ΕO	BA	1C	DC	C1	75	39	B8	83	EB
0000000110	44	00	00	00	45	00	00	00	46	00	00	00	47	00	00	00	73	70	07	D7	E6	EO	OE	AE	CD	C1	1D	5C	9A	83	3B	88
0000000120	48	00	00	00	49	00	00	00	4A	00	00	00	4B	00	00	00	34	07	77	70	68	OE	EE	EO	D1	1C	DC	C1	A3	39	B8	83
000000130	4C	00	00	00	4D	00	00	00	4E	00	00	00	4F	00	00	00	47	73	70	07	8E	E6	EO	0E	1D	CD	C1	1D	3A	9A	83	3B
000000140	50	00	00	00	51	00	00	00	52	00	00	00	53	00	00	00	74	34	07	77	E9	68	UE	EE	D3	D1	1C	DC	Ab	A3	39	88
000000150	54	00	00	00	55	00	00	00	56	00	00	00	57	00	00	00	40	47	73	70	98	8E	Eb CO	EU	31	10	CD	C1	63	3A	9A	83
000000160	58	00	00	00	59	00	00	00	58	00	00	00	55	00	00	00	CB	/9	34	72	8D DC	E9	68	DE	IB	21	10	IC OD	3/	A0 63	83 23	39
0000000170	50	00	00	00	5U 6 1	00	00	00	55	00	00	00	10	00	00	00	DE E1	40	4/	24	00	90	5C FO	60	DO	10	10	CD D 1	70	03	38	9A 3.2
0000000180	60	00	00	00	61	00	00	00	66	00	00	00	67	00	00	00	13	60	40	17	24	DC	6.9	00	60	1D DO	21	10	DO	37	6 D	22
0000000190	69	00	00	00	60	00	00	00	60	00	00	00	6P	00	00	00	3.0	5L F1	40	74	41	03	90 90	FO	00	96	18	10	06	00	37	3A 86
00000001R0	60	00	00	00	6D	00	00	00	6F	00	00	00	6E	00	00	00	AU OC	12	65	40	18	34	DC	98	30	68	RS	31	60	DO	70	63
0000000100	70	00	00	00	71	00	00	00	72	00	00	00	73	00	00	00	CO	20	F1	26	81	41	03	8D	03	83	86	1B	00	06	nn.	37
0000000100	74	00	00	00	75	nn	00	00	76	nn	00	00	77	00	nn	00	OF	00	14	6F	1F	18	34	DC	3F	30	68	B8	7F	60	DΩ	70
0000000120	78	00	00	00	79	00	00	00	74	00	00	00	7B	00	00	00	FF	co	AO	E1	FF	81	41	C3	FE	03	83	86	FD	07	06	nD
00000001E0	70	00	00	nn	70	nn	nn	00	7F	nn	nn	00	7F	nn	nn	00	FA	0F	nc	1A	F4	1F	18	34	E9	3F	30	68	D.3	7F	60	DΩ
0000000200	01	00	00	00	00	00	00	00	82	00	00	00	83	00	00	00	1	00	00	00	00	00	00	00	02	00	00	00	04	00	00	00
0000000210	84	00	00	00	85	00	00	00	86	00	00	00	87	00	00	00	09	00	00	00	12	00	00	00	24	00	00	00	49	00	00	00
0000000220	88	00	00	00	89	00	00	00	8A	00	00	00	8B	00	00	00	92	00	00	00	24	01	00	00	49	02	00	00	92	04	00	00
000000230	8C	00	00	00	8D	00	00	00	8E	00	00	00	8F	00	00	00	24	09	00	00	49	12	00	00	92	24	00	00	24	49	00	00
			64	l-bit	head	ler													64	l-bit l	head	ler										

Figure 3-3 Example Test data in sector#0/#1 by increment/LFSR pattern

Test data of each 512-byte block has different 64-bit header which consists of 48-bit LBA address and 16-bit all 0 value. 48-bit LBA address is unique value for each 512-byte block. The data after 64-bit header is the test pattern which is selected by user. The example of test pattern is shown in Figure 3-3. 32-bit incremental pattern is shown in the left window and 32-bit LFSR pattern is shown in the right window.



ผิดพลาด! ไม่พบแหล่งการอ้างอิง – ผิดพลาด! ไม่พบแหล่งการอ้างอิง show error message when user input is invalid. "Invalid input" is displayed on the console and then it returns to main menu to receive new command.

> 1 +++ Write data selected +++ Enter Start LBA : 0 - 0x1DCF32AF => 0x20000000 Invalid input Error message Out-of-range LBA address --- Main menu [Ver = 1.3] ---[0] : Identify Device [1] : Write SSD [2] : Read SSD [3] : Security Erase

Figure 3-4 Invalid Start LBA input

```
+++ Write data selected +++
Enter Start LBA : 0 - 0x1DCF32AF => 0
Enter Sector Count : 1 - 0x1DCF32B0 => 0x1dcf32b1
Invalid input Out-of-range length
--- Main menu [Ver = 1.3] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
[3] : Security Erase
```

Figure 3-5 Invalid Sector count input

```
1

+++ Write data selected +++

Enter Start LBA : 0 - 0x1DCF32AF => 0

Enter Sector Count : 1 - 0x1DCF32B0 => 0x1000000

Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 5

Invalid input Out-of-range pattern

--- Main menu [Ver = 1.3] ---

[0] : Identify Device

[1] : Write SSD

[2] : Read SSD

[3] : Security Erase
```

Figure 3-6 Invalid Test pattern input



3.3 Read SSD

Select '2' to send Read command to SATA device. Three inputs are required for this menu.

- 1) Start LBA: Input start address of SATA device in sector unit. The input is decimal unit when input only digit number. User can add "0x" as a prefix for hexadecimal input.
- 2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" as a prefix for hexadecimal unit.
- 3) Test pattern: Select test pattern to verify data from SATA device. Test pattern must be matched with the test pattern using in Write Command menu. Five patterns can be selected, i.e., 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.



When all inputs in the Read command menu are valid, the test system starts reading data from the SATA device. While operating Read command, the console displays the amount of transferred data every second. Upon completion of the data transfer, the test performance, total size, and time usage are displayed as a test result. However, if some inputs are out-of-range, the console displays "Invalid input".



Figure 3-8 and Figure 3-9 show the error message when data verification is failed. "Verify fail" is displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until the read operation is done.

In case of cancel operation, the previous command does not complete in a good sequence. It is recommended to power-off/on SATA device and press "RESET" button to restart system.

```
+++ Read data selected +++
Enter Start LBA : 0 - 0 \times 1 \text{DCF32AF} = > 0
Enter Sector Count : 1 - 0 \times 1 \text{DCF32BO} = > 0 \times 1000000
Selected Pattern [0]Inc32 [1]Dec32 [2]A11_0 [3]A11_1 [4]LFSR=> 0
                                                                        Wrong pattern
Verify fail
1st Error at Byte Addr = 0x00000008
                               = 0×0000002
Expect Data
                                                  Verify failure message
Read Data
                                = 0×0000001
Press any key to cancel operation
561.947 MB
  1.125 GB
                   No cancel operation
  7.319 GB
7.882 GB
  8.445 GB
                                                        Output performance
Total = 8[GB] , Time = 15[s] , Transfer speed = 563[MB/s]
   - Main menu [Ver = 1.3] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD _
[3] : Security Erase
      Figure 3-8 Data verification is failed but wait until read complete
 +++ Read data selected +++
Enter Start LBA : 0 - 0x1DCF32AF => 0
Enter Sector Count : 1 - 0x1DCF32B0 => 0x1000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 0
 Verify fail
 1 \text{ st Error} at Byte Addr = 0x00000008
                                = 0×0000002
 Expect Data
                                                   Verify failure message
 Read Data
                                = 0×0000001
Press any key to cancel operation
Operation is cancelled
Please reset system before start new test cancel the operation
   -- Main menu [Ver = 1.3] ---
 [0] : Identify Device
[1] : Write SSD
 [2] : Read SSD
 [3] : Security Erase
  Figure 3-9 Data verification is failed and press key to cancel operation
```

3.4 Security Erase

Select '3' to send Security Erase command to SATA Device. Please confirm that SATA device supports Security Erase feature using Identify device menu. The estimated time of security erase operation is also displayed in Identify device menu.

After selecting the menu, confirmation message is displayed on the console. User inputs 'y' or 'Y' to continue Security erase operation or inputs other keys to cancel operation.

While operating this command, the console displays an incremental number every second to indicate that the command is operating. After the operation is completed, total time usage is displayed as a test result.



Figure 3-10 Result from Security Erase command

Figure 3-11 shows the example when user inputs other keys to cancel the command.

```
+++ Security Erase selected +++
Security Erase will erase all contents on SSD
It may use long time for this operation
Press 'y' to confirm = nCancel operation Message after cancel
--- Main menu [Ver = 1,3] ---
[0] : Identify Device 'n' to cancel operation
[1] : Write SSD
[2] : Read SSD
[3] : Security Erase
```

Figure 3-11 Cancel Security Erase command



4 Revision History

Revision	Date	Description
1.3	27-Feb-23	Support A10GX
1.2	15-Nov-17	Add LFSR pattern and Alaric board
1.1	24-Nov-16	Correct security erase menu
1.0	28-Oct-16	Initial version release