



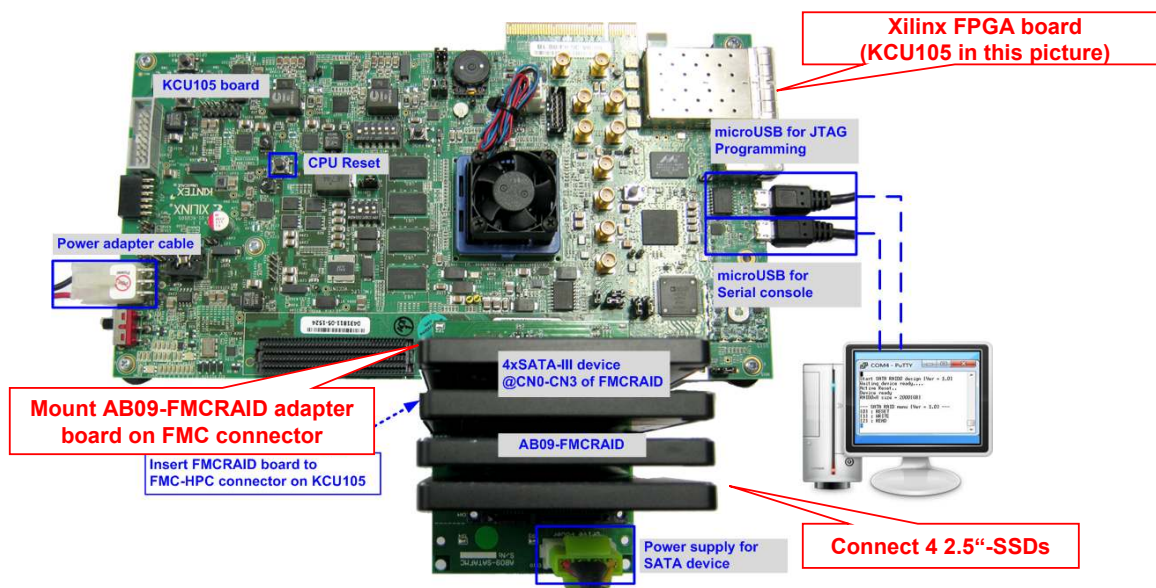
SATA-IP RAID prototype system for Xilinx FPGA

System Outline

- RAID prototype for the latest Xilinx FPGA
- Use RAID adapter board (AB09-FMCRAID)
- Operate 4-channel RAID0 (parallel access)
- Standard and High Performance version
- Show read/write result to PC via RS232C
- Execute test pattern read/write
- Display measured transfer performance



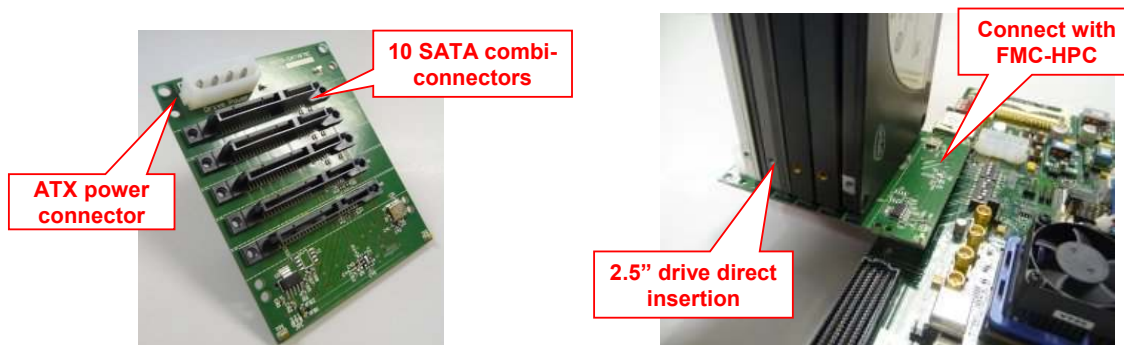
Prototype System



RAID prototype system using Xilinx FPGA board

RAID Adapter Board

- Can support up to 10 SATA channels (each 5 SATA ports on both component and solder side)
- Connect with FMC-HPC connector on Xilinx FPGA board
- 2.5''-SSD/HDD drive direct insertion
- Drive power supply via standard ATX power connector
- Part Number: AB09-FMCRAID
- Available on Mouser website <https://www.mouser.com/>

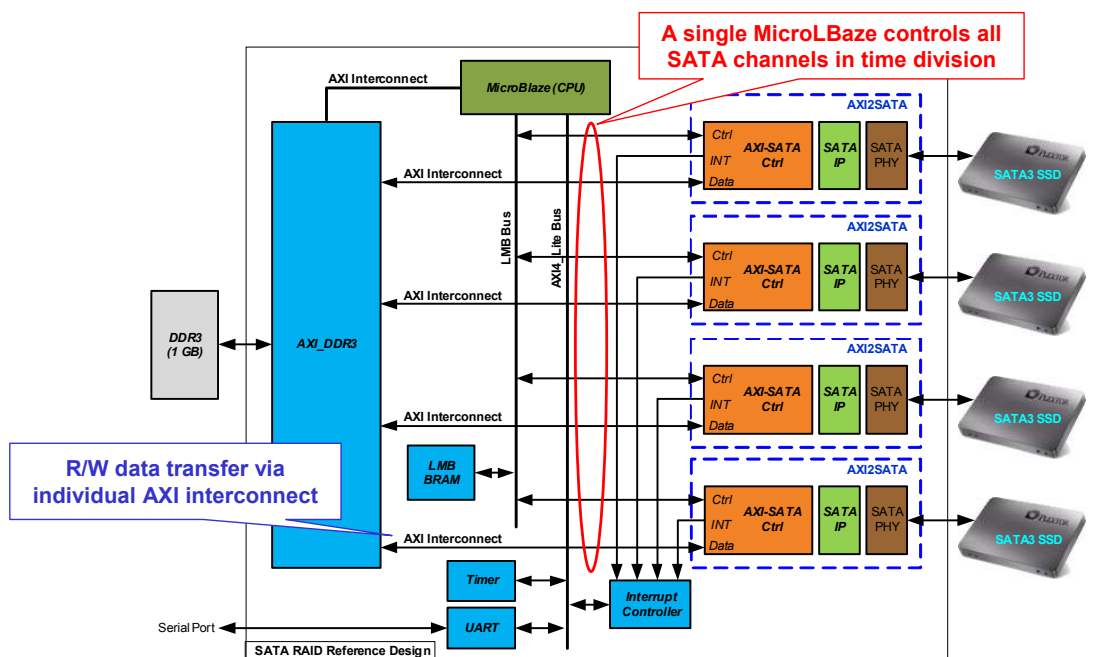


Two types RAID design

- **Standard Version (MicroBlaze control)**
 - Use MicroBlaze for SATA-IP controller
 - All channel control by time division in CPU F/W
 - Requires SATA-IP only (no need HCTL-IP)
- **High Performance Version (HCTL-IP control)**
 - Use HCTL-IP core for SATA-IP controller
 - Minimum latency, Maximum performance
 - Requires Both SATA-IP and HCTL-IP core

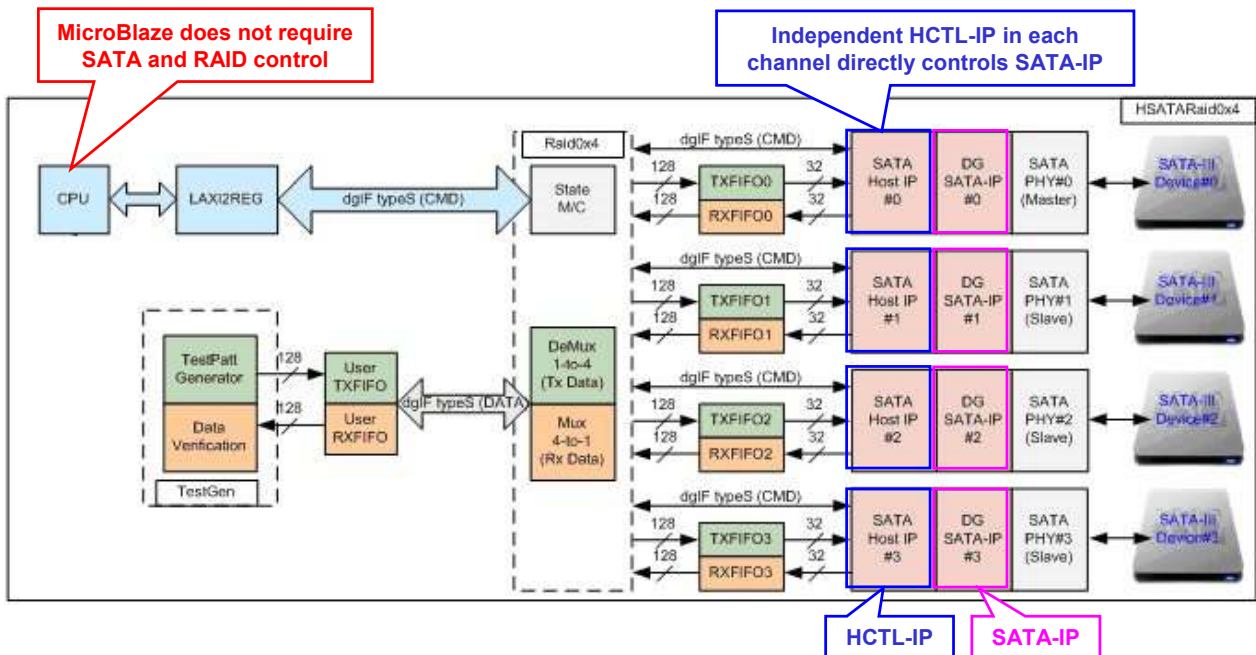


Standard Version Block Diagram



Standard version RAID prototype system block diagram

High Performance Version Block Diagram



High Performance version RAID prototype system block diagram

Write Result (High Performance Version)

32GByte Write Result

Read Result (High Performance Version)

Set transfer size
0x4000000 sector = 32GB

Set data pattern
4 = LFSR pseudo random pattern

Read = 2225MB/s

4ch RAID Read Performance result

[Measurement Condition]
FPGA: KCU105 board
SSD: Samsung 850PRO x 4
High Performance Version

32GByte Read Result

RAID Performance

- **Write speed efficiency=99%**
 - Single=520MB/s, 4ch-RAID=2068MB/s
 - Speed efficiency = $2068 / (4 \times 520) = 99\%$
- **Read speed efficiency=97.29%**
 - Single=560MB/s, 4ch-RAID=2225MB/s
 - Speed efficiency = $2225 / (4 \times 560) = 99\%$

↓

Almost 100% speed efficiency

RAID Design in deliverables

- Vivado project is attached with SATA-IP and/or HCTL-IP product
- Full source code except IP core
 - VHDL for hardware and C for MicroBlaze firmware
- Can save user system development duration
 - Confirm real board operation by original reference design
 - Then modify a little to approach final user product
 - Check real operation in each modification step



Short-term development is possible without big turn back

Conclusion

- Can build RAID prototype with FPGA & RAID adapter
 - Quick check of RAID system without new board building
- RAID performance is almost 100% of single drive total
 - Multiply performance by drive count
- Prototype design is available for SATA-IP users
 - Reduce RAID system development period based on this design



For more detail

- Detailed technical information available on the web site.
 - https://dgway.com/SATA-IP_X_E.html
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Revision History

Rev.	Date	Description
1.0	04-Jun-09	RAID prototype system introduction 1st release
1.1E	21-Feb-13	Updated to KC705 based RAID system
1.3E	03-Sep-18	Added latest family support, added high performance version description

THANK YOU

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