Serial ATA-IP core Introduction

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Introduction

SerialATA(SATA) IPcore compliant with the Serial ATA specification revision 2.6 and work on Xilinx Virtex5 and Spartan6 device.
This IPcore provide link layer. Design Gateway provide transport layer and 20bit 150MHz RocketIO GTP physical layer design for 3.0Gbps SATA-II interface as reference design. It can connect with SATA-II HDD without PHY chip
We provide 1-hour limitation bit files for Xilinx ML505/ML506 and SP605 board. You can evaluate SATA-IPcore on your board.

Features

- Compliant with the Serial ATA specification revision 2.6
- Support both of SATA Host and SATA Device (Applicable to SATA Peripheral development)
- Simple transaction interface with Host processor or DMA Engine
- 32-bit internal data path
- 4KB FIFO implemented by BlockRAM in transmit and receive paths
- Support SATA-II (SATA-I support is also possible by PHY parameter settings change)
- Low frequency operation
  - IP Core clock 75.0MHz and PHY clock 150MHz for SATA-II
  - IP Core clock 37.5MHz and PHY clock 75MHz for SATA-I
- CONT primitive support for continue primitive suppression to reduce EMI
- Support 20bit width PHY implemented by Virtex5 GTP
- Able to evaluate on ML505/ML506 and SP605 board before purchasing the IPcore

Block diagram

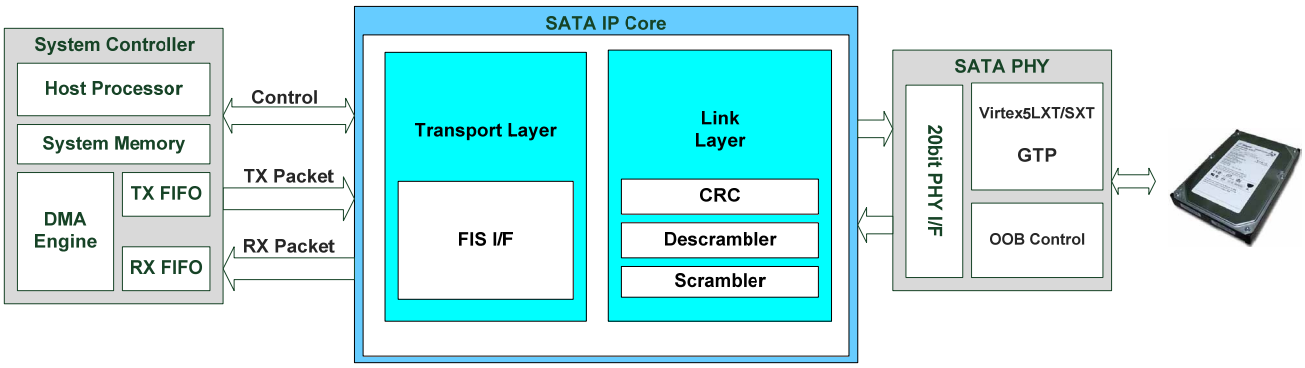


Fig1 Block diagram of SATA-IPcore

Resources

Table1: Example Implementation Statistics

Family	Example Device	Fmax (MHz)	Slices[1]	IOB[2]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Virtex®-5 (SXT)	XC5VSX50T-1FFG1136C	208	579	121	6	2	0	2	1	ISE® 10.1.03i
Spartan-6 LXT	**XC6SLX45T-3FGG484**	**227**	**514**	**121**	**3**	**2**	**0**	**1**	**1**	**ISE® 11.1.04i**

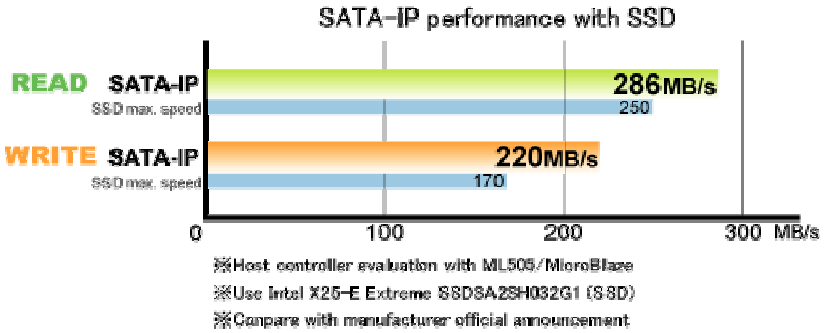
Notes:
1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming all core I/Os and clocks are routed off-chip
3) GCLK, DCM/CMT, and MGT resource is not used in SATA IP core, but they are used in SATA PHY design. GCLK and DCMresource utilizations are from speed auto negotiation SATA PHY. Only 1 DCM and 4 GCLKs are applied for fixed-speed SATA PHY

Provided with Core

- NGC Netlist
- Test Bench, Simulation Library
- ISE/EDKProject, Reference Design for ML505/ML506 or SP605
- Datasheet, Users guide and Design guide

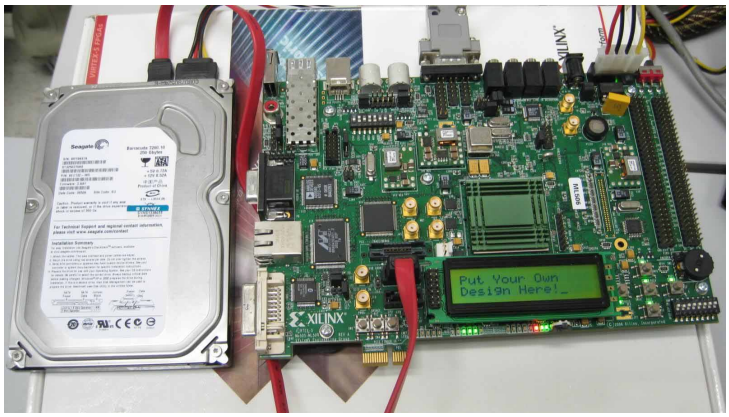
Performance

SerialATA-IPcore can draw maximum HDD performance because of SATA-II supporting. This IPcore is checked on Seagate, IBM/Hitachi, WesternDigital, Samsung HDD, Intel and PhotoFast SATA-II SSD (Jul 2009)



Evaluation by SP605 or ML505/506

We provide 1-hour limitation bit files for Xilinx ML505/ML506 and SP605 board. You can evaluate SATA-IPcore on your board before you purchase this IP. For more detail, please see Design Gateway web page.



SATA-IP with RAID system

By several SerialATA-IPcore implementation on FPGA, you can achieve RAID system with SerialATA HDD. This IPcore make simple wiring on a board and reducing FPGA I/O pins. It is best solution for RAID system that uses many HDD. Design Gateway provide SerialATA extension adaptor board for ML555 that can build RAID system with up to 8 HDD. Moreover Design Gateway have RAID technologies (RAID0,RAID1,RAID5). About integration of SerialATA-IPcore with RAID, please contact us.