SATA-IP Host Demo Instruction on 7-Series and KCU105

Rev2.0 23-Aug-23

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This document describes SATA-IP Host evaluation procedure using SATA-IP Host reference design bit-file on AC701, KC705, ZC706, VC707, VC709, and KCU105 board. The design on VC709 and KCU105 can support fixed SATA-III device only while other boards can run for both SATA-II and SATA-III devices.

1 Environment

For real board evaluation of Host reference design, environment setup is shown in Figure 1-1 - Figure 1-6.

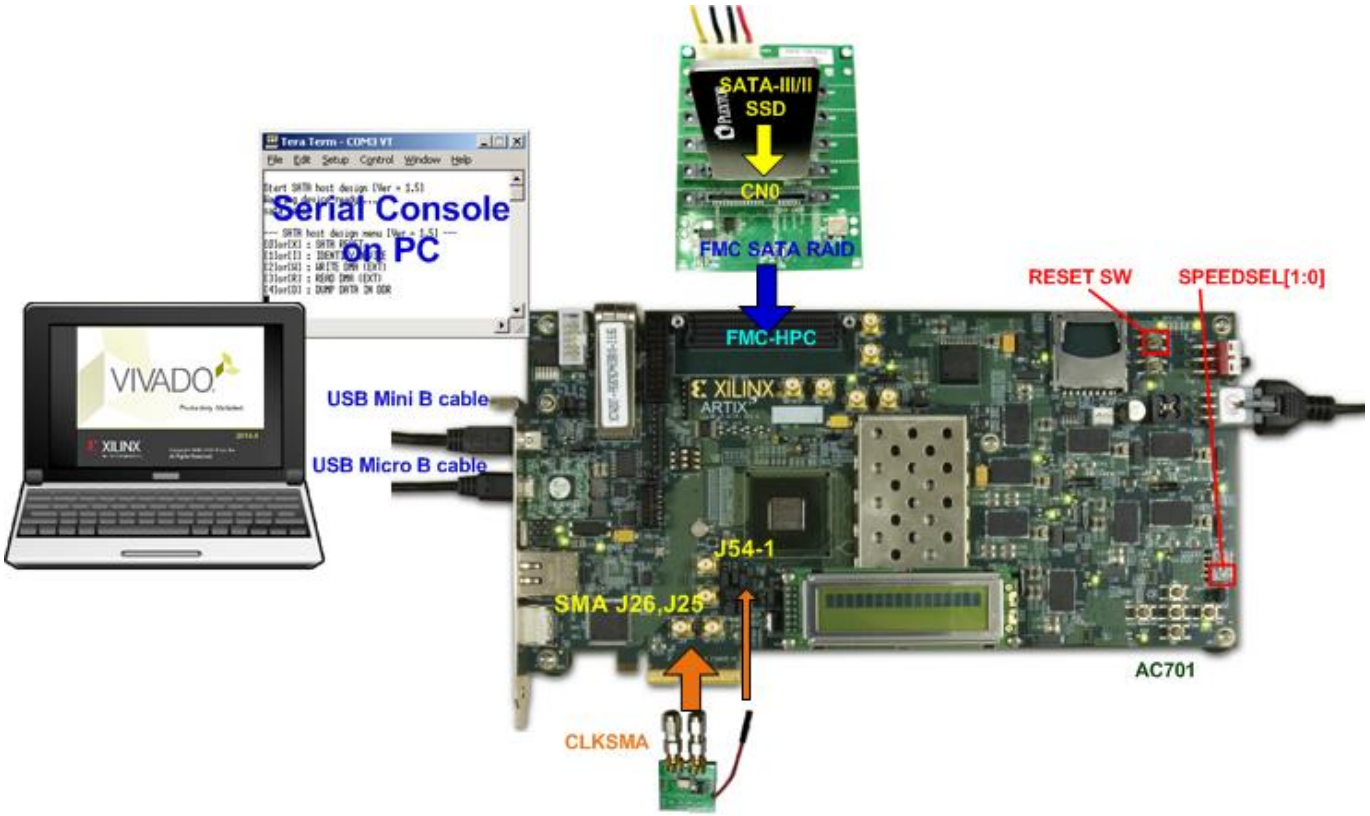

Figure 1-1 SATA-IP host demo environment on AC701 board

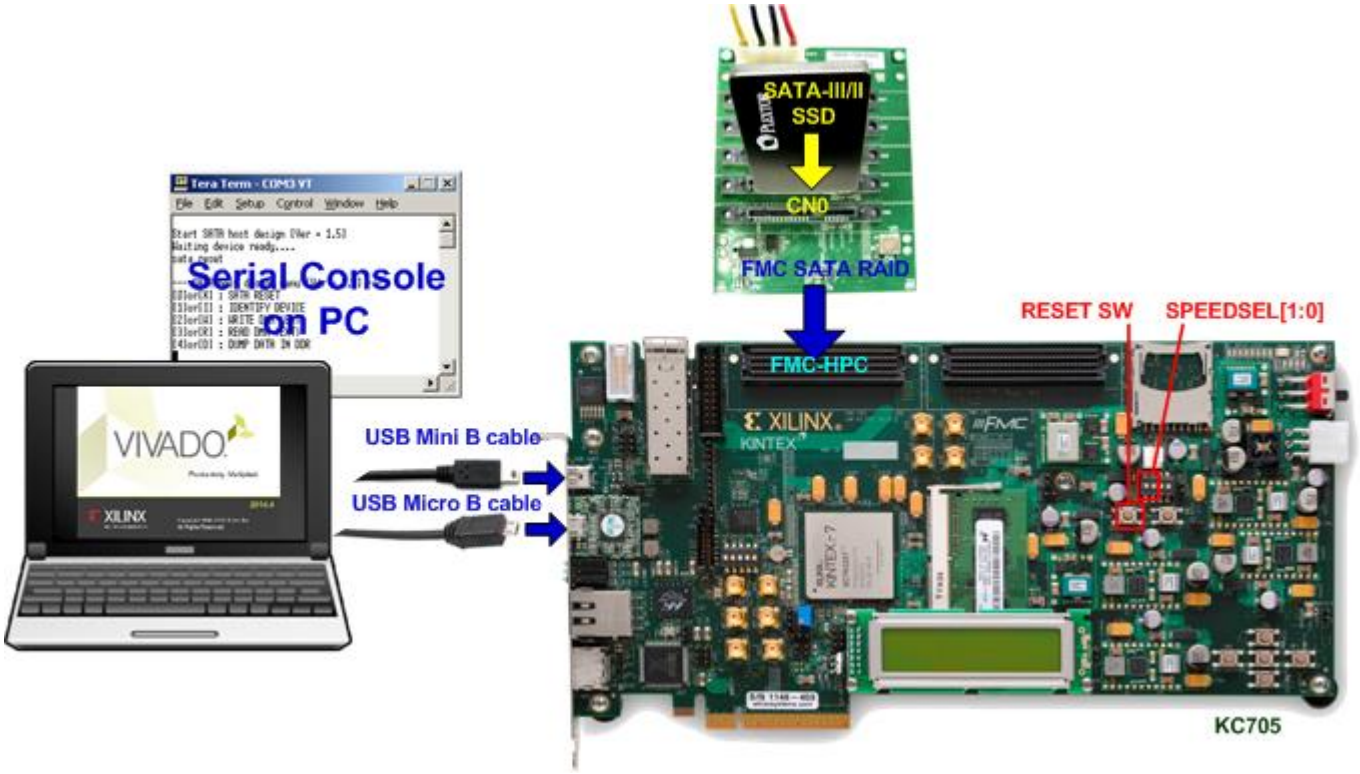

Figure 1-2 SATA-IP host demo environment on KC705 board

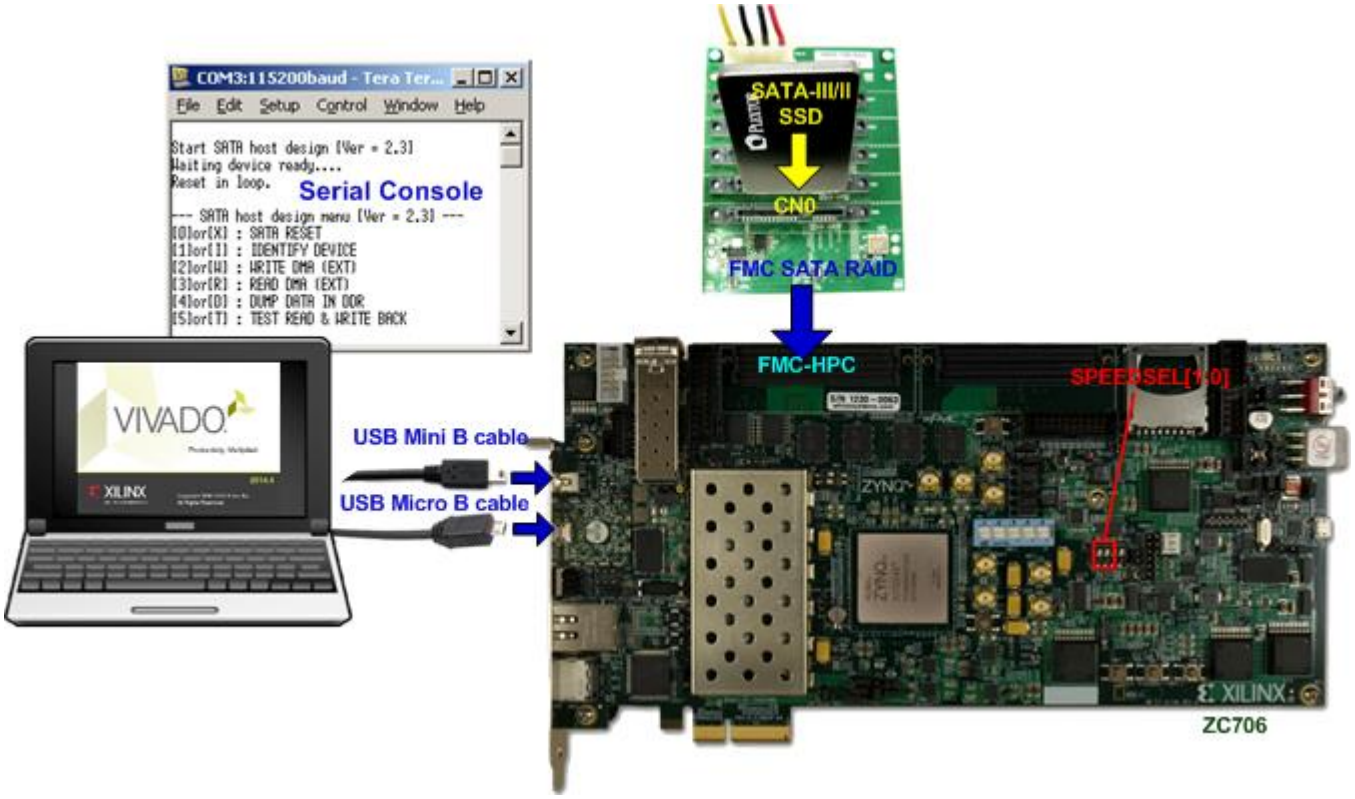

Figure 1-3 SATA-IP host demo environment on ZC706 board

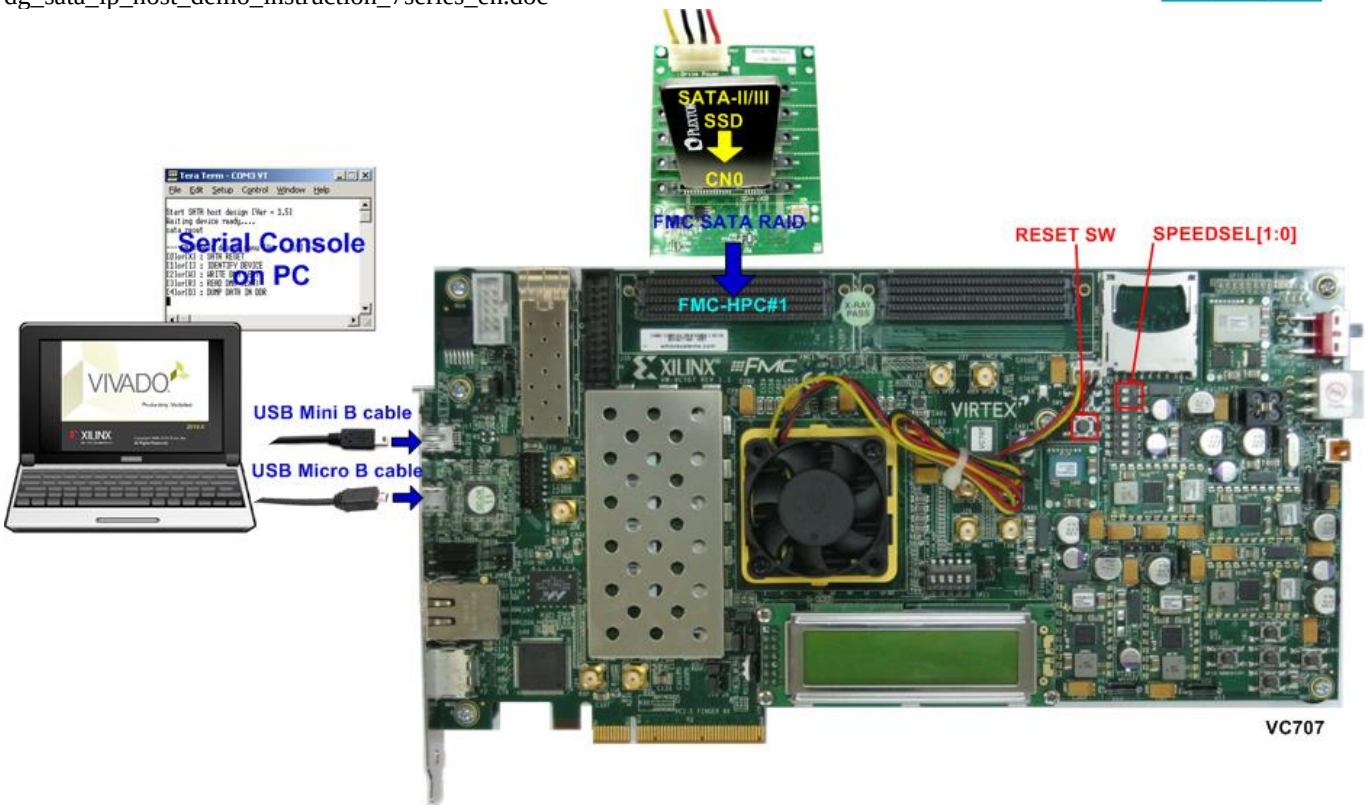

Figure 1-4 SATA-IP host demo environment on VC707 board

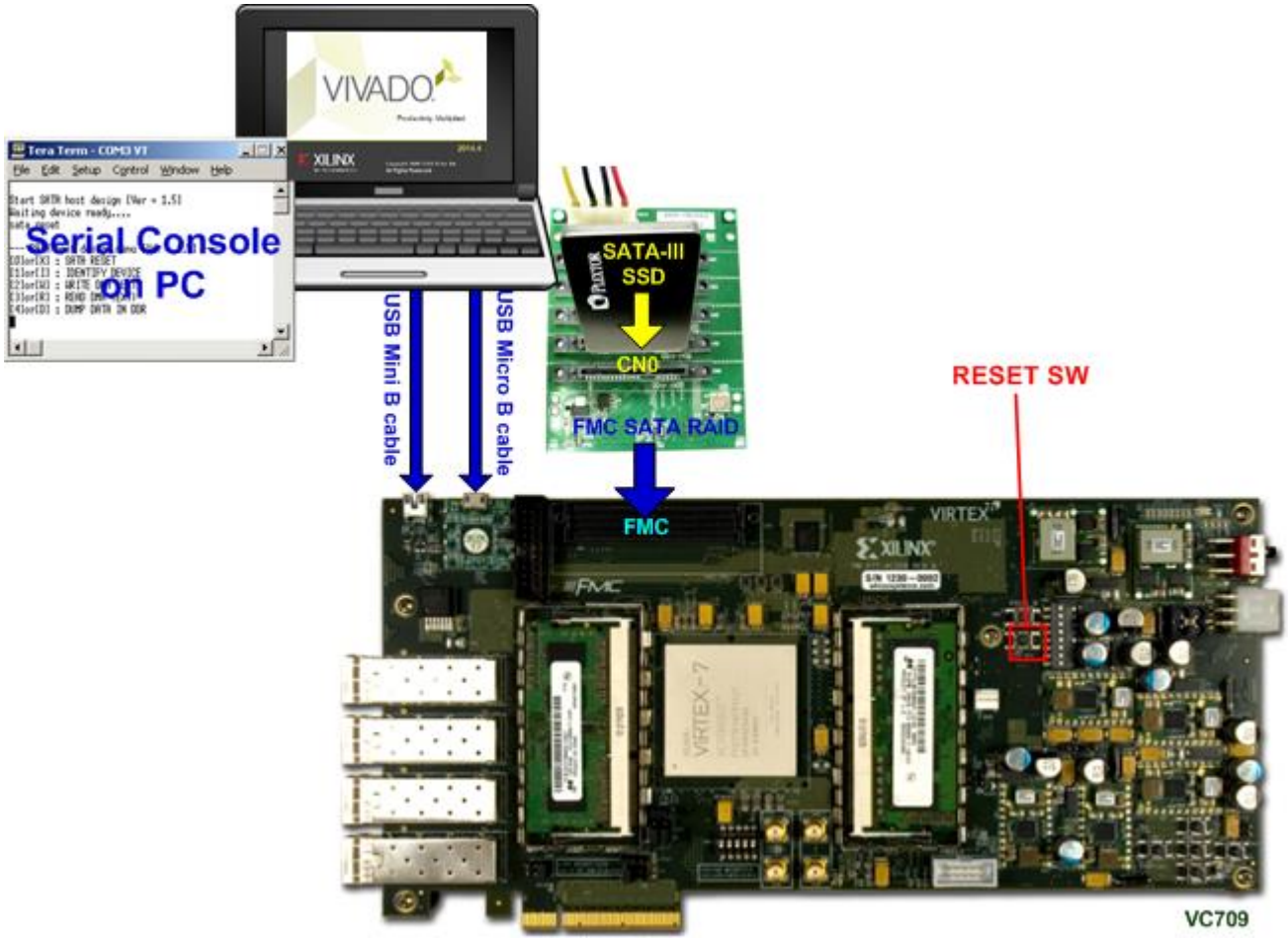

Figure 1-5 SATA-IP host demo environment on VC709 board

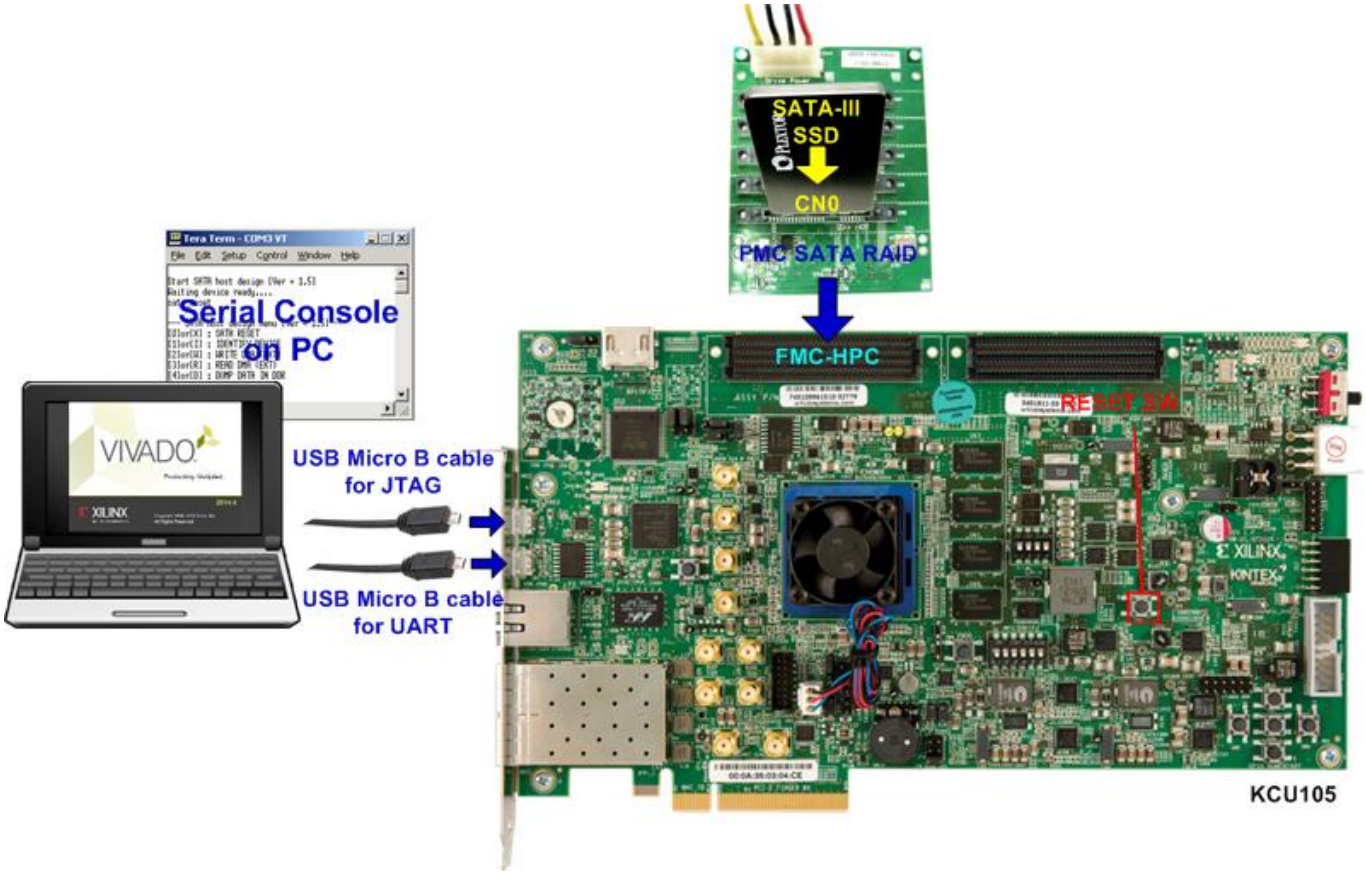

Figure 1-6 SATA-IP host demo environment on KCU105 board

2 Evaluation procedure

- Check all system is power off.
- Connect FMC SATA RAID board to FMC-HPC(#1) connector.
  Note: FMC SATA RAID board is provided by Design Gateway.
- Connect power to power connector on FMC SATA RAID board.
- Connect SATA3/SATA2 Device to CN0 on FMC SATA RAID board.
- For AC701, KC705, ZC706, and VC707 board which support both SATA-II and SATA-III device, set DIPSW bit [2:1] at GPIO DIPSW position (SW2@AC701, SW4@KC705, SW12@ZC706, and SW2@VC707) to select SATA speed mode. The description is described in Table 2-1.

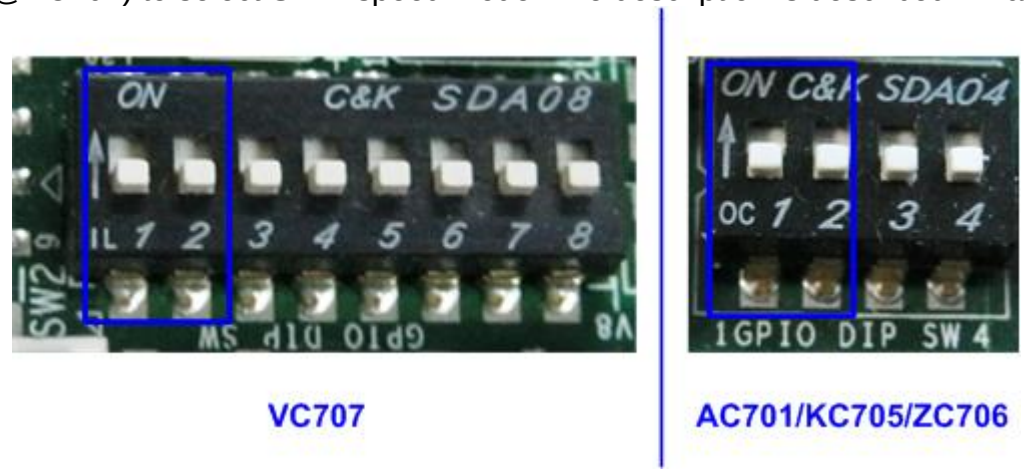

Figure 2-1 DIPSW setting for selecting auto-negotiation mode

DIPSW[2]	DIPSW[1]	Description
'1'	'1'	Fixed-speed at SATA3 (6.0 Gbps)
'1'	'0'	Fixed-speed at SATA2 (3.0 Gbps)
'0'	'X'	Auto-speed negotiation mode

Table 2-1 DIPSW setting to select SATA speed

- Connect USB mini/micro B cable from USB UART port on FPGA board to PC for Serial Console. KCU105 uses micro B cable while others use mini B cable.
- Connect USB micro B cable from Digilent on FPGA board to PC for JTAG programming.

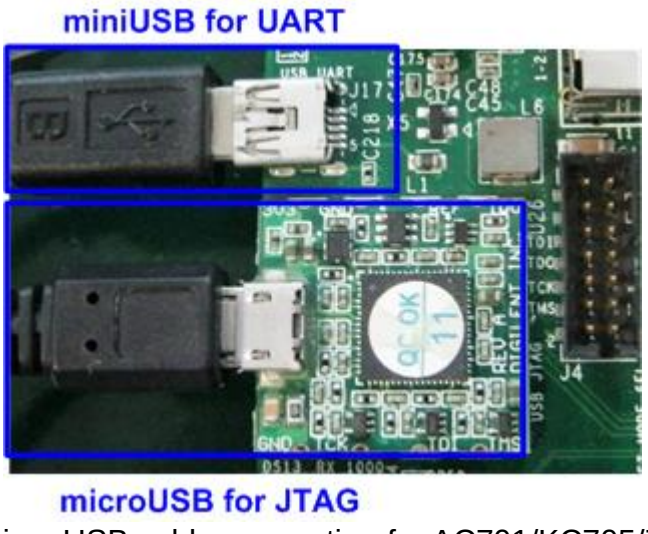

Figure 2-2 mini and micro USB cable connection for AC701/KC705/ZC706/VC707/VC709

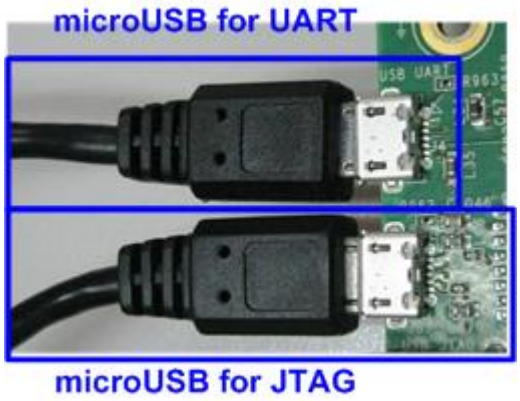

Figure 2-3 two micro USB cable connections on KCU105

- Connect Power cable to FPGA board and then power up.
- Open serial monitoring software such as HyperTerminal. Terminal settings should be (Baud Rate=115,200 Data=8 bit Non-Parity Stop=1).
- Download bit-file to FPGA board
  - For ZC706 board, please follow below steps.
  1) Copy “ready_for_download” folder to PC.
  2) Open “ISE Design Suite Command Prompt” and change working directory to “ready_for_download” folder.

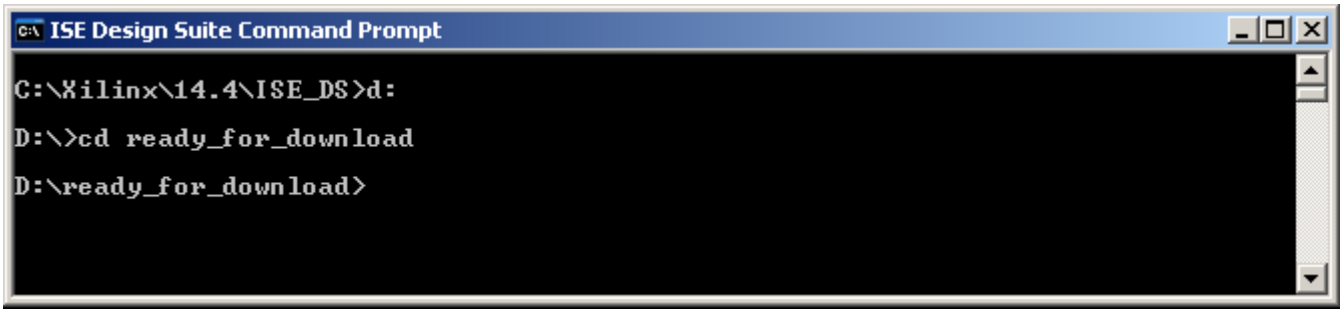

Figure 2-4 ISE Design Suite Command Prompt for ZC706 board

3) Type “zc706_bist.bat” to start downloading configuration file and the firmware. On the console, “Download 10 … Done” is displayed after both bit file and firmware file are loaded complete. Then, user can exit this menu and see LED status and Serial console.

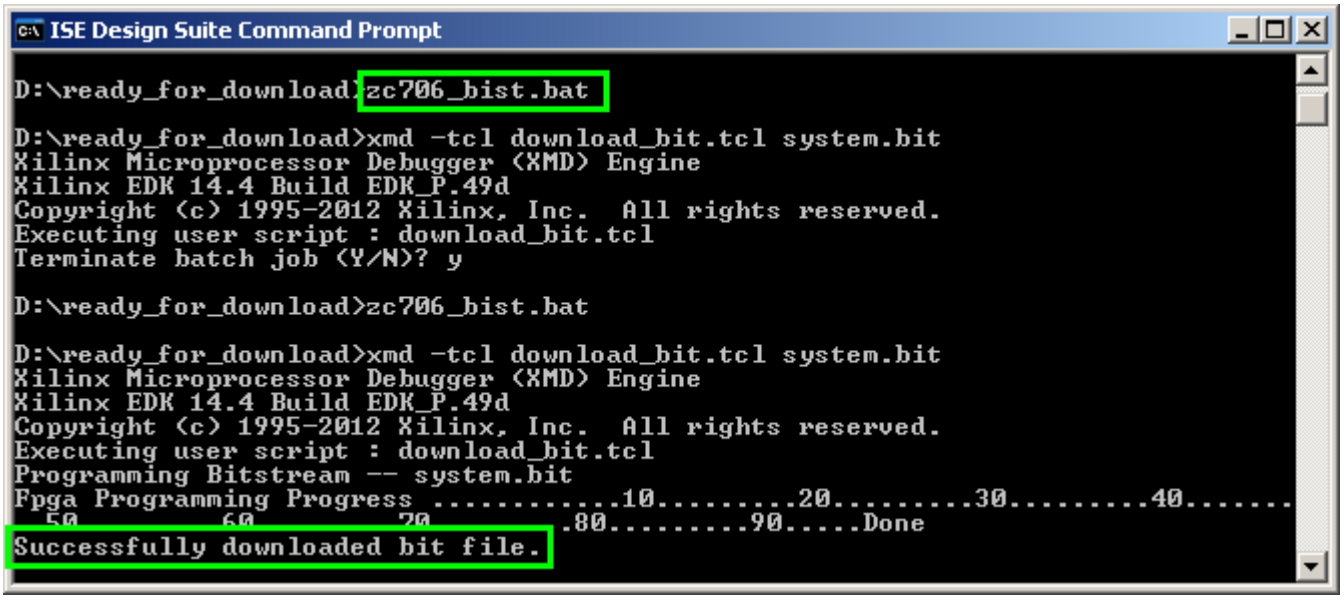

Figure 2-5 Downloading configuration file for ZC706 board

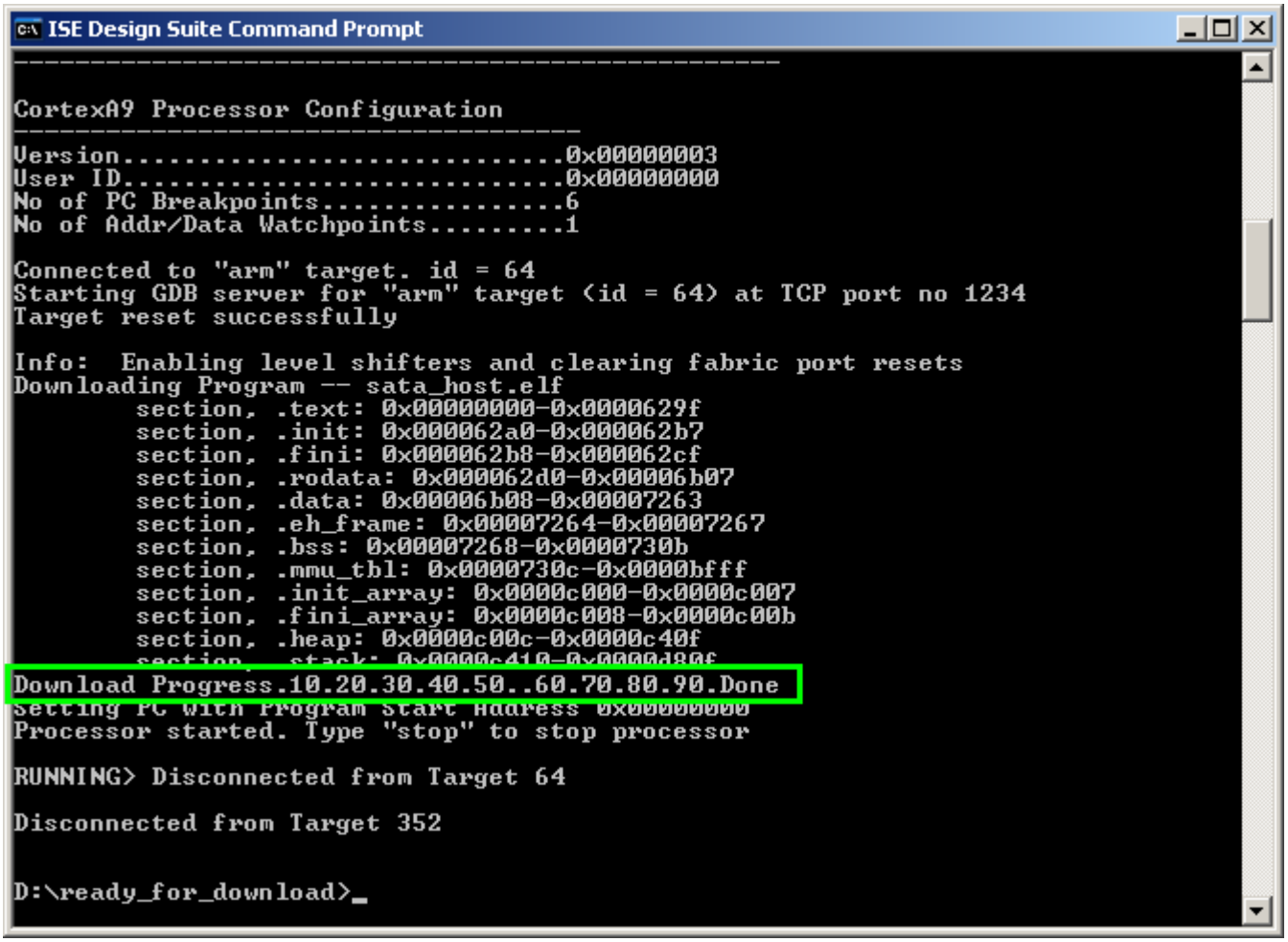

Figure 2-6 End of Downloading Firmware for ZC706 board

- For other boards, bit file can be downloaded from Vivado or iMPACT tool.

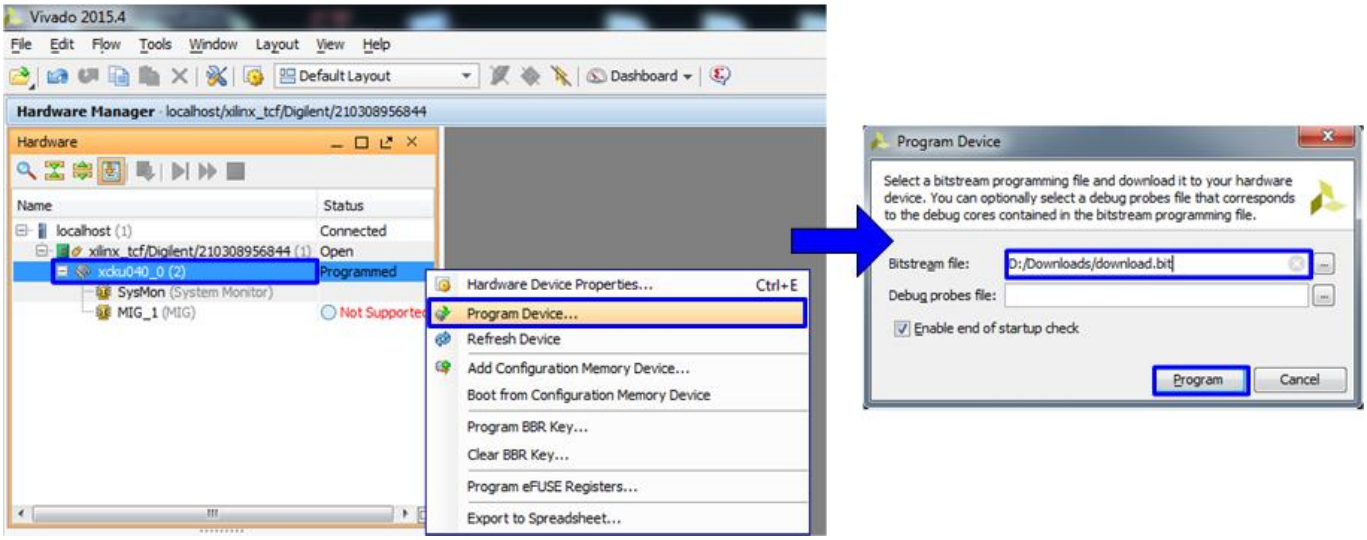

Figure 2-7 Download bit file from Vivado tool for other boards except ZC706

- After FPGA start operation, check (PL) GPIO LEDs status on FPGA board at LED0/L-LED1/C. Both LEDs must be ON, as shown in Figure 2-8 and Figure 2-9. LED2/R status depends on SATA speed status. Each LED description is described as follows.

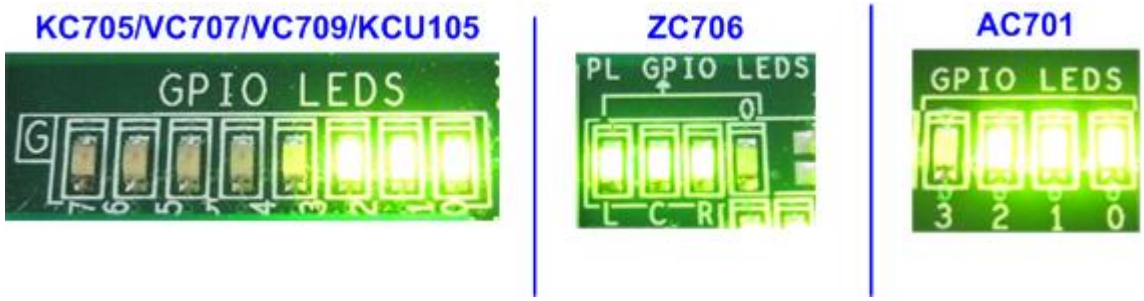

Figure 2-8 LED status after system set up complete on SATA-3 speed

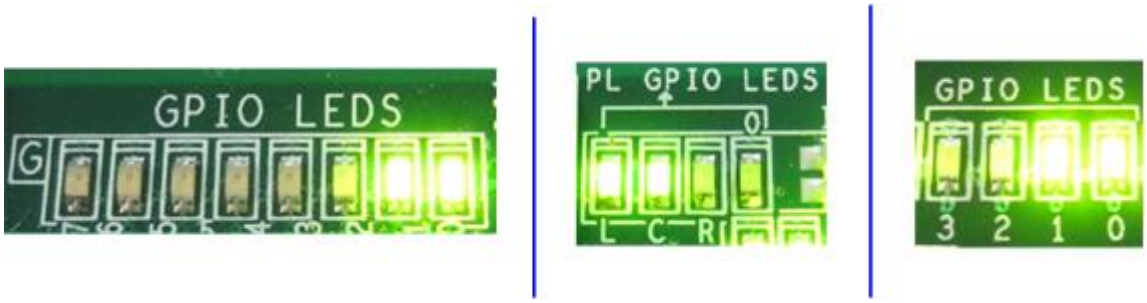

Figure 2-9 LED status after system set up complete on SATA-2 speed

LED	ON	OFF
LED0/L	OK	150 MHz of SATA clock on FMC SATA RAID cannot lock. Please check 150 MHz clock source on FMC SATA RAID board.
LED1/C	OK	SATA-IP cannot detect SATA device. Please check SATA device and the connection.
LED2/R	SATA-III	SATA-II (Not support on VC709 and KCU105)
LED3/0	Always OFF	

Table 2-2 LED Status of host reference design on FPGA board

- At serial console on PC, main menu will be displayed as shown in Figure 2-10. Then, user can execute each command operation. Please check serial-cable connection if this menu is not displayed on console.

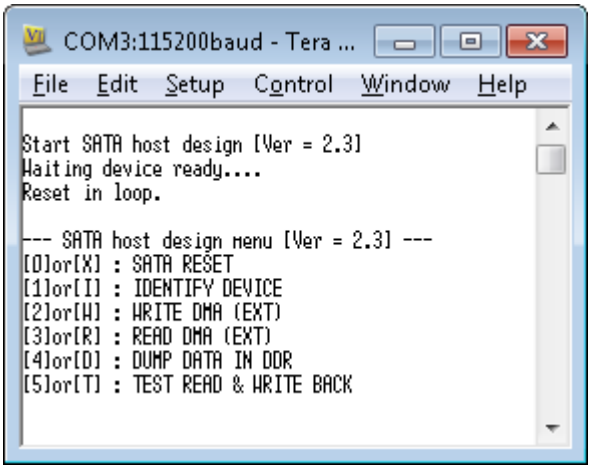

Figure 2-10 Main Menu of host demo

3 Main Menu

3.1 SATA RESET

Select '0' or 'X' for sending hardware reset signal to SATA-IP. Hardware reset is designed to reset both SATA-IP and SATA-PHY module. So, SATA initialize process will be started again and display "SATA RESET selected", as shown in Figure 3-1, after sending this reset.

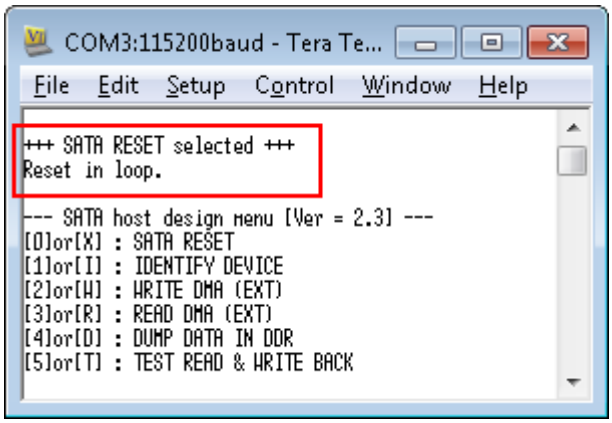

Figure 3-1 SATA Reset Output

3.2 IDENTIFY DEVICE

Select '1' or 'I' for sending "IDENTIFY DEVICE" command to HDD/SSD. Disk information (Model name, 48-bit LBA Supported, disk capacity) will be displayed by using this menu, as shown in Figure 3-2.

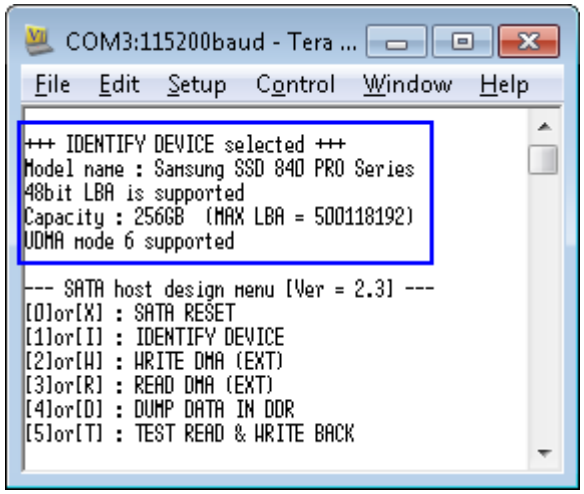

Figure 3-2 Disk Information from IDENTIFY DEVICE command

3.3 WRITE DMA (EXT)

Select '2' or 'W' for sending "WRITE DMA (EXT)" command to HDD/SSD. Three inputs are required for this menu, i.e.

- Start LBA: this value is the start sector number of HDD/SSD to write data.
- Sector Count: this value is the total transfer size in sector unit (512 byte) for writing HDD/SSD. This size is the data size for CPU to fill to write buffer. If the input is more than 65536 (maximum size for one SATA command), only 65536 sector data is filled and the later command will use same data area with the first command.
- Write Pattern: this value is used for selecting test pattern to write to buffer and then forward to HDD/SSD. There are six test patterns in this demo, i.e. 32-bit increment [0], 32-bit decrement [1], 00000000H [2], FFFFFFFFH [3], current data in read buffer [4], and LFSR counter [5].

After Software receives all inputs correctly,

- "Prepare data" will be displayed during CPU writing test pattern data to write buffer.
- "Execute Write" will be displayed during CPU sending WRITE DMA (EXT) command and transferring data from write buffer to HDD/SSD.
- Transfer speed will be displayed after write operation complete.

Figure 3-3 shows the example of test result when operation complete. Write operation will be cancelled from two cases, i.e. receiving error input or receiving any input from user during CPU processing this operation, as shown in Figure 3-4 and Figure 3-5 sequentially.

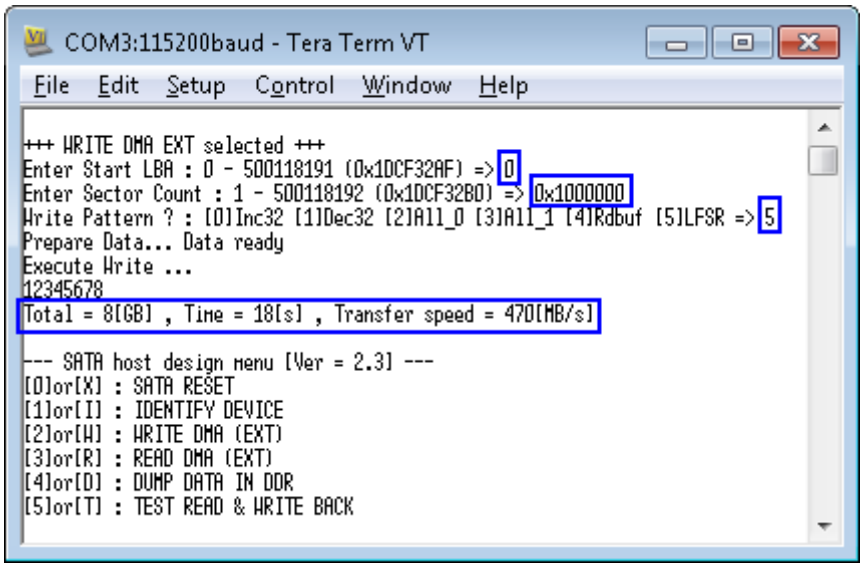

Figure 3-3 WRITE DMA (EXT) command input and output

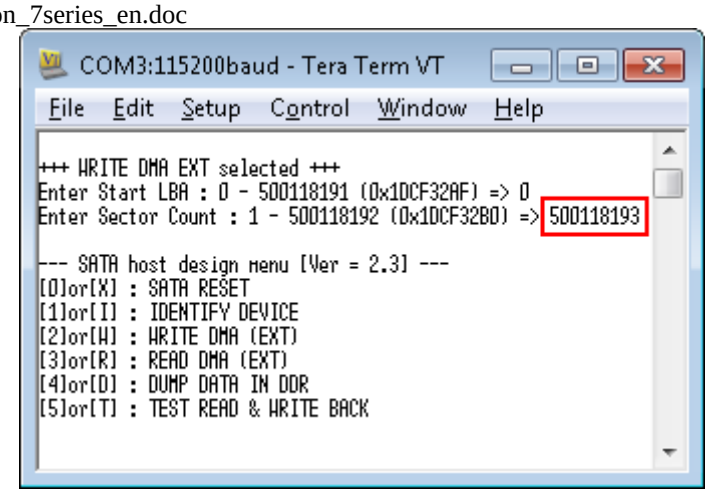

Figure 3-4 Write Operation cancelled from error input

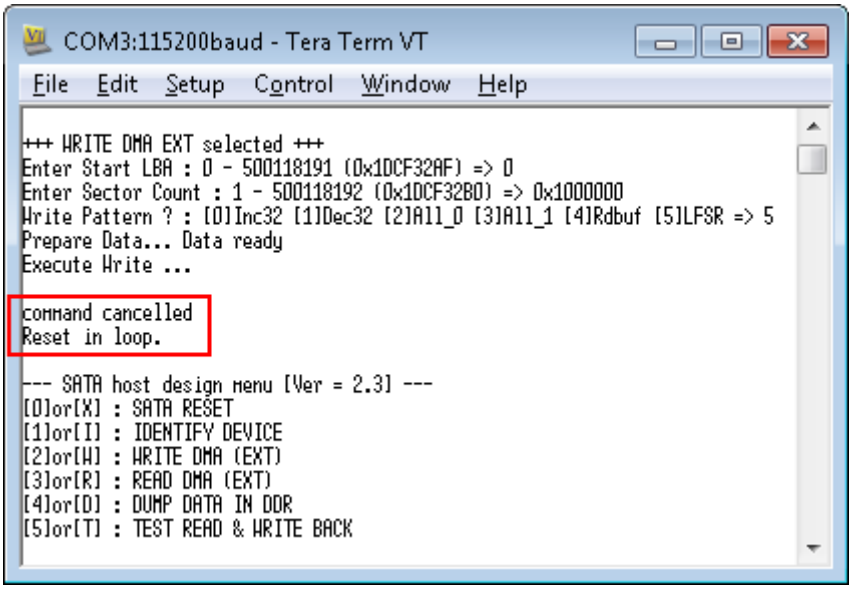

Figure 3-5 Write Operation cancelled from receiving input during operation

3.4 READ DMA (EXT)

Select '3' or 'R' for sending "READ DMA (EXT)" command to HDD/SSD. Two or three inputs are required for this menu, i.e.

- Start LBA: same description with Start LBA in WRITE DMA (EXT) menu.
- Sector Count: same description with Sector Count in WRITE DMA (EXT) menu. If this input is not more than 65536, the third input will be displayed for selecting verification pattern. If input is more than 65536, the third input will not be displayed to skip data verification process for checking performance only, as shown in Figure 3-6.
- Verify Pattern (Optional): this value is used for selecting verification pattern. This input should be matched with the pattern in WRITE DMA (EXT) menu. Six verification patterns can be selected, similar to write pattern. "Verify Data … Success" is displayed for success case, and "Data Mismatch with failure value" is displayed for failure case, as shown in Figure 3-7.

Similar to WRITE DMA (EXT) menu, Read operation will be cancelled if receiving error input or receiving any input from user during CPU processing, as shown in Figure 3-8 and Figure 3-9 sequentially.

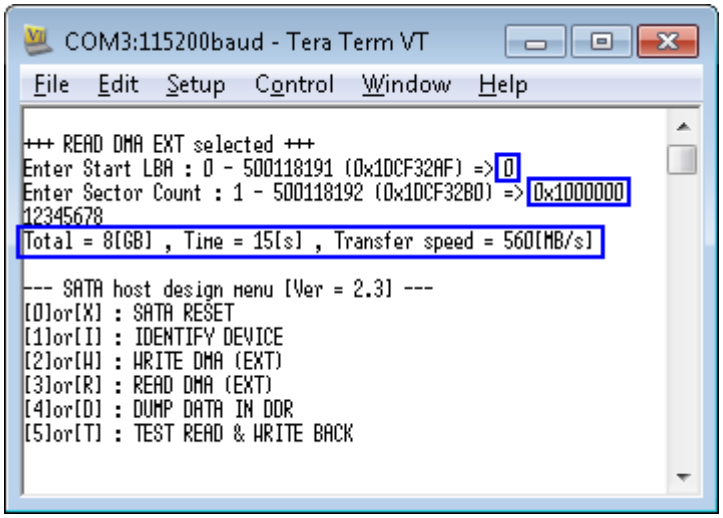

Figure 3-6 READ DMA (EXT) command without verify

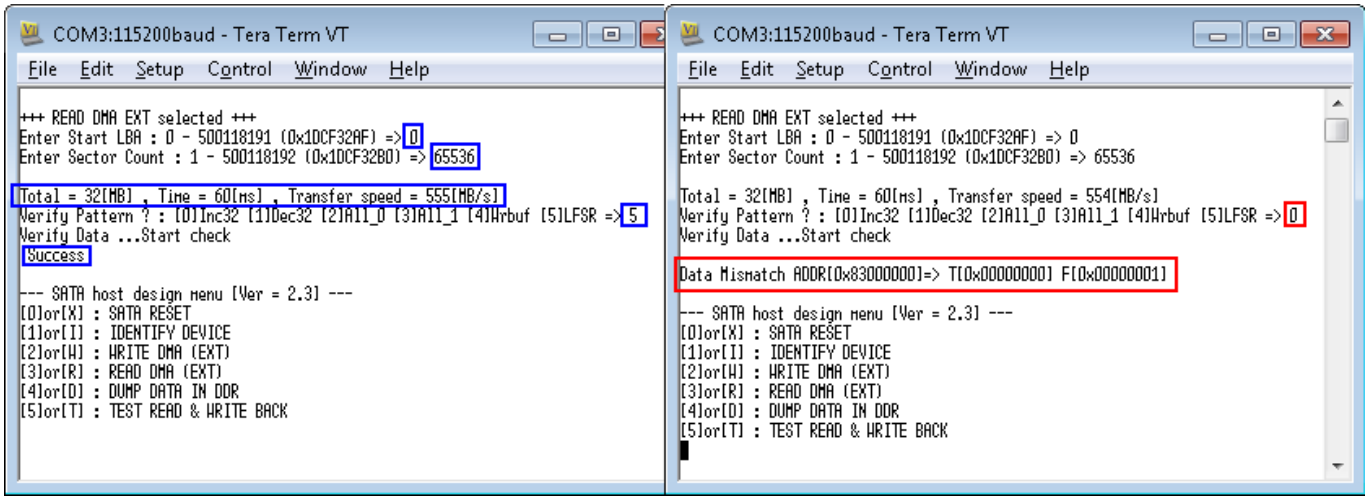

Figure 3-7 READ DMA (EXT) with verify process

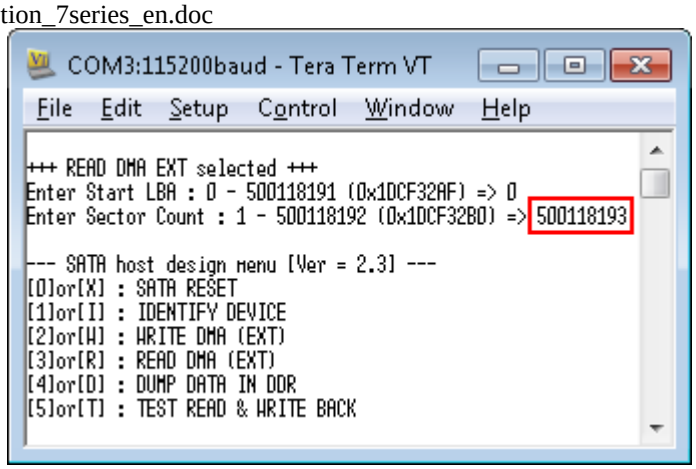

Figure 3-8 Read Operation cancelled from error input

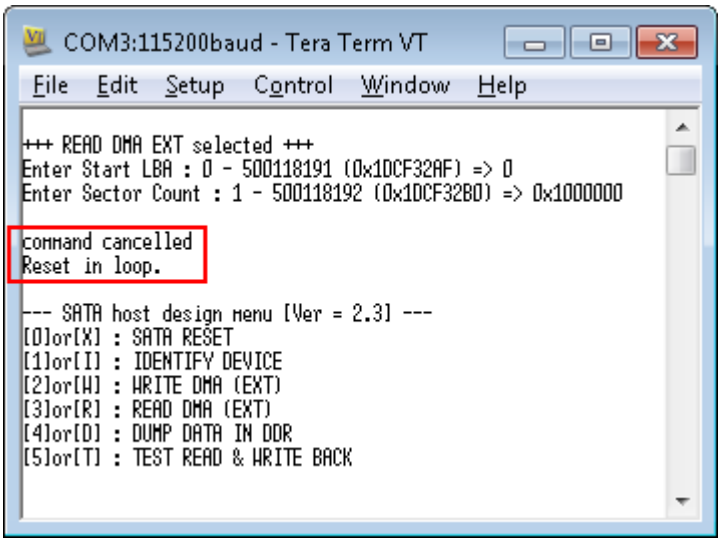

Figure 3-9 Read Operation cancelled from receiving input during operation

3.5 DUMP DATA IN DDR

Select '4' or 'D' to dump data from buffer to display on Serial Console. In this demo, DDR3/4 is mapped to address = 8000_0000h - BFFF_FFFFh (for all boards except KCU105) or 8000_0000h – FFFF_FFFFh (for KCU105). Six submenus can be selected, i.e.

- 'G': this submenu is used to select the address to read, as shown in Figure 3-10. The address can be input to be hex value by adding prefix "0x", so normally input will be received in decimal value.

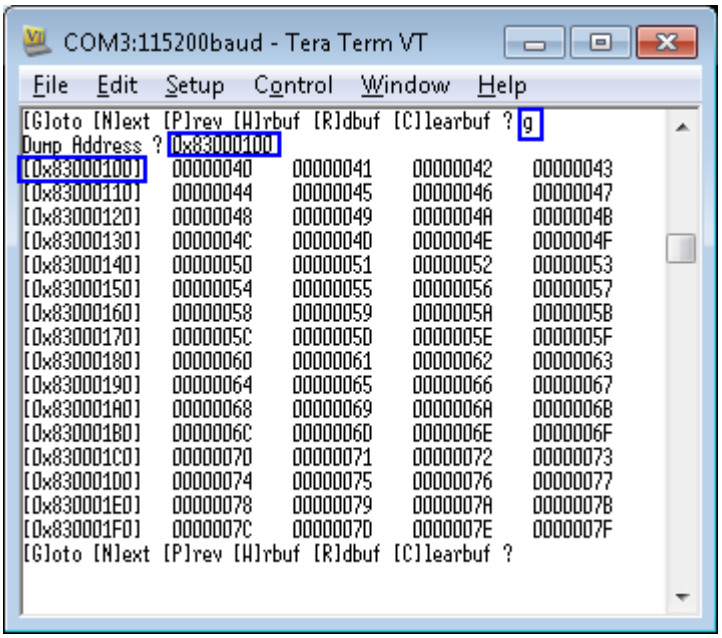

Figure 3-10 Goto submenu example

- 'N': this submenu is used to read next 256 byte data in buffer, as shown in Figure 3-11.
- 'P': this submenu is used to read previous 256 byte data in buffer, as shown in Figure 3-11.

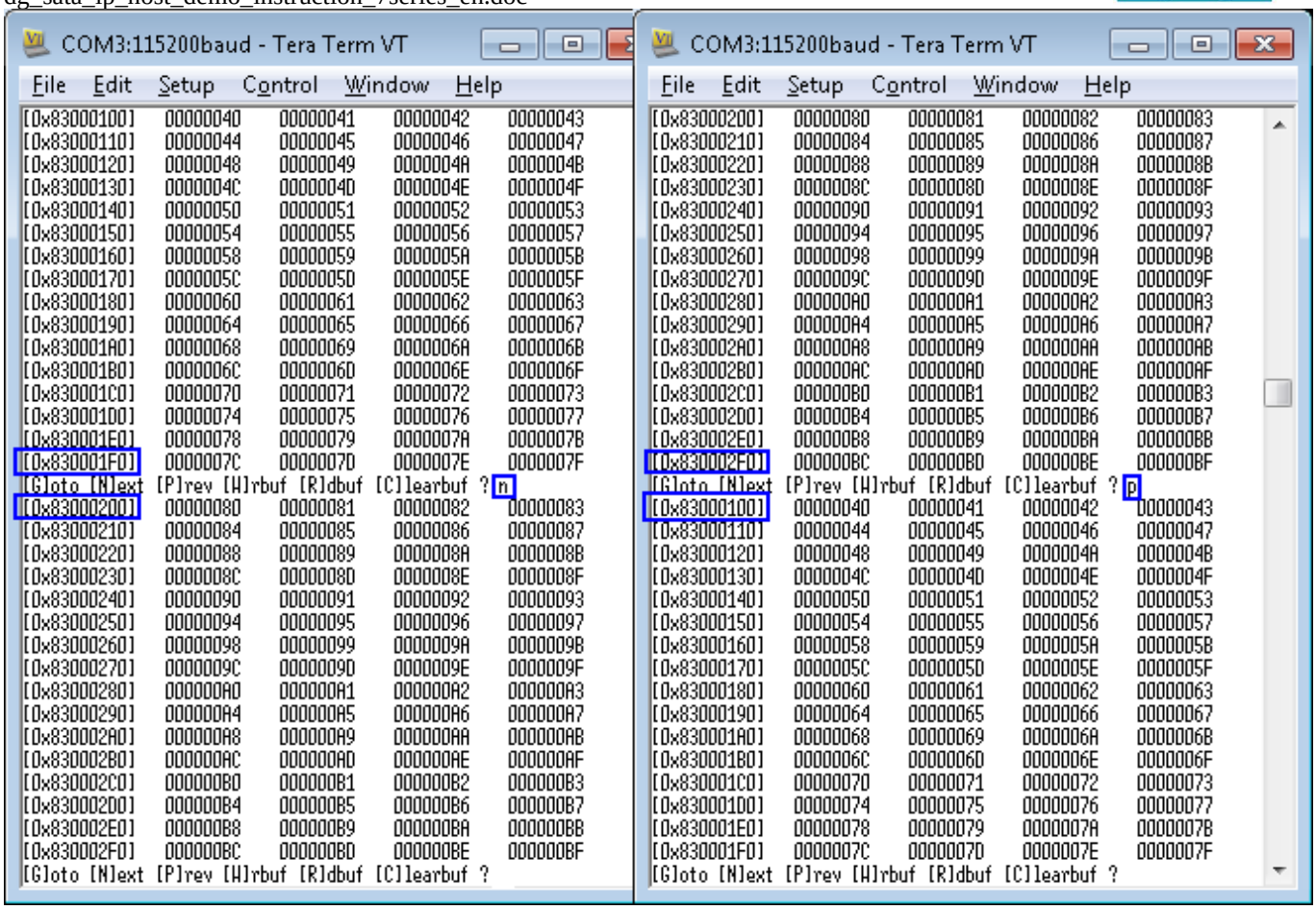

Figure 3-11 Read Next/Previous 256 byte data in buffer

- 'W': this submenu is used to read 256 byte data at top of write buffer, as shown in Figure 3-12.
- 'R': this submenu is used to read 256 byte data at top of read buffer, as shown in Figure 3-12.

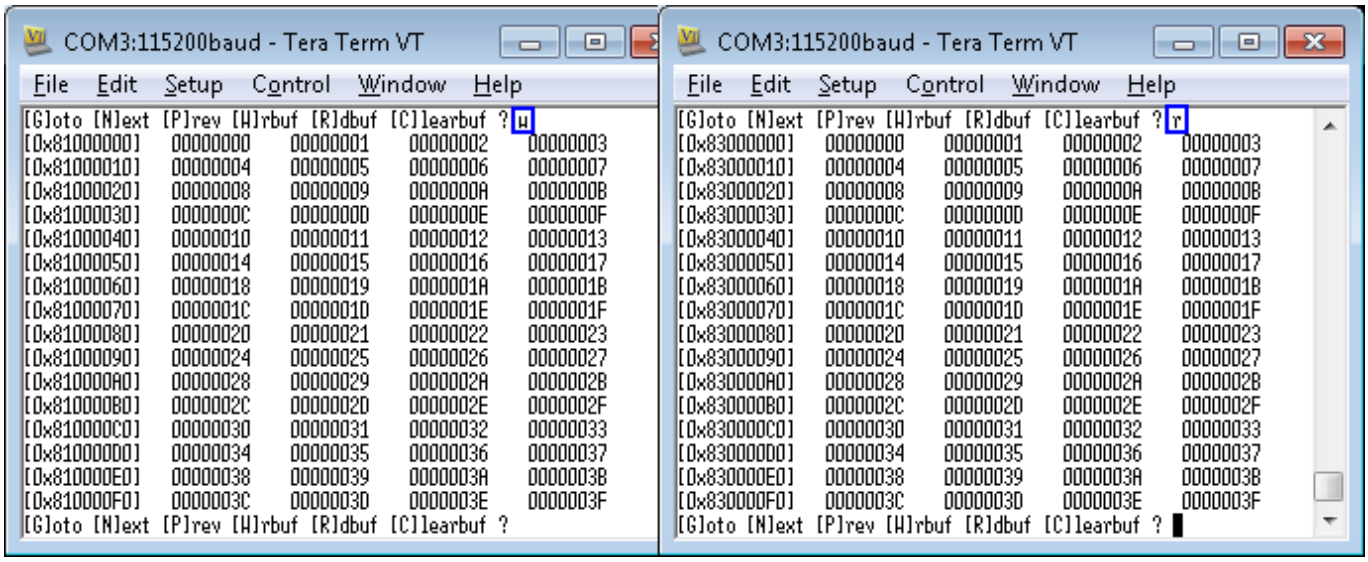

Figure 3-12 Read 256 byte data at top of write/read buffer

- 'C': this submenu is used to clear data in write/read buffer to be zero value. Select 'Y' to confirm for clear write/read buffer, but user can select 'N' to not clear the current buffer.

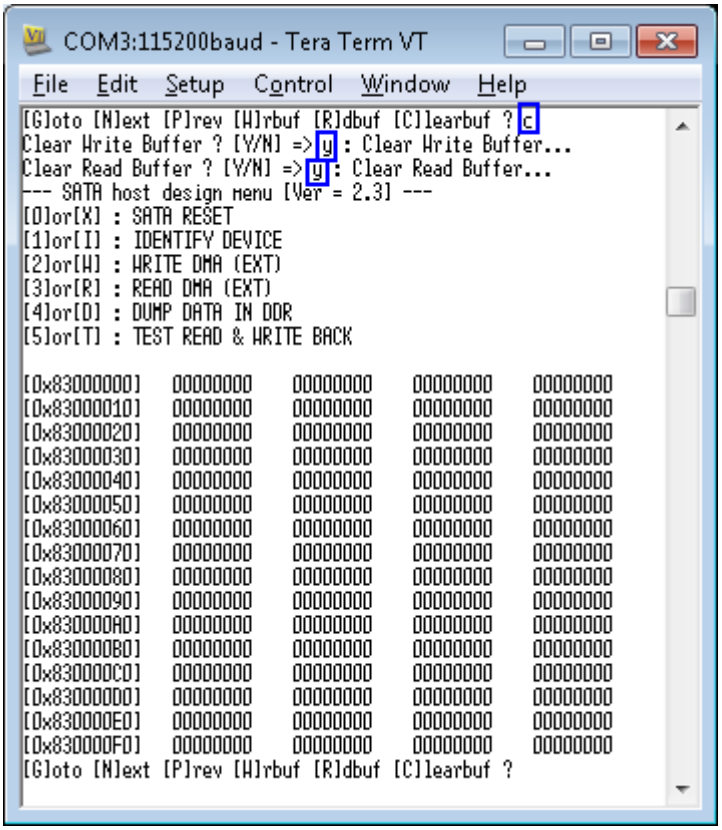

Figure 3-13 Clear buffer to be zero

User can exit this menu by input other key, such as 'x'.

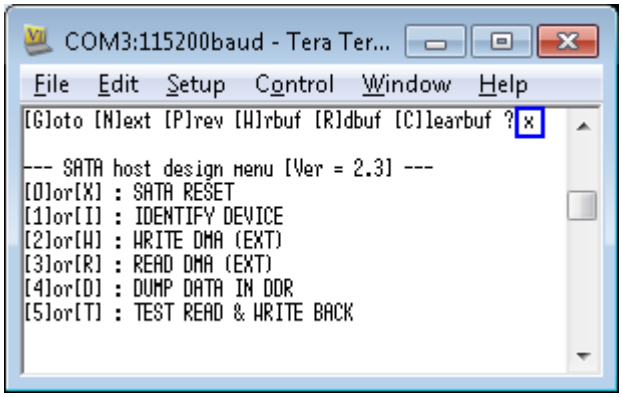

Figure 3-14 Exit dump menu

3.6 TEST READ & WRITE BACK

Select '5' or 'T' for test sending "WRITE DMA (EXT)" and "READ DMA (EXT)" without fill or verify test pattern. Write and Read speed will be displayed as output for this menu, as shown in Figure 3-15. Two inputs are required to use this menu, similar to "READ DMA (EXT).

The test operation will be cancelled if CPU receives any input from user during operation.

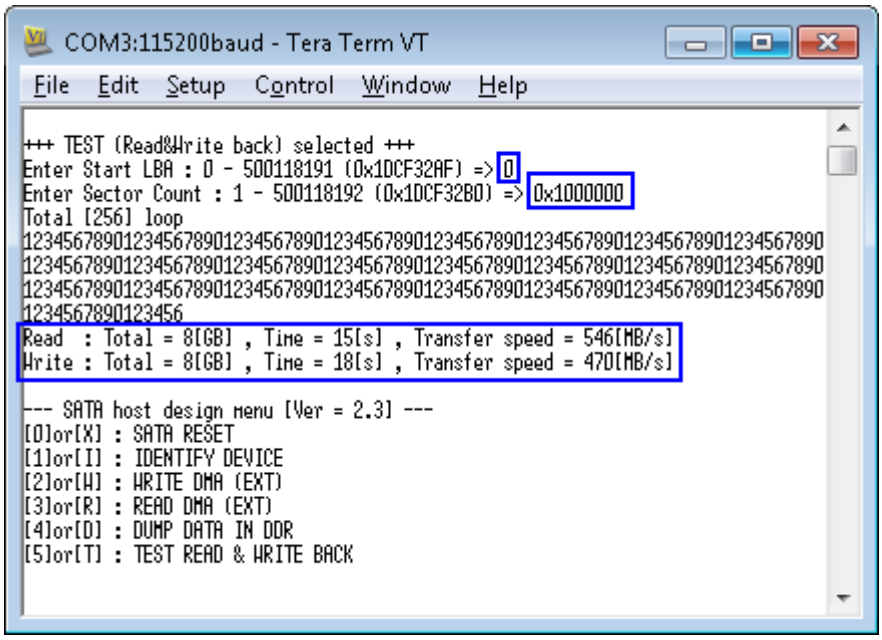

Figure 3-15 Test Menu Operation

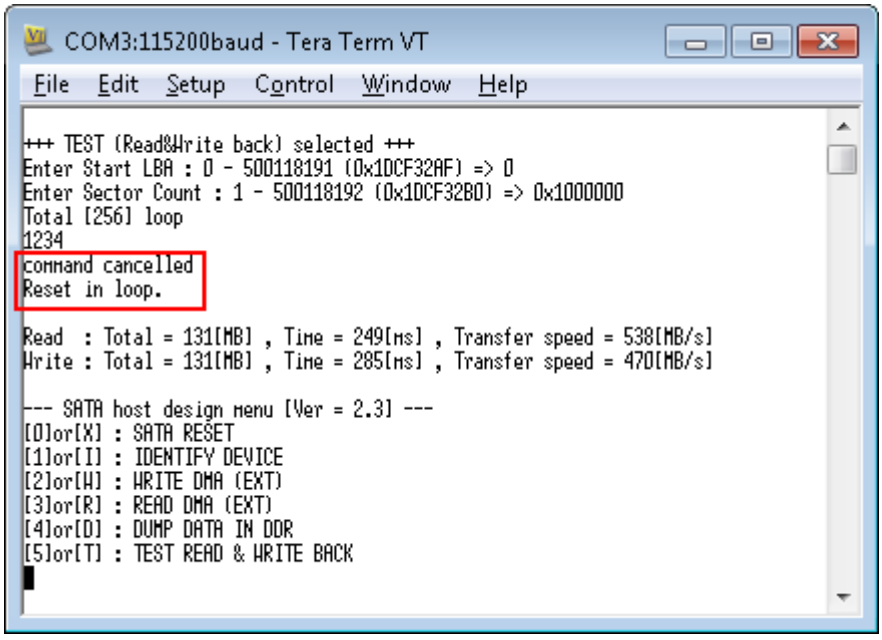

Figure 3-16 Test Operation cancelled

4 Revision History

Revision	Date	Description
1.0	21-Apr-14	Initial version release
2.0	21-Jan-16	Support 7-series and KCU105 board