SATA-IP RAIDx4 Demo Instruction on 7-Series and KCU105

Rev2.0 21-Jan-16

This document describes how to use SATA-IP RAIDx4 Demo reference design bit-file on KC705, ZC706, VC707, VC709, and KCU105 board. This design is RAID0 system connecting with 4 SATA-III HDD/SSDs to increase transfer speed in system to be 4 times of one SATA-III HDD/SSDs.

1 Environment

For real board evaluation of RAID reference design, environment setup is shown in Figure 1-1 - Figure 1-5.

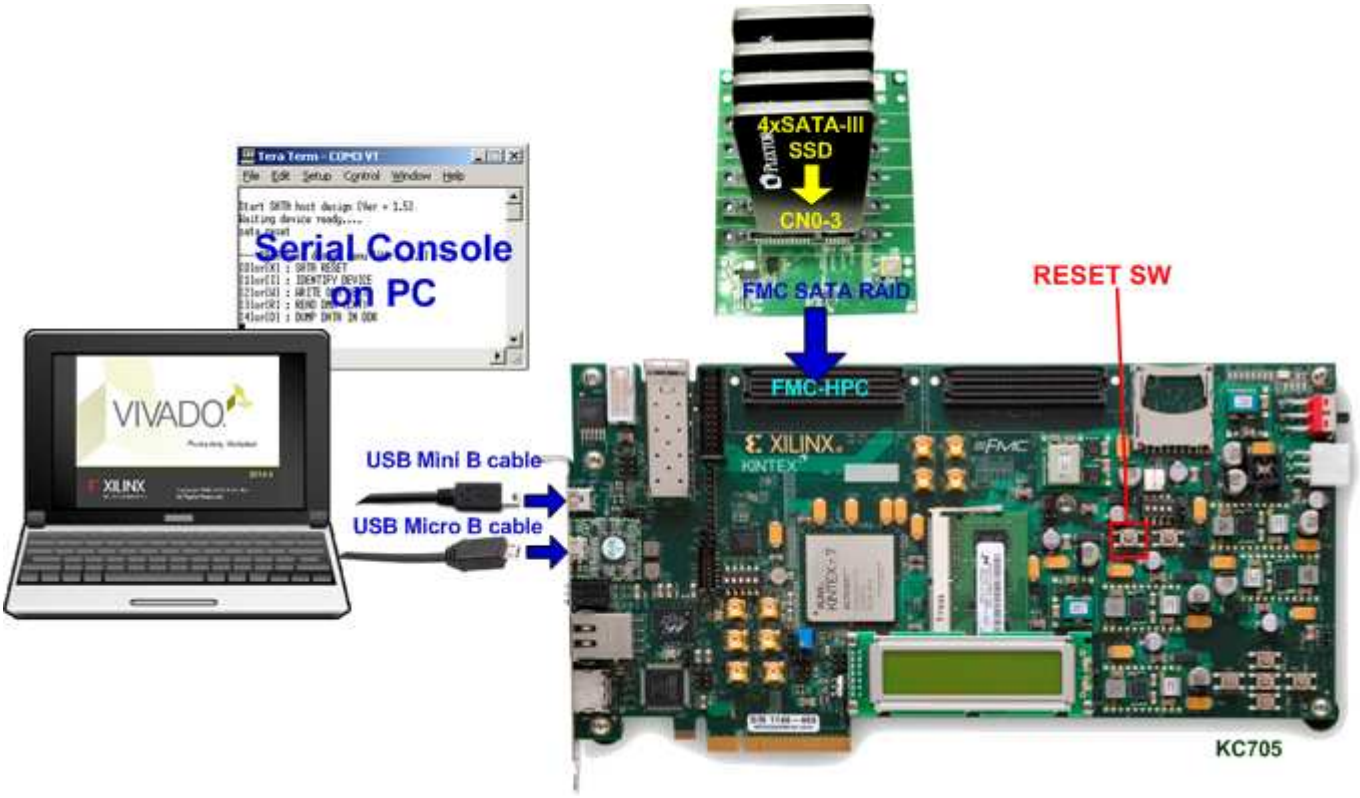

Figure 1-1 4-ch RAID0 demo environment on KC705

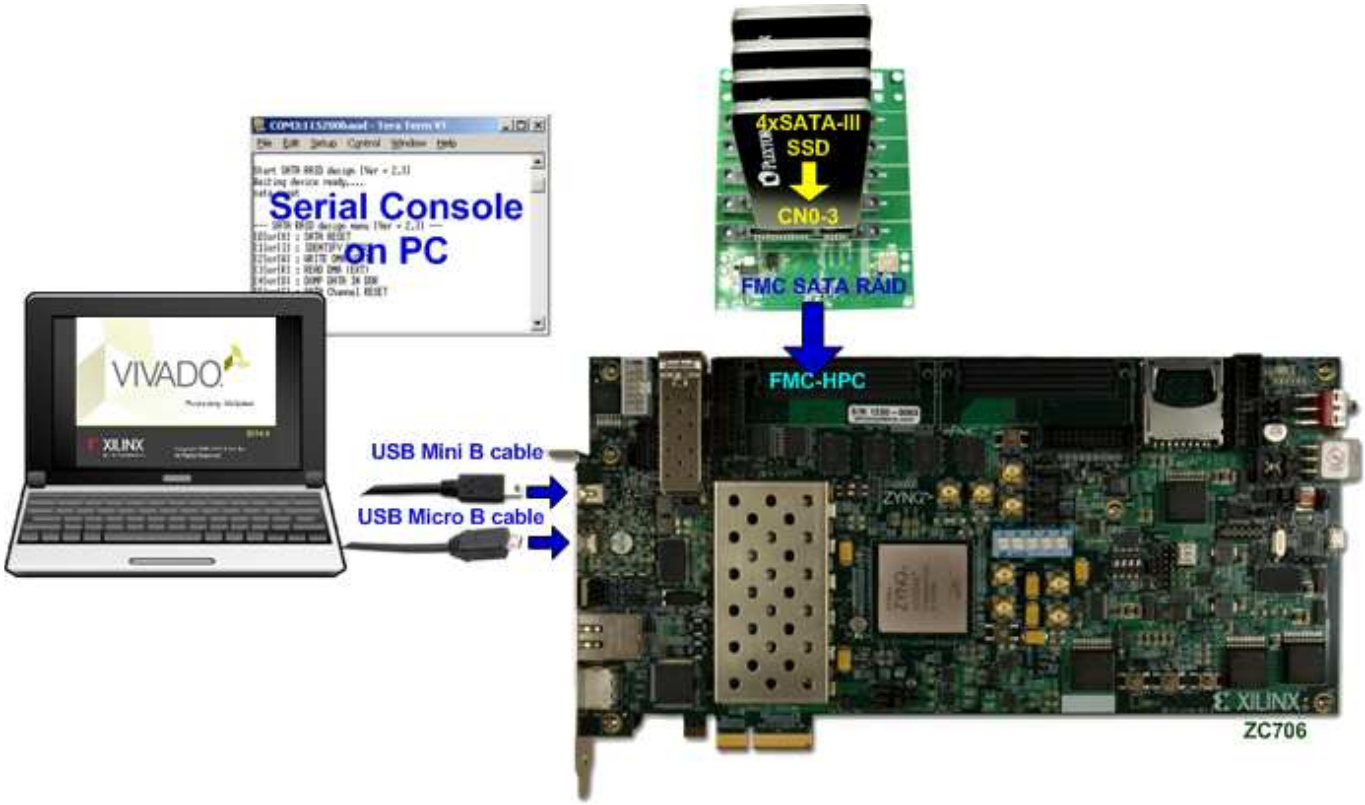

Figure 1-2 4-ch RAID0 demo environment on ZC706

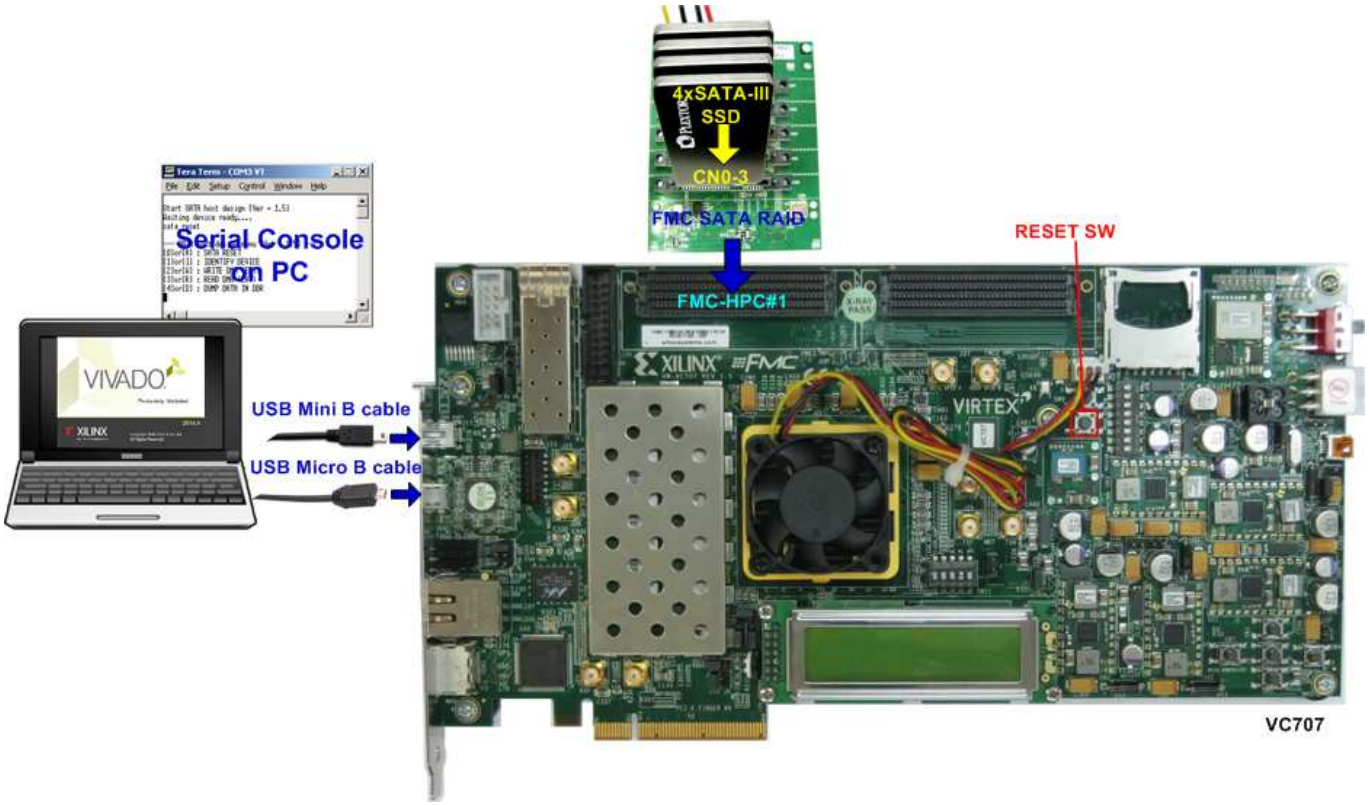

Figure 1-3 4-ch RAID0 demo environment on VC707

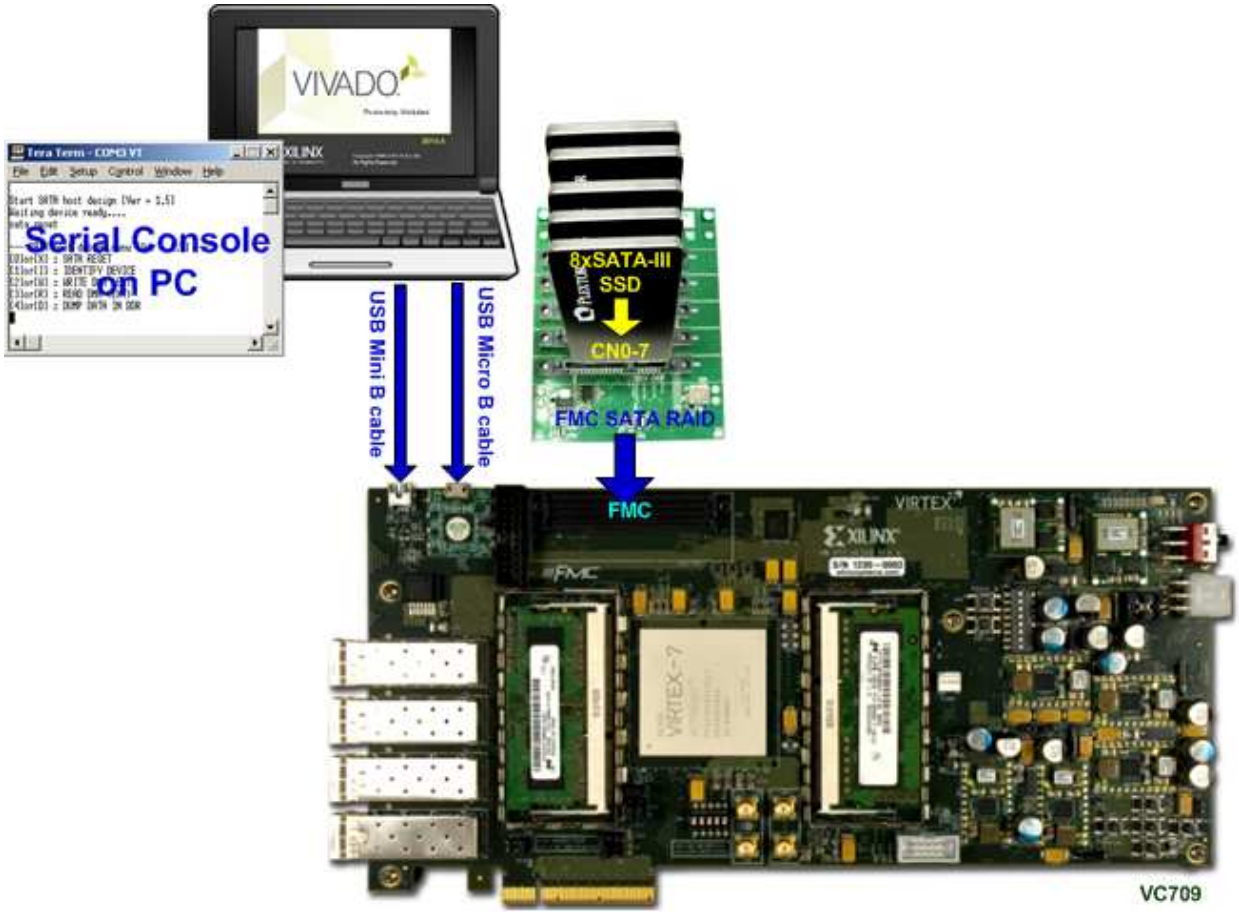

Figure 1-4 4-ch RAID0 demo environment on VC709

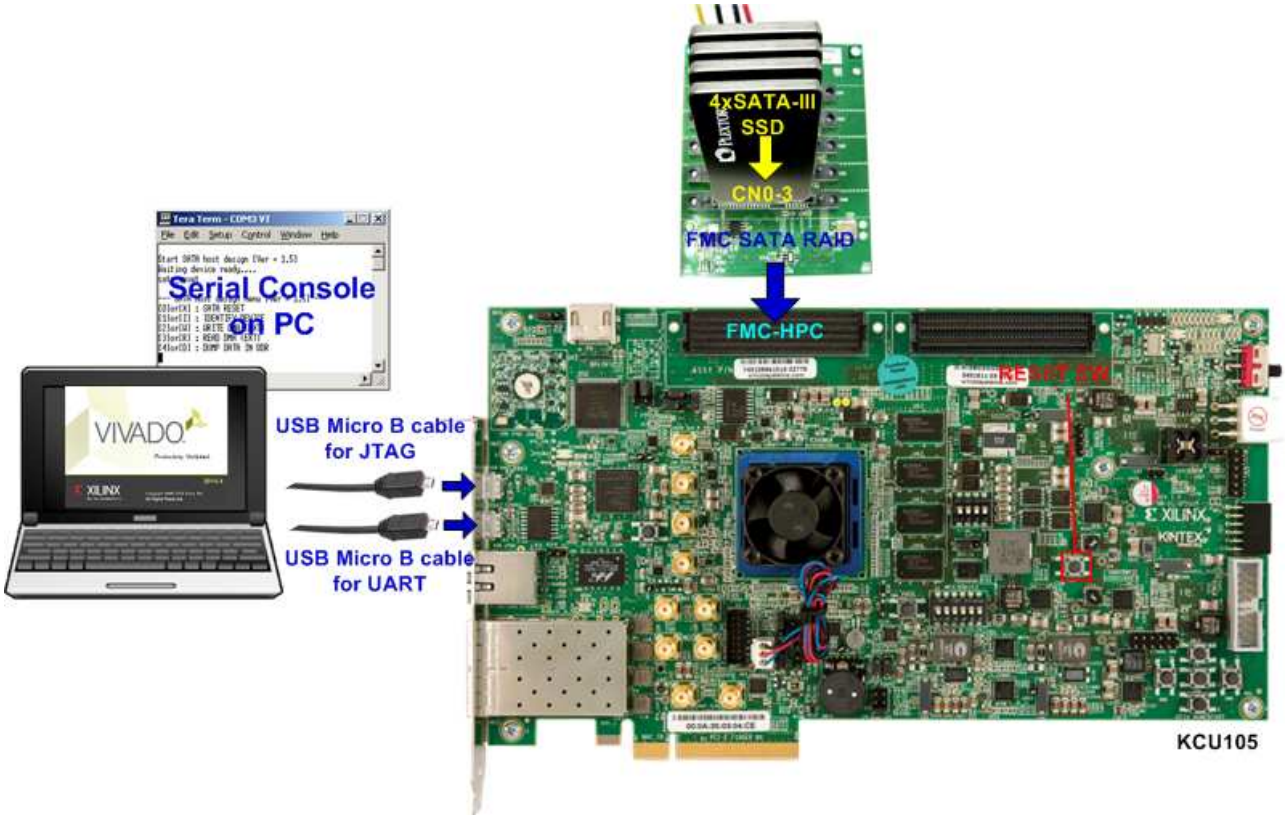

Figure 1-5 4-ch RAID0 demo environment on KCU105

2 Evaluation procedure

- Check that system is power off.
- Connect FMC SATA RAID board to FMC-HPC(#1) connector.
  Note: FMC SATA RAID board is provided by Design Gateway.
- Connect power to power connector on FMC SATA RAID board.
- Connect 4 SATA-III Device to CN0-CN3 on FMC SATA RAID board.
- Connect USB mini/micro B cable from USB UART Port on FPGA board to PC for Serial Console. KCU105 uses micro B cable while others use mini B cable.
- Connect USB micro B cable from Digilent on FPGA board to PC for JTAG programming.

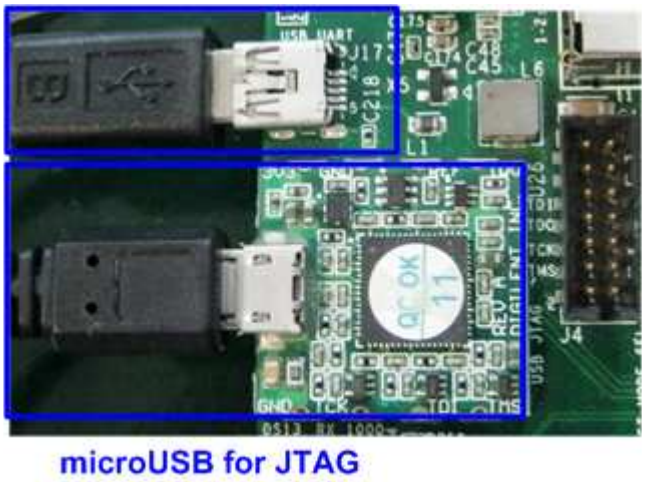

Figure 2-1 mini and micro USB cable connection for KC705/ZC706/VC707/VC709

Figure 2-2 two micro USB cable connections on KCU105

- Connect Power cable to FPGA board and then power up.
- Open serial monitoring software such as HyperTerminal. Terminal settings are Baud Rate=115200, Data=8 bit, Non-Parity, and Stop=1.

- Download bit-file to FPGA board.
  - For ZC706 board, please follow below steps.
  1) Copy “ready_for_download” folder to PC.
  2) Open “ISE Design Suite Command Prompt” and change working directory to “ready_for_download” folder.

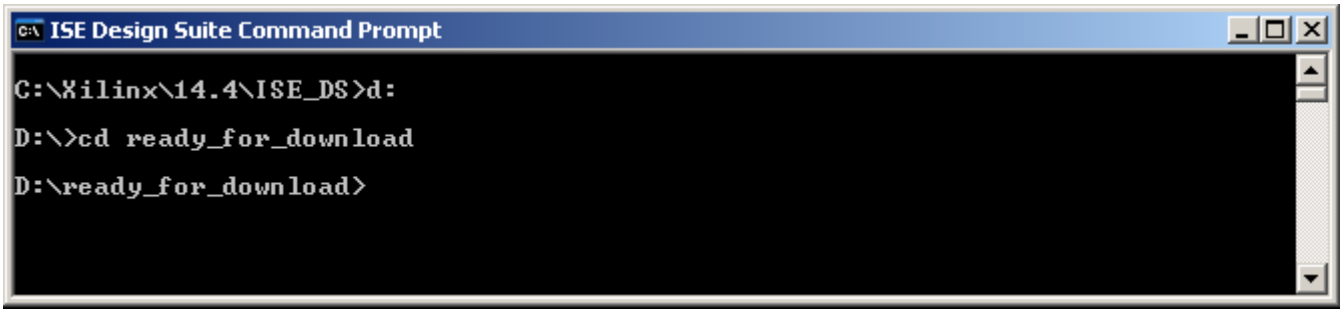

Figure 2-3 ISE Design Suite Command Prompt for ZC706 board

3) Type “zc706_bist.bat” to start downloading configuration file and the firmware. On the console, “Download 10 … Done” is displayed after both bit file and firmware file are loaded complete. Then, user can exit this menu and see LED status and Serial console.

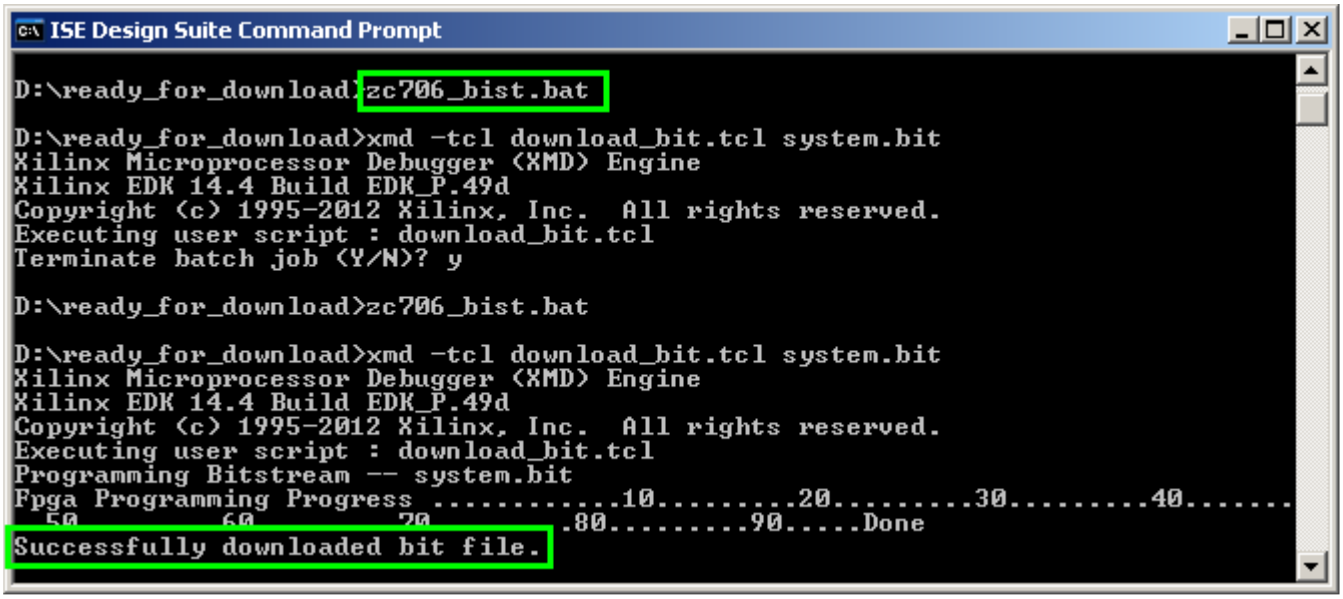

Figure 2-4 Downloading configuration file for ZC706 board

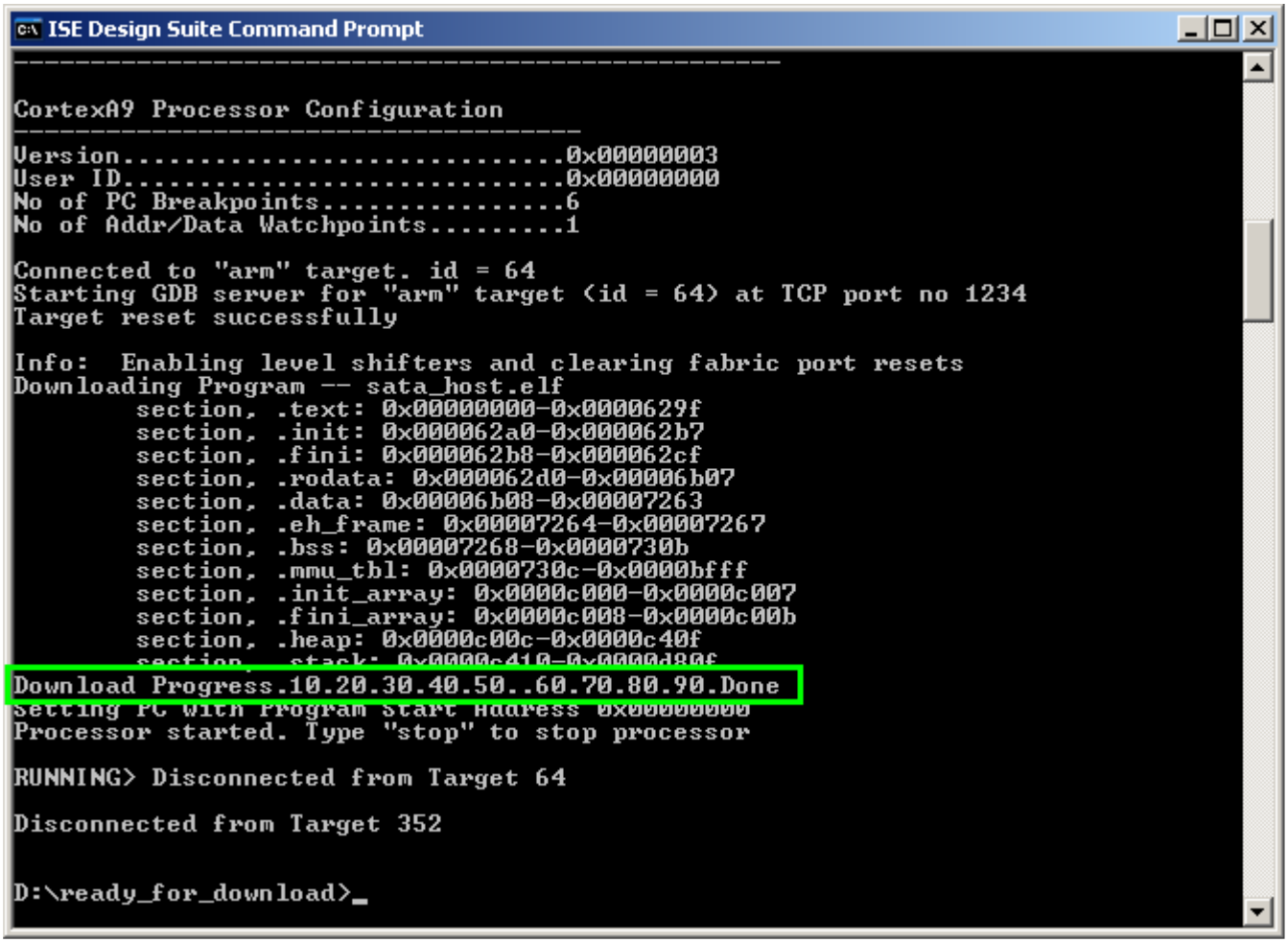

Figure 2-5 End of Downloading Firmware for ZC706 board

- For other boards, bit file can be downloaded from Vivado or iMPACT tool.

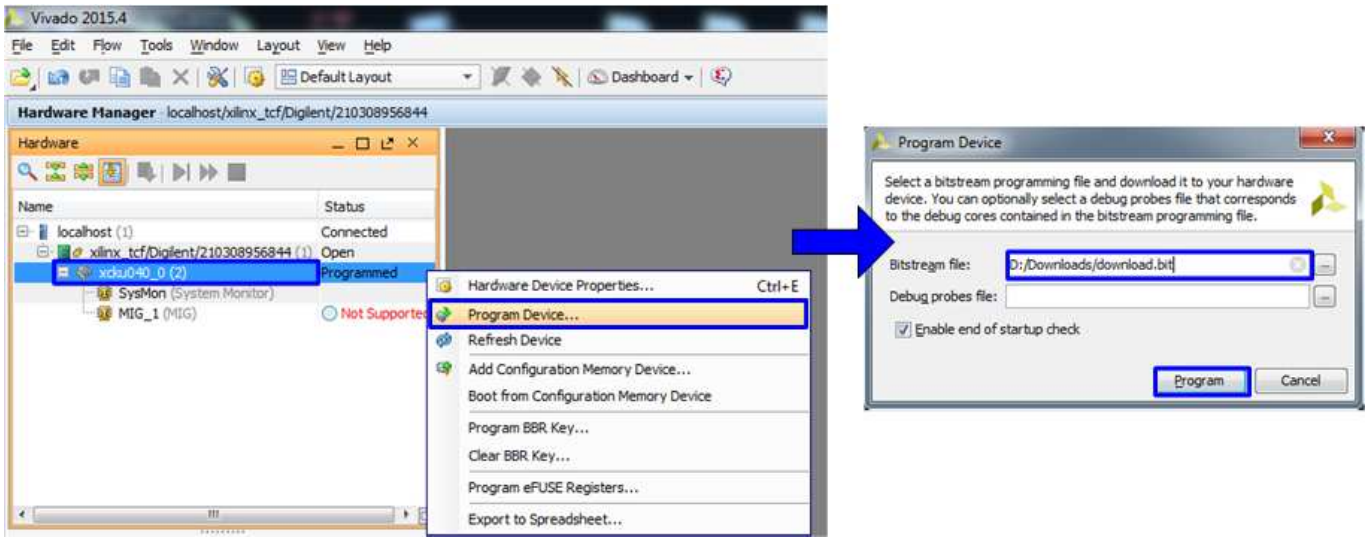

Figure 2-6 Download bit file from Vivado tool for other boards except ZC706

- After FPGA start operation, check GPIO LEDs status on FPGA board at LED0-LED7 (For ZC706, check LEDL-LED0). All LEDs must be ON, as shown in Figure 2-7. Each LED description is described as follows.

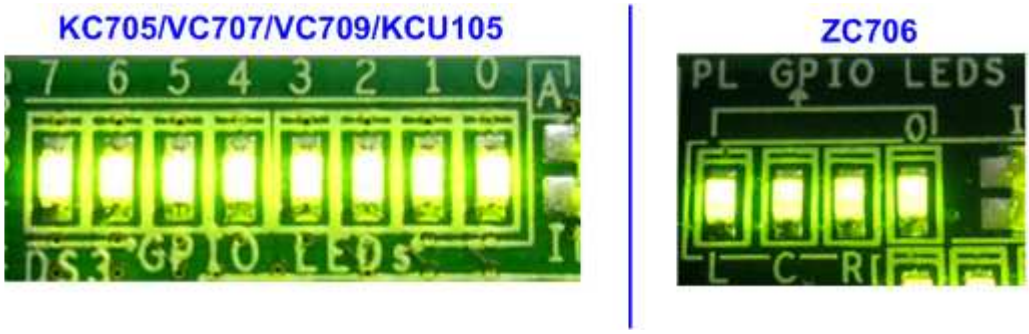

Figure 2-7 LED status after system set up complete on FPGA board

LED	ON	OFF
LED0/L	OK	150 MHz of SATA clock on FMC SATA RAID cannot lock. Please check 150 MHz clock source on FMC SATA RAID board.
LED1/C	OK	SATA-IP cannot detect SATA device. Please check SATA device at CN#0 and the connection.
LED2/R	Same description to LED0/L.	
LED3/0	Same description to LED1/C, but check SATA device at CN#1.	
LED4	Same description to LED0/L.	
LED5	Same description to LED1/C, but check SATA device at CN#2.	
LED6	Same description to LED0/L.	
LED7	Same description to LED1/C, but check SATA device at CN#3.	

Table 2-1 LED Status of RAID reference design

- The serial console on PC will display main menu, as shown in Figure 2-8, if all four SATA devices can initialize successfully. Then, user can execute each command operation following the menu.
- If any disk cannot link up and initialize, error message will be displayed to report error disk number, as shown in Figure 2-9. The disk number can be referred to CN number directly. For example, Disk1 means SATA device at CN#1.

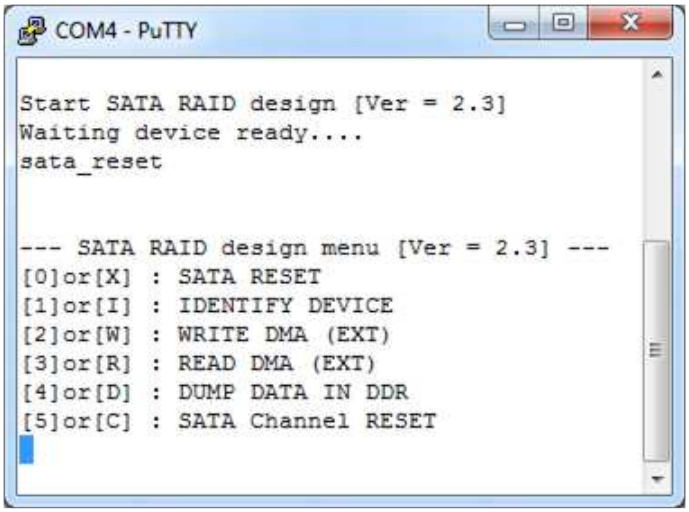

Figure 2-8 Main Menu of host demo

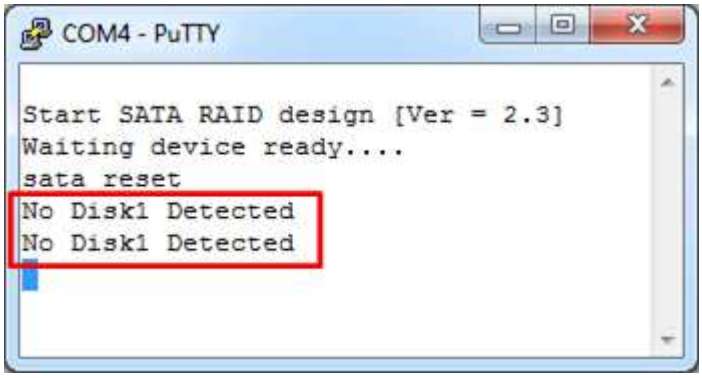

Figure 2-9 The error message when disk number#1 has problem

3 Main Menu

3.1 SATA RESET

Select '0' or 'X' for sending hardware reset signal to all four SATA-IPs. Hardware reset is designed to reset both SATA-IP and SATA-PHY module in every SATA channel. So, SATA initialize process will restart again and display "SATA RESET selected", as shown in Figure 3-1, after sending this reset.

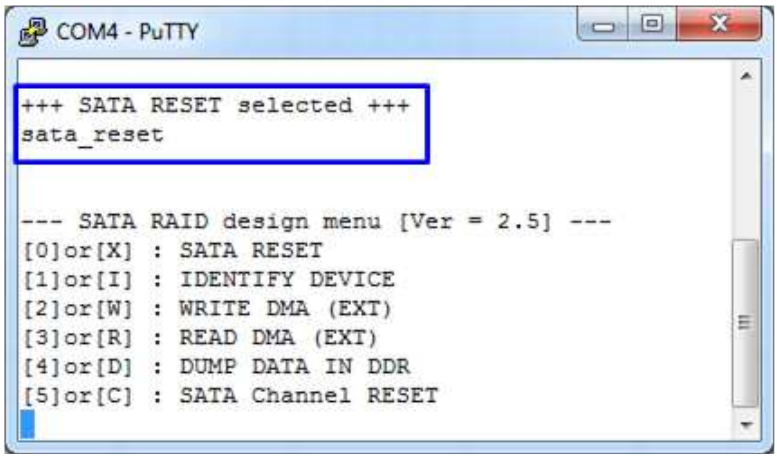

Figure 3-1 SATA Reset Output

3.2 IDENTIFY DEVICE

Select '1' or 'I' for sending "IDENTIFY DEVICE" command to HDD/SSD. Disk information (Model name, 48-bit LBA supported, disk capacity) of all four channels will be displayed by using this menu, as shown in Figure 3-2. From this command, maximum LBA size will be calculated from disk which has minimum size x 4.

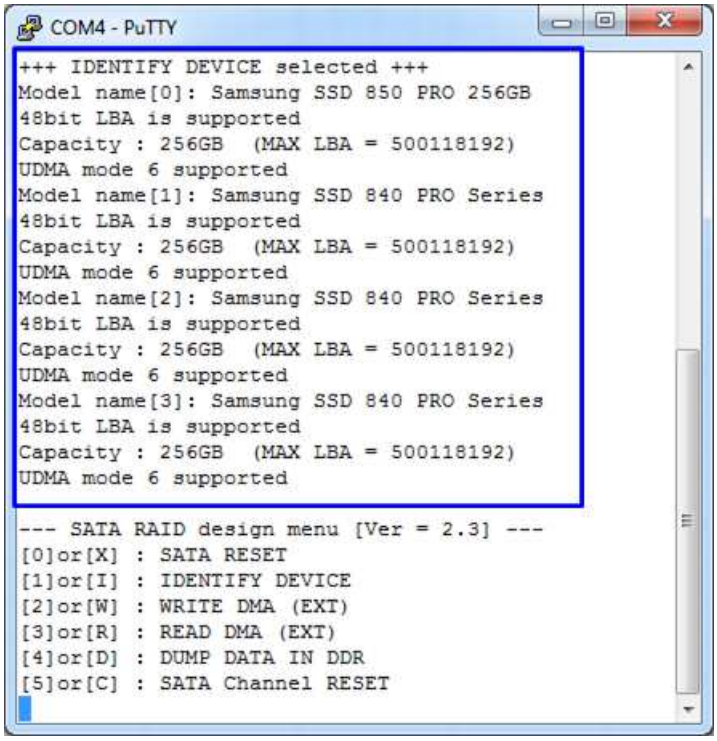

Figure 3-2 Disk Information from IDENTIFY DEVICE command

3.3 WRITE DMA (EXT)

Select '2' or 'W' for sending "WRITE DMA (EXT)" command to HDD/SSD. Three inputs are required for this menu, i.e.

- Start LBA: this value, divided by 4, is the start sector number of each HDD/SSD to write data.
- Sector Count: this value, divided by 4, is the total transfer size in sector unit (512 byte) for writing each HDD/SSD. This size is the data size for CPU to fill to write buffer. If the input is more than 262144 (4 x maximum size of one SATA command), only 262144 sector data is filled and the later command will use same data area with the first command.
- Write Pattern: this value is used for selecting test pattern to write to buffer which will be forwarded to HDD/SSD. There are six test patterns in this demo, i.e. 32-bit increment [0], 32-bit decrement [1], 00000000H [2], FFFFFFFFH [3], current data in read buffer [4], and LFSR counter [5].

After Software receives all inputs correctly,
- "Prepare data" will be displayed during CPU writing test pattern data to write buffer.
- "Execute Write" will be displayed during CPU sending WRITE DMA (EXT) command and transferring data from write buffer to HDD/SSD.
- Transfer speed will be displayed after write operation complete.

Figure 3-3 shows two examples of write command with different transfer size. Bigger transfer size can show higher performance speed.

Write operation is cancelled by two cases, i.e. receiving error input or receiving input from keyboard during CPU processing, as shown in Figure 3-4 and Figure 3-5 sequentially.

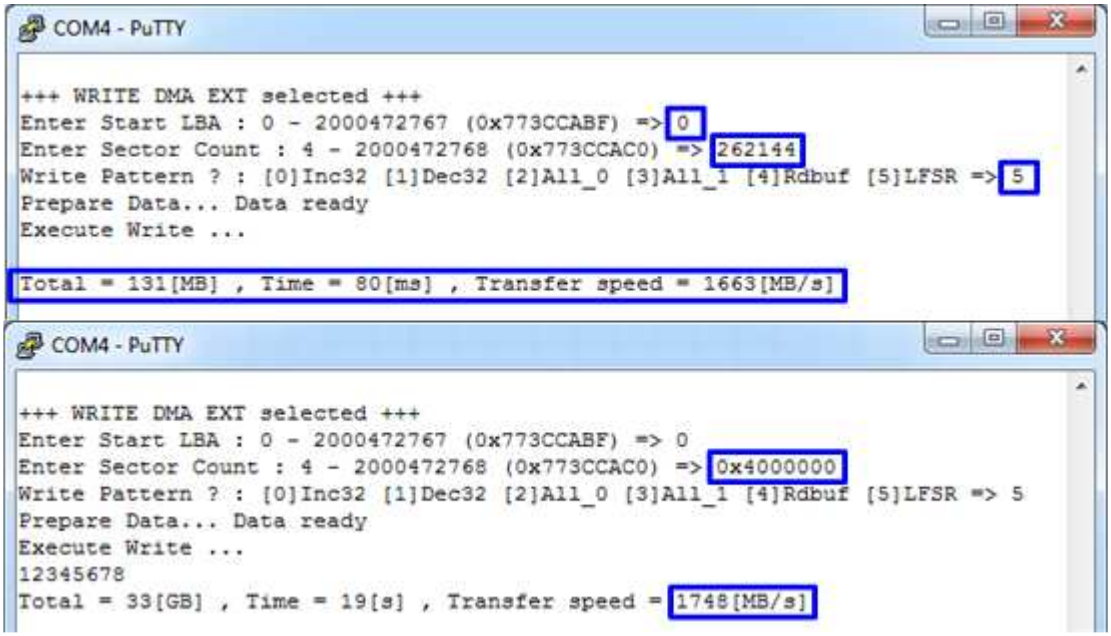

Figure 3-3 WRITE DMA (EXT) command input and output

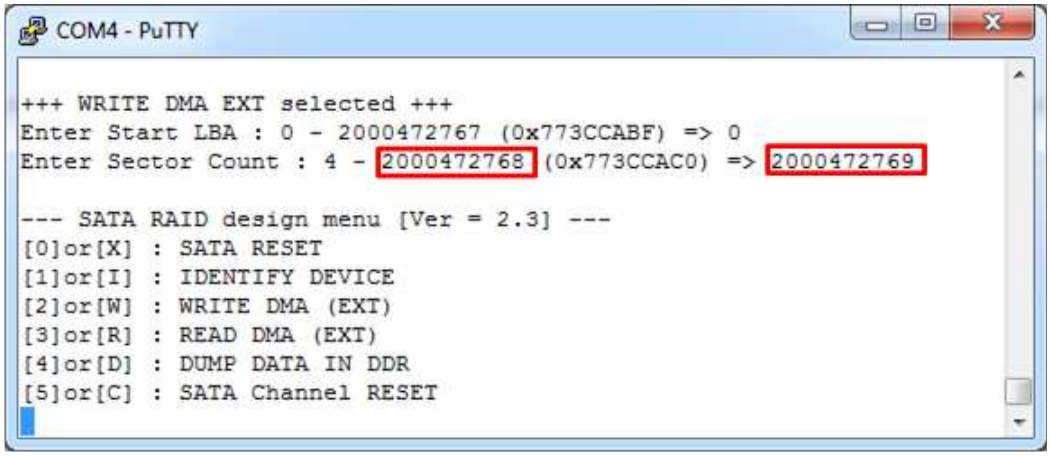

Figure 3-4 Write Operation cancelled from error input

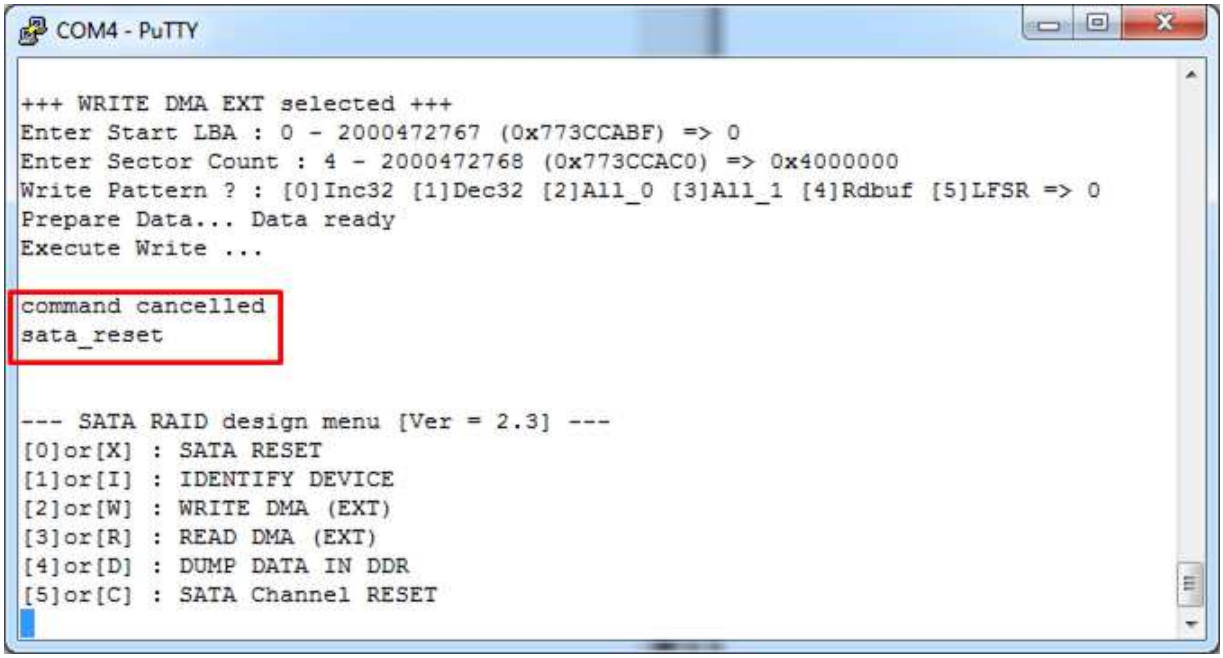

Figure 3-5 Write Operation cancelled from receiving input during operation

3.4 READ DMA (EXT)

Select '3' or 'R' for sending "READ DMA (EXT)" command to HDD/SSD. Two or three inputs are required for this menu, i.e.

- Start LBA: same description with Start LBA in WRITE DMA (EXT) menu, but this is for read operation.
- Sector Count: same description with Sector Count in WRITE DMA (EXT) menu. If this input is not more than 262144, the third input will be displayed for selecting verification pattern. If input is more than 262144, the third input will not be displayed to skip data verification process for checking performance only, as shown in Figure 3-6.
- Verify Pattern (Optional): this value is used for selecting verification pattern. This input should be matched with the pattern in WRITE DMA (EXT) menu. Six verification patterns can be selected, similar to write pattern. "Verify Data … Success" is displayed for success case, and "Data Mismatch with failure value" is displayed for failure case, as shown in Figure 3-7.

Similar to WRITE DMA (EXT) menu, Read operation can be cancelled by receiving error input or receiving input from keyboard during CPU processing, as shown in Figure 3-8 and Figure 3-9 sequentially.

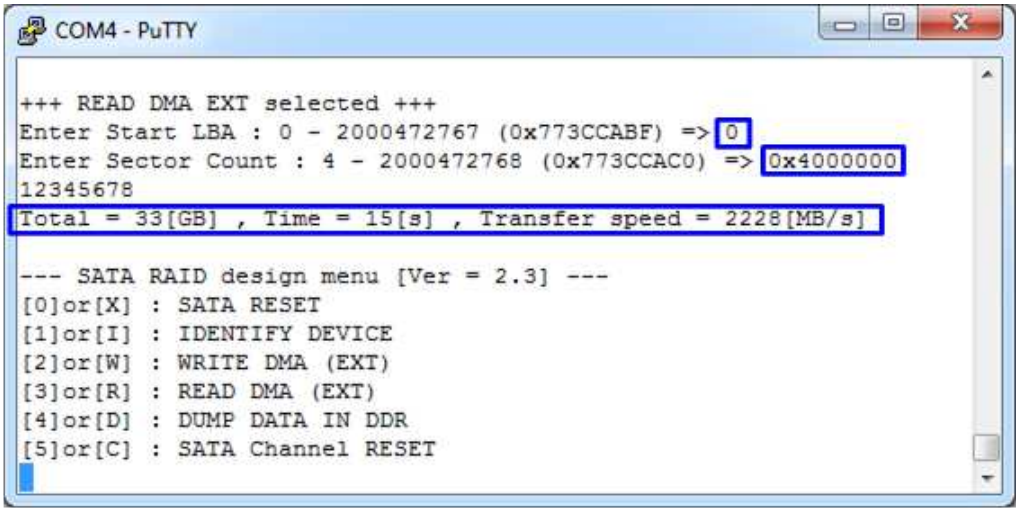

Figure 3-6 READ DMA (EXT) command without verify

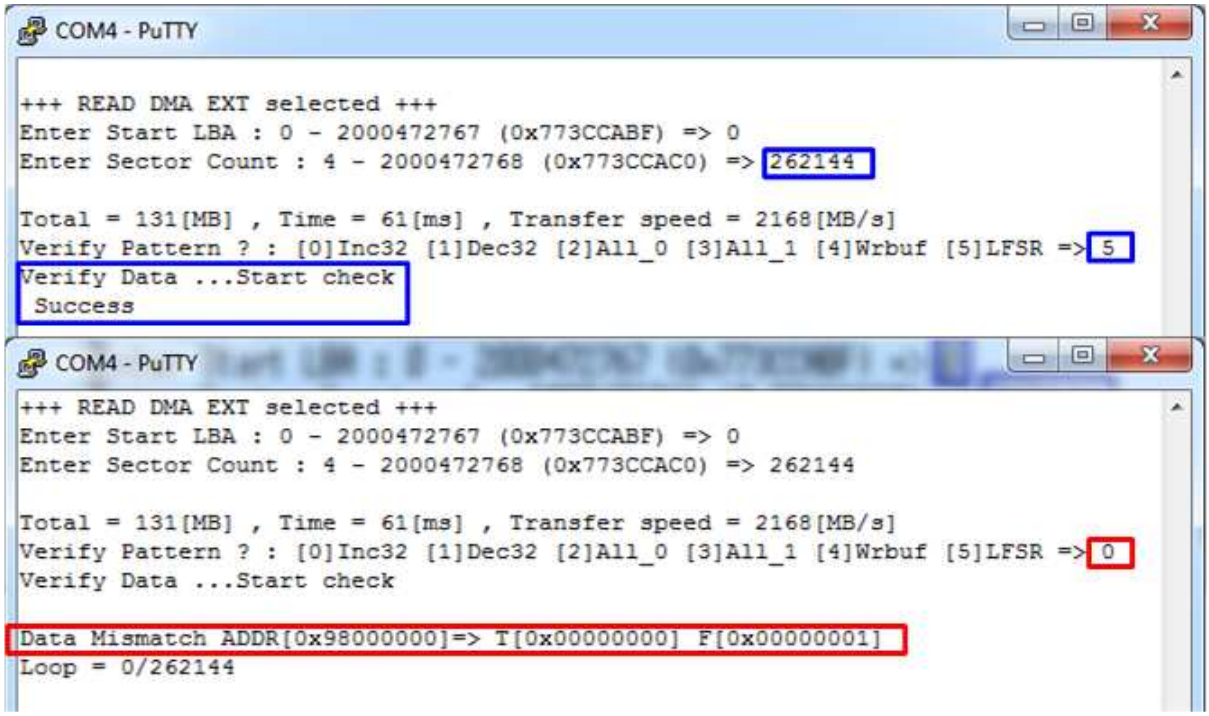

Figure 3-7 READ DMA (EXT) with verification process

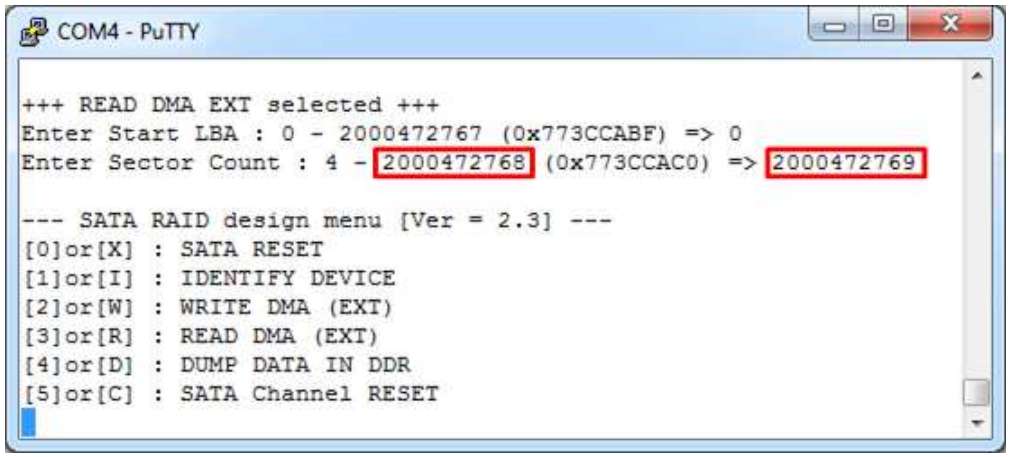

Figure 3-8 Read Operation cancelled from error input

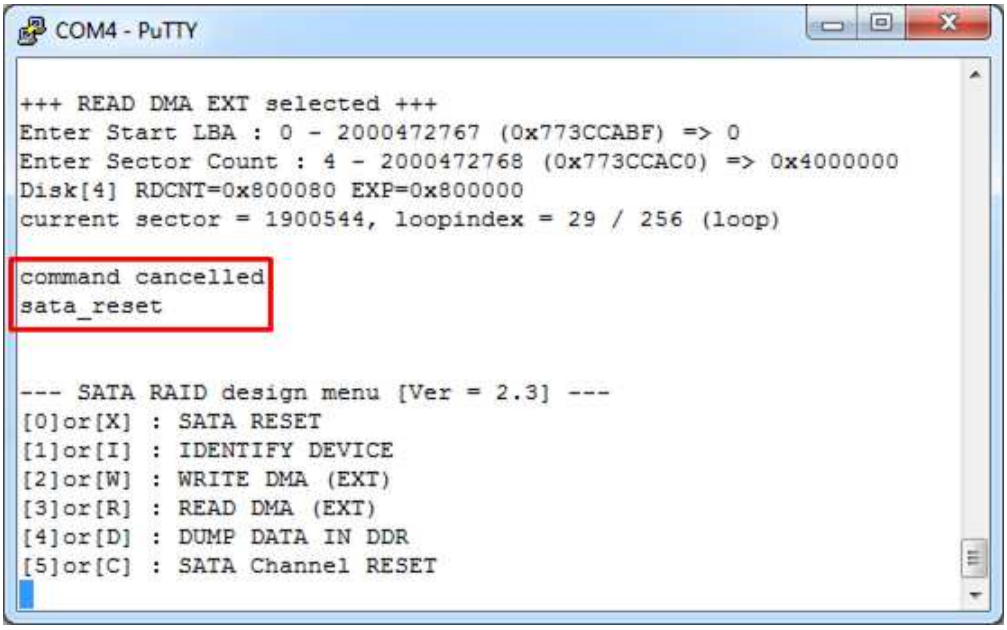

Figure 3-9 Read Operation cancelled from receiving input during operation

3.5 DUMP DATA IN DDR

Select '4' or 'D' to dump data from buffer to display on Serial Console. In this demo, DDR3/4 is mapped to address = 8000_0000h - BFFF_FFFFh (for all boards except KCU105) or 8000_0000h - FFFF_FFFFh (for KCU105). Six submenus can be selected, i.e.

- 'G': this submenu is used for selecting read DDR address, as shown in Figure 3-10. The address can be input to be hex value by adding prefix "0x", and decimal value will be received with no any prefix.

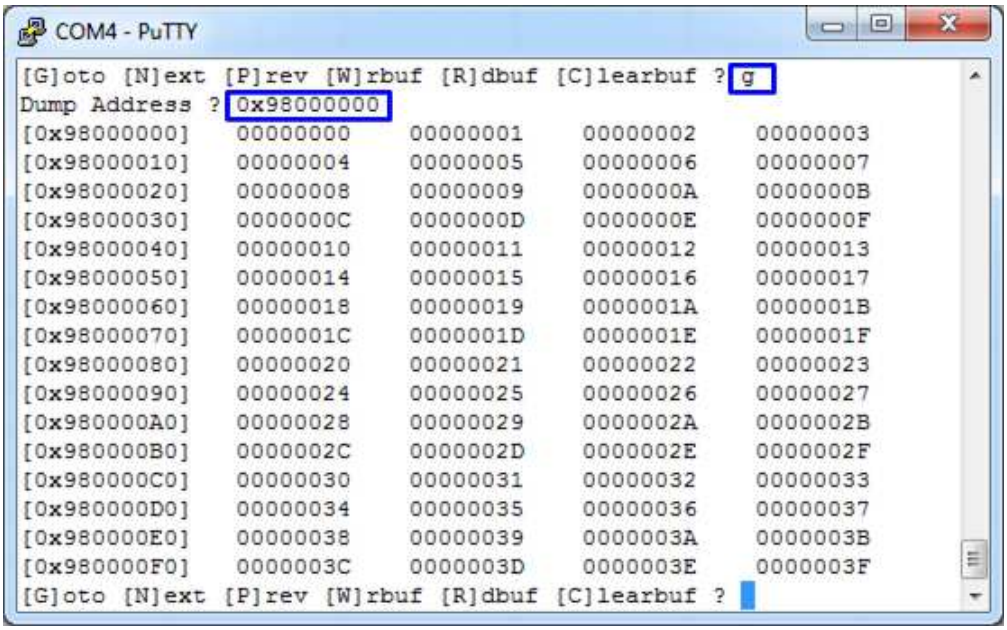

Figure 3-10 Goto submenu example

- 'N': this submenu is used for reading next 256 byte data in buffer, as shown in Figure 3-11.
- 'P': this submenu is used for reading previous 256 byte data in buffer, as shown in Figure 3-11.

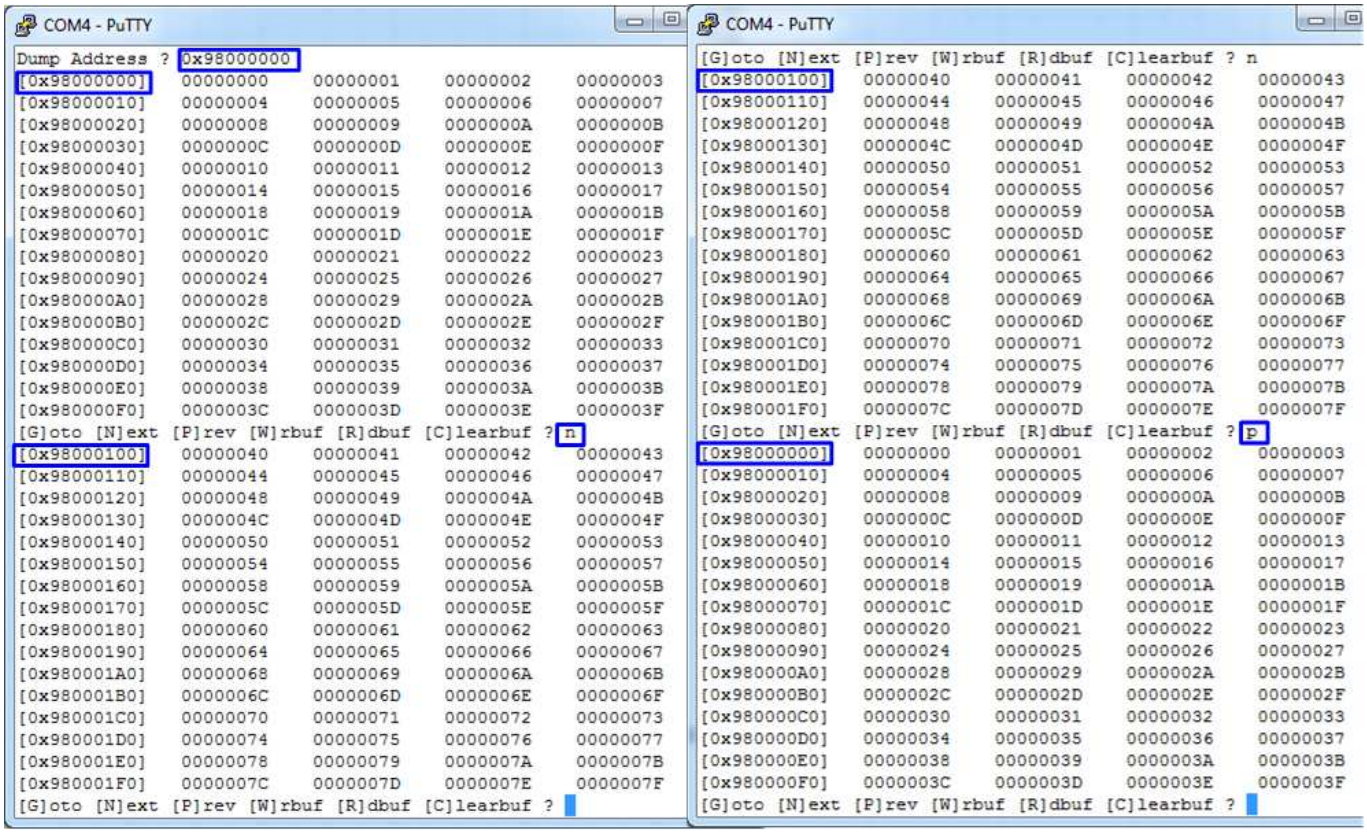

Figure 3-11 Read Next/Previous 256 byte data in buffer

- 'W': this submenu is used for reading 256 byte data at top address of write buffer, as shown in Figure 3-12.
- 'R': this submenu is used for reading 256 byte data at top address of read buffer, as shown in Figure 3-12.

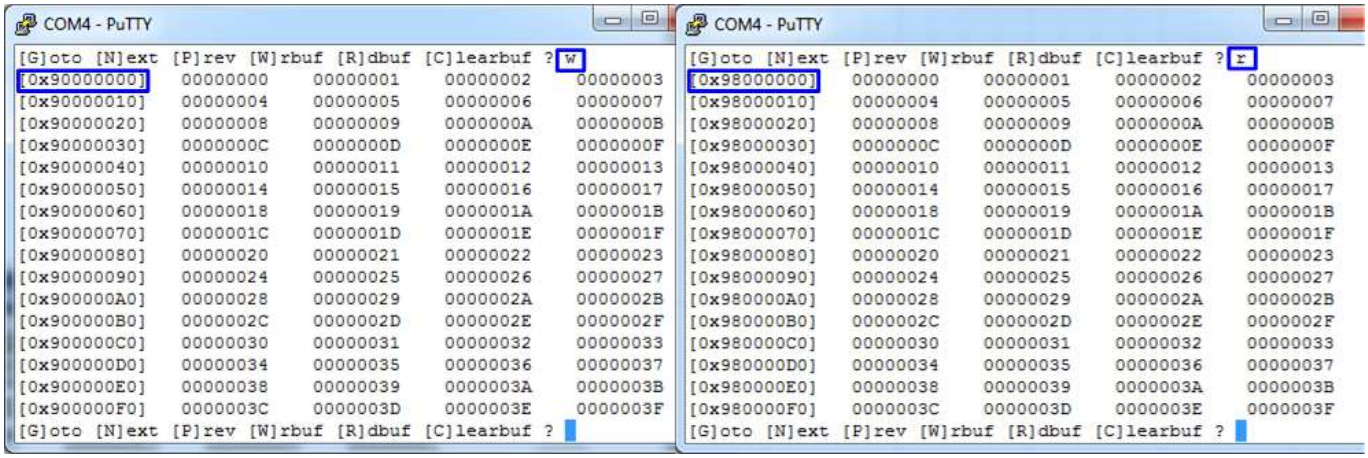

Figure 3-12 Read 256 byte data at top of write/read buffer

- 'C': this submenu is used for clear data in write/read buffer to zero value. Select 'Y' to confirm for clear write/read buffer, or select 'N' to cancel clearing buffer.

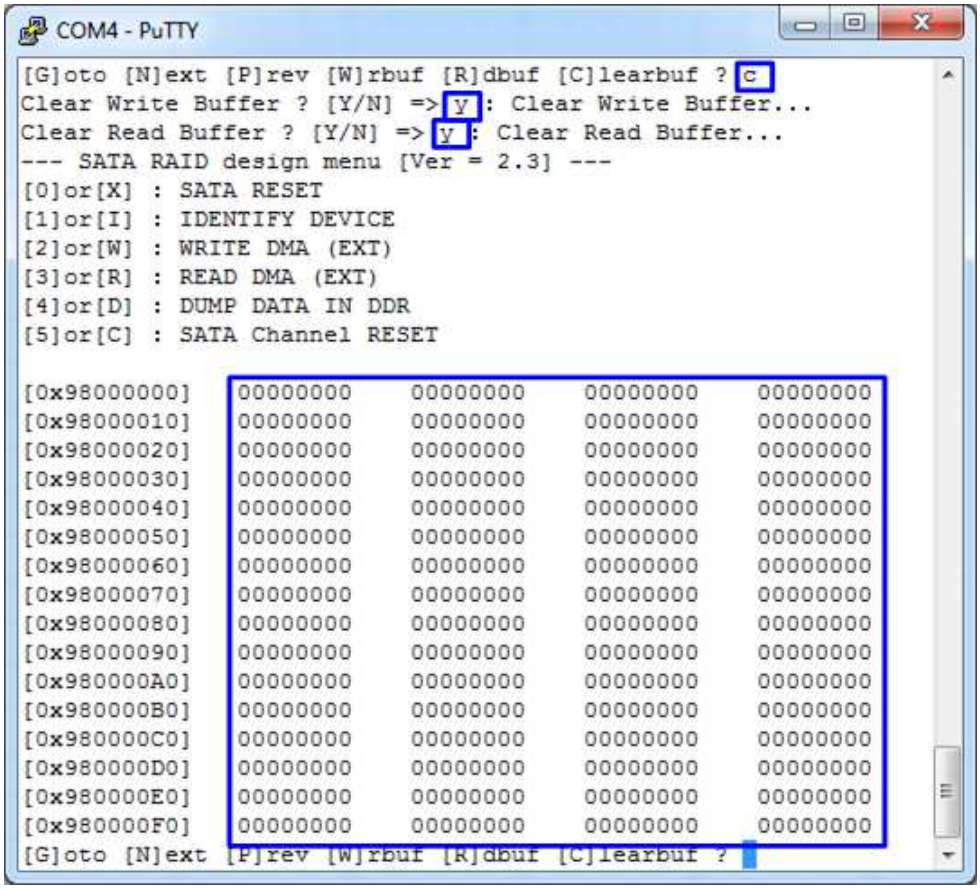

Figure 3-13 Clear buffer to be zero

User can exit this menu by input other key, such as 'x'.

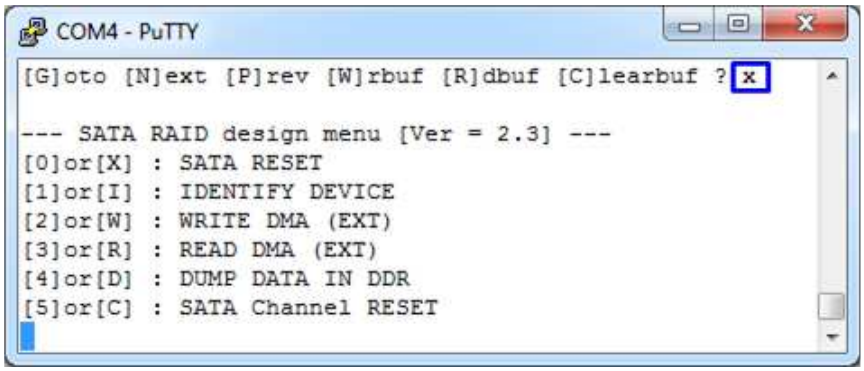

Figure 3-14 Exit dump menu

3.6 SATA Channel RESET

Select ‘5’ or ‘C’ to reset one of four SATA-IP and SATA-PHY.

One input is required to select SATA channel [0] – [3] which refers to SATA device at CN#0 to CN#3. LED1/3/5/7 will turn off during reset.

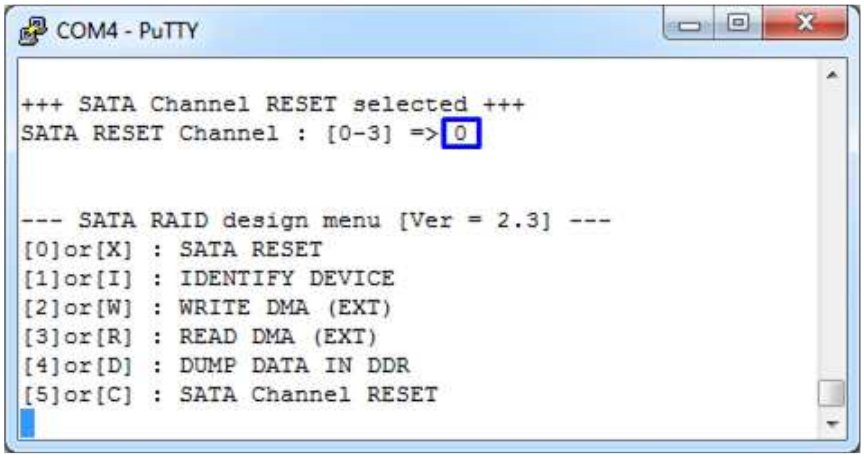

Figure 3-15 Reset for one SATA channel

4 Revision History

Revision	Date	Description
1.0	02-May-14	Initial version release
2.0	21-Jan-16	Support 7-series and KCU105 board