SATA-IP RAIDx4 reference design on 7-Series and KCU105

Rev2.0 7-Jul-23

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1. Introduction

Before starting RAID0 demo, it is recommended for user to read the details of one channel host demo reference design from “dg_sata_ip_refdesign_host_7series_en” document to understand SATA-IP and system environment firstly. In this document, it will describe only the additional part to extend SATA port from one channel to 4 channels and run RAID0 operation.

2. Environment

To run RAID0 reference design, please prepare following environment as shown in Figure 2-1.

- KC705/ZC706/VC707/VC709/KCU105 board
- Vivado/ISE for programming bit file
- FMC SATA RAID board, provided by Design Gateway
- 4 SATA-III Device (HDD/SSD) connecting to SATA connector on FMC SATA RAID board
- USB Micro-B cable for FPGA configuration
- USB Mini-B/Micro-B cable for serial communication. For serial communication, set baud rate=115,200 / data=8bit / Non-Parity / Stop=1bit.

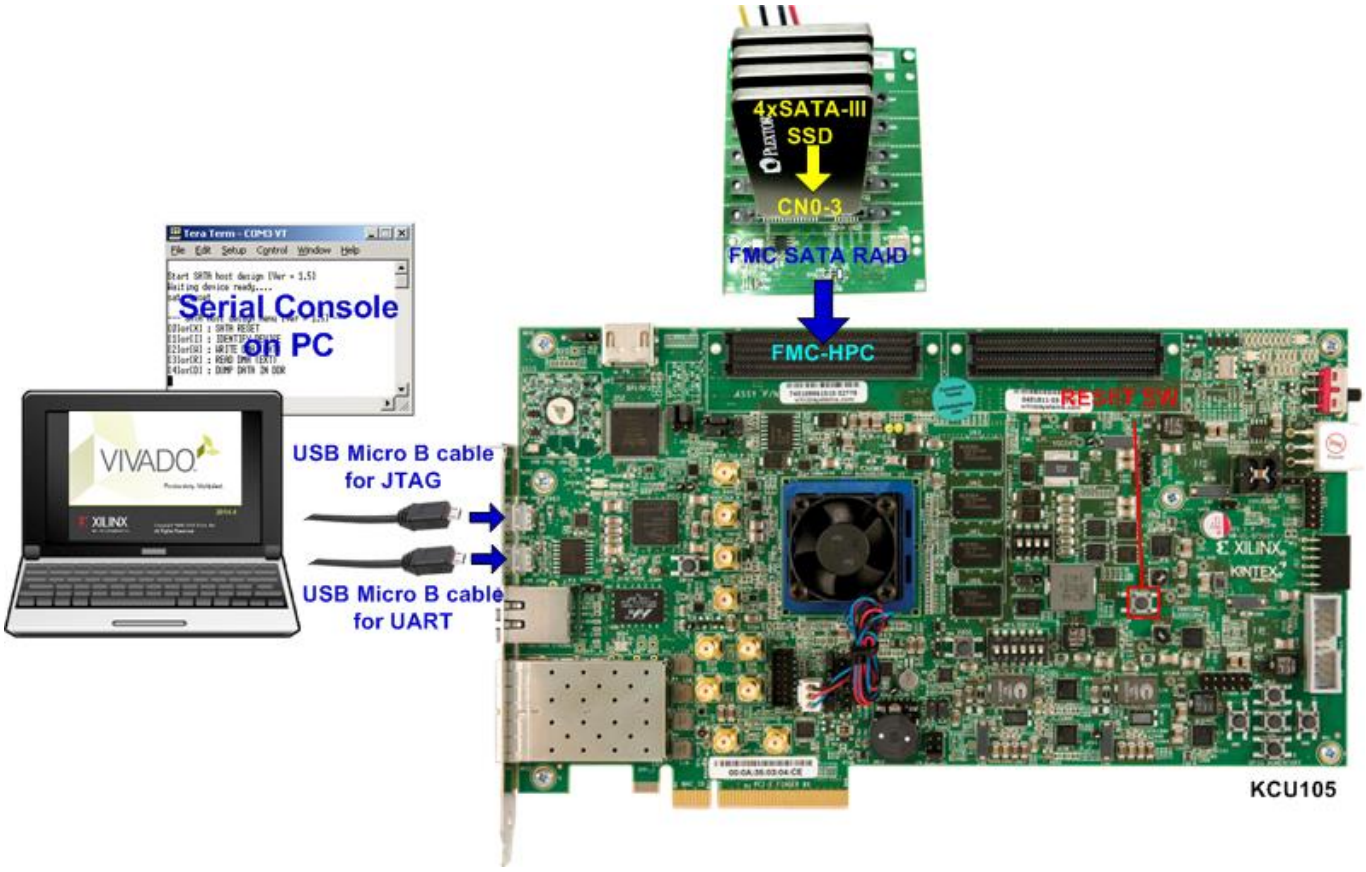

Figure 2-1 Reference design environment

The details to show how to run the demo step-by-step are described in “SATA-IP RAIDx4 Demo Instruction on 7-Series and KCU105” document.

3. Hardware description

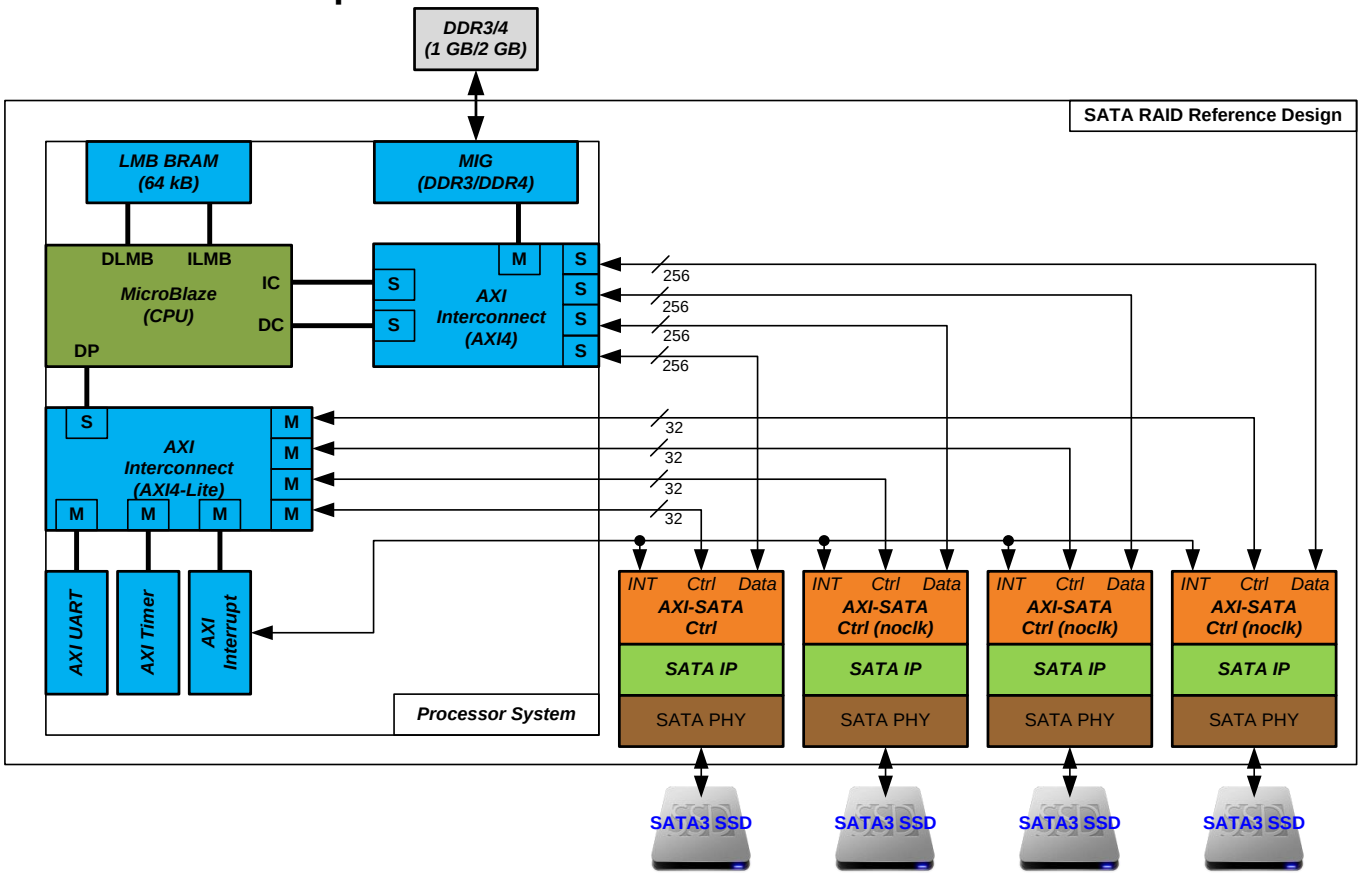

Figure 3-1 RAIDx4 reference design block diagram on FPGA board except ZC706

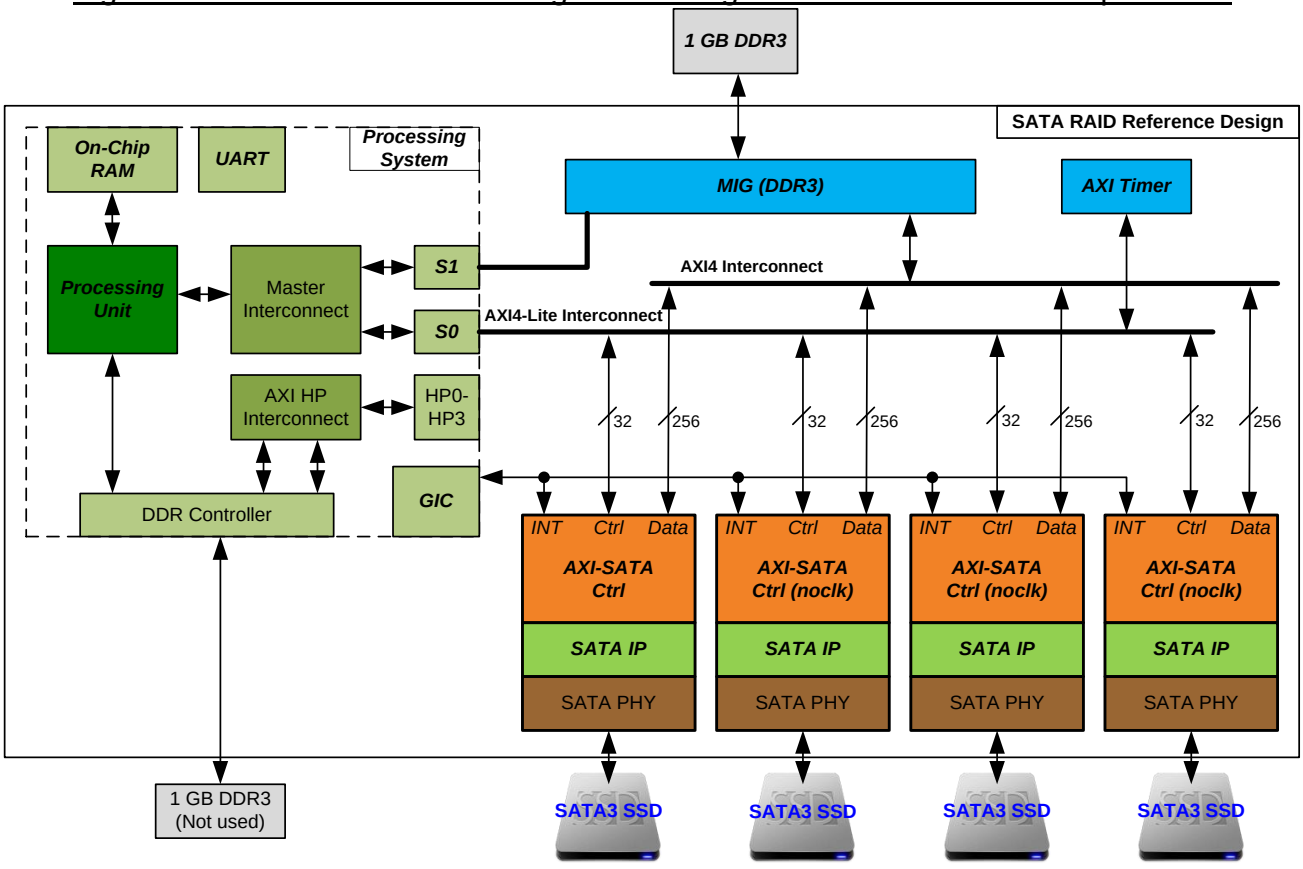

Figure 3-2 RAIDx4 reference design block diagram on ZC706 board

- SATA IP RAID0x4 design implementation on FPGA

To extend SATA channel from one to four channels, three AXI42SATA_noclk modules are added to connect to Processor system for RAID0 operation. To reduce clock resource, SATAPHY of additional channels will use shared clock resource output from the first channel (master channel). AXI4SATA (master channel) includes master PHY logic while AXI4SATA_noclk includes slave PHY logic which does not use clock resource. Similar to 1-ch host demo, data port of AXI42SATA(_noclk) connects to AXI4 bus of DDR3/4 while control/status port connects to processor (MicroBlaze/ARM) through AXI4-Lite bus.

- PHY Layer

Because of all four SATA channels share same clock resource, SATA PHY layer on RAID design will not support auto-speed negotiation function to switch SATA speed between SATA-III and SATA-II, like 1-ch design. Only SATA-III speed is supported for RAID design. PHY layer of master channel is “sata2phy_xx.vhd” while slave channel is “sata2phy_xx_noclk.vhd”.

- Transport Layer by AXI-SATACtrl

Block diagram and register map for AXI-SATACtrl in RAID0 demo is same as 1-ch host demo design. Please check more details from 1-ch host demo document. Since four channels are connected to AXI4 interconnect, so base address for AXI4-Lite interface of each channel will be assigned to different address. While data address to store FIS packet for each channel is shown in Figure 3-3. DDR memory area in this demo is split into 4 areas, i.e.

- TX_FIS_ADDR for storing transmit non-DATA FIS from processor to SATA device. All 4 SATA channels use the same transmit area to create same FIS to SATA device.
- RX_FIS_ADDR0-3 for storing received non-DATA FIS from each SATA device to processor, so four different areas are mapped in DDR.
- DATA_SEND_ADDR0-3 for storing transmit DATA FIS from processor to SATA device. Data in each SATA device is different, so four areas are mapped.
- RX_DATA_ADDR0-3 for storing received DATA FIS from each SATA device to processor, so four different areas are mapped in DDR.

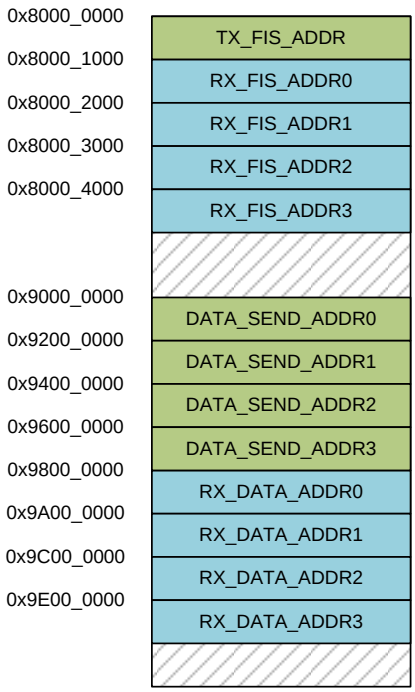

Figure 3-3 DDR3/4 memory map

4. Software description

Basic operation of RAID0 demo is same as 1-ch host demo. Three SATA commands are selected to implement in the demo, i.e. IDENTIFY DEVICE, WRITE DMA (EXT), and READ DMA (EXT). To start any command operation, processor firmware sends the same command to all SATA devices. So, address and transfer length of each command for all SATA devices will be set to same value. After sending command completely, each SATA channel will be controlled through interrupt service routine which is assigned to different function to separate the operation of each SATA device. Data in demo is arranged to RAID0 format by processor firmware in data preparation and verification function. Data area within DDR for each SATA device will be arranged in contiguous area.

Figure 4-1 shows reference design operation result on serial terminal screen.

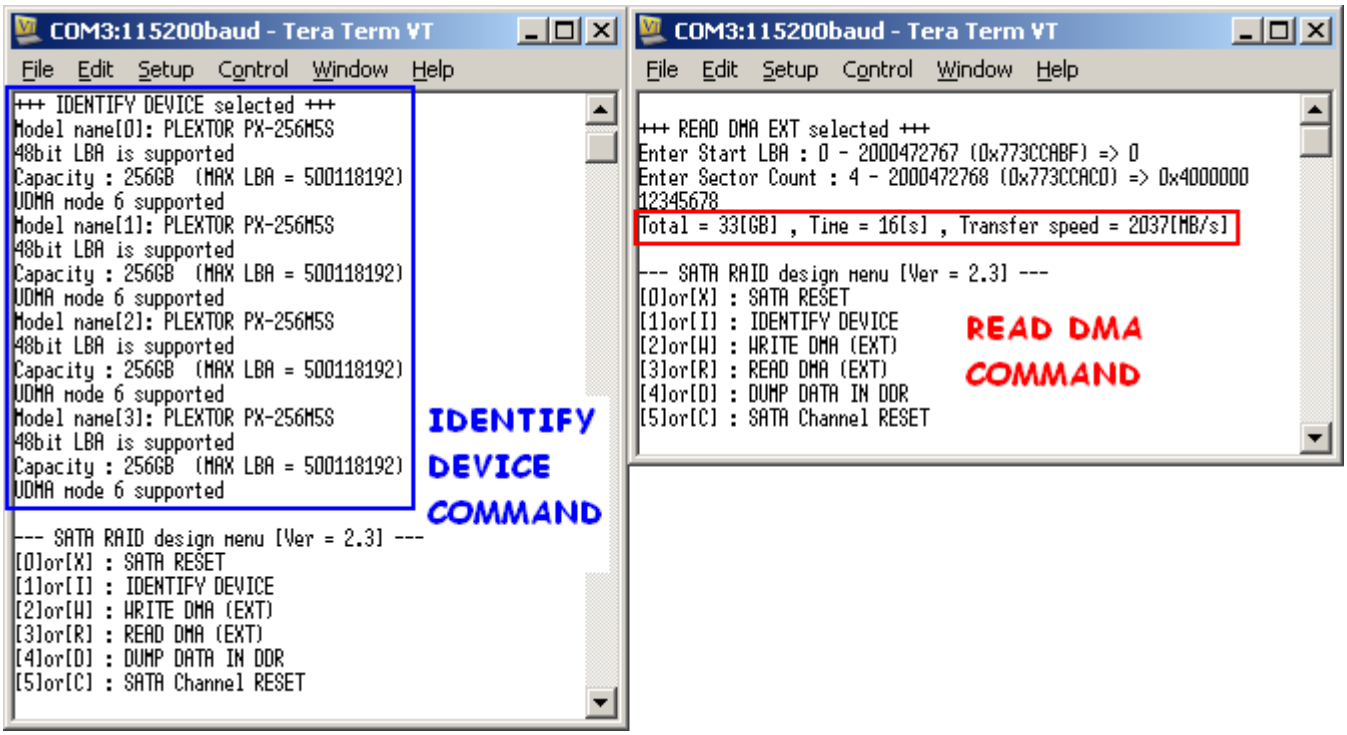

Figure 4-1 Operation result sample screen

5. Revision History

Revision	Date	Description
1.0	02-May-14	Initial release
2.0	22-Jun-16	Support 7-series and KCU105 board

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