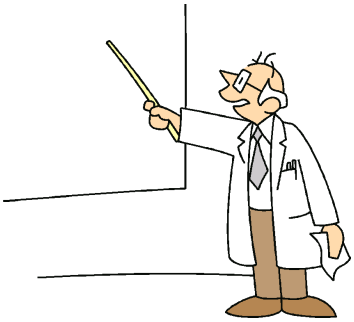
TOE10G-IP Introduction (Intel)

Ver1.2E

Ultimate 10GbE network solution!

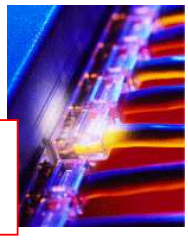
Agenda

- 10GbE&TCP/IP Overview
  - Advantage and Disadvantage of TCP on 10GbE
- TOE10G-IP core overview
- TOE10G-IP core description
  - Initialization
  - High-speed transmit
  - High-speed reception
- User I/F, Buffer size parameterization
- Reference design
- Resource usage and real performance



10GbE Overview

- **What is 10GbE (10Giga-bit Ethernet)?**
  - **Industrial standard high-speed network**
  - **10Gbps transfer speed**
  - **Many connection type**



TOE10G-IP is applicable to all 10GbE standard

Connection Type	Merit	Demerit	Note
Optical Cable	Low latency (100ns) Long distance	Expensive	Needs optical module and cable
Direct Attach	Low cost	Short distance (5-7m maximum)	Direct insertion to SFP+ socket
10GBASE-T	Low cost Popular (RJ-45)	High latency (2us)	Special coding (LDPC)

10GbE connection type

Advantage of TCP/IP on 10GbE

- **Advantage of TCP/IP**
  - **Standard Ethernet protocol**
  - **Guaranteed data reliability**
  - **Major OS provides protocol stack**

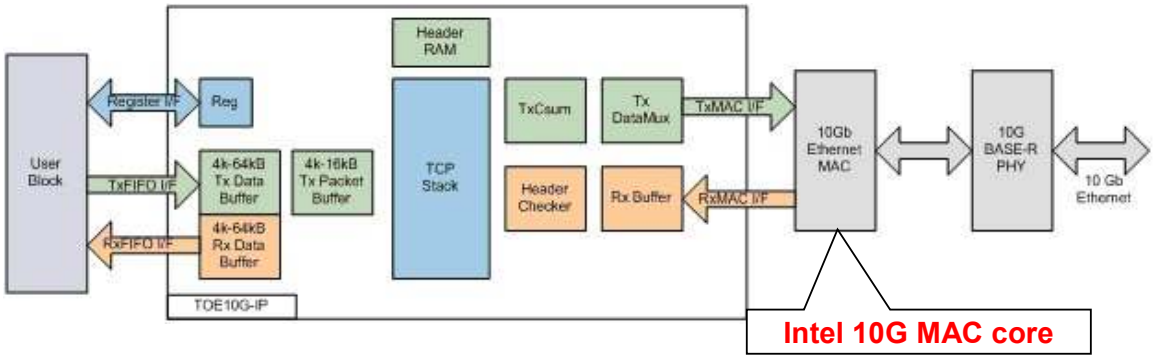
Windows Linux Mac OS solaris VxWorks WIND RIVER

- **Disadvantage of TCP/IP**
  - **Heavy CPU load due to complicated TCP process**
  - **Difficult to raise performance(30-40% efficiency)**
  - **Needs expensive high performance CPU**

TOE10G-IP core can provide ideal solution!

TOE10G-IP core Overview

- TCP/IP off-loading engine for 10GbE
- Inserts between user logic and Intel 10G MAC module
- Fully hard-wired TCP control for both Tx and Rx
- Supports Full Duplex communication



TOE10G-IP core block diagram

TOE10G-IP core Advantage 1

- Fully hard-wired TCP/IP protocol control
  - Possible to build CPU-less network system
  - Zero load for CPU
- Ultra high speed for both of Tx and Rx direction
  - About 1200MByte/sec real transfer speed
- Guarantee transfer data reliability
  - Tx: Automatic retry when No-ACK, Duplicate-ACK, timeout
  - Rx: Automatic ACK control by Sequence number calculation

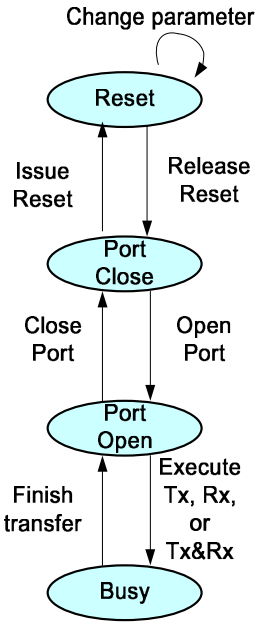
TOE10G-IP core Advantage 2

- **Selectable data buffer size**
  - Selectable buffer size of memory usage vs. performance
- **Compatible with Intel MAC core (LL Ethernet 10G MAC)**
  - Also supports low cost 10GEMAC-IP from DesignGateway
- **Many reference design on Intel evaluation board**
  - Full project for standard Intel board
  - Free SOF-file for evaluation before purchase
  - All source code (except IP-core) in design project
  - Multiple Sessions design available for Server Application

- **Supports 10GBASE-T as well as 10GBASE-R**
  - Applicable to low cost Cat6 cable and RJ45 connector

TOE10G-IP core Operation

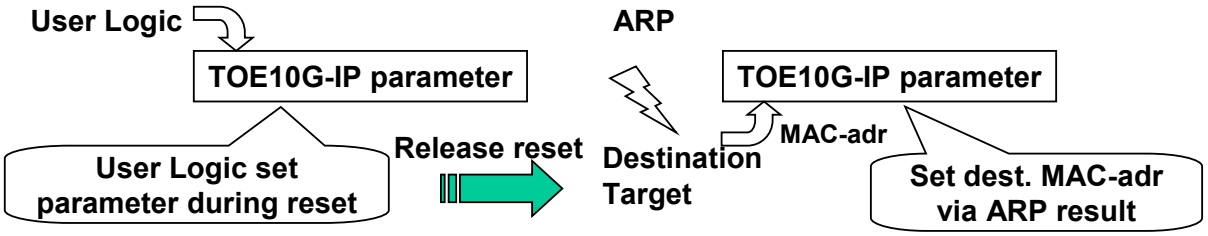
- **Set parameter (IP-adr&MAC-adr, etc) during Reset**
- **Release Reset then initialize including ARP**
- **Idle state after initialization finish, wait command**
- **Port open by either of Active (Client) or Passive (Server) mode**
- **Tx and Rx operates individually (full-duplex)**
- **If want change parameter, move to Reset state (transfer/packet length can change except Busy)**



State Diagram

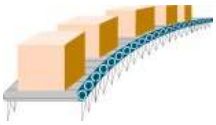
TOE10G-IP Initialization

- Set parameter to TOE10G-IP
  - User logic can set parameter during TOE10G-IP reset
  - Set IP address, MAC address, and Port number
  - Release reset after parameter setting finish
- TOE10G-IP executes ARP after reset release
  - Issue ARP to destination target
  - Get MAC-adr of the target via ARP result



High-Speed Tx

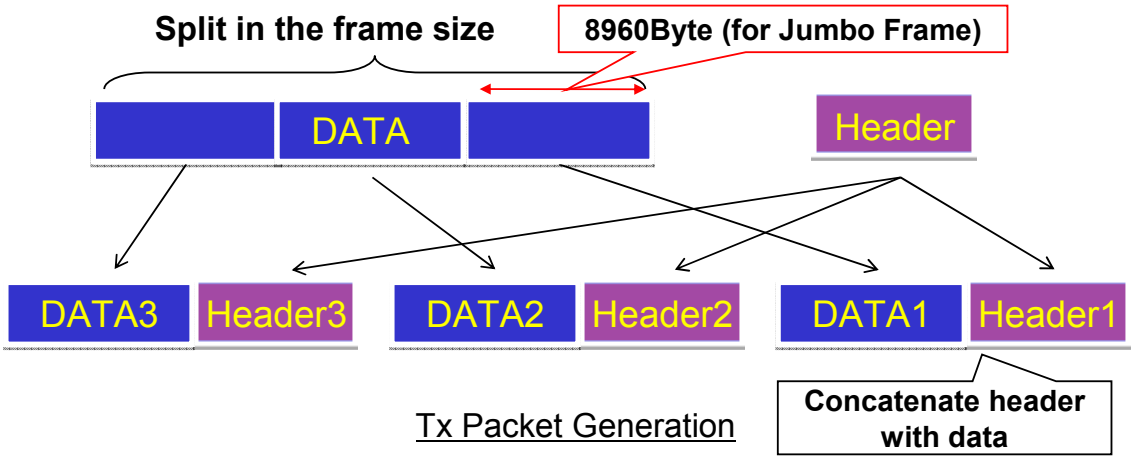
- Tx packet generation
  - User Logic writes Tx data to TxFIFO
  - Split Tx data in the frame size
  - Concatenate header with Tx data



- Automatic retransmit function
  - Check ACK reply from destination
  - Detect No-ACK, Duplicate-ACK, and Timeout
  - Resend same packet by such ACK error detection

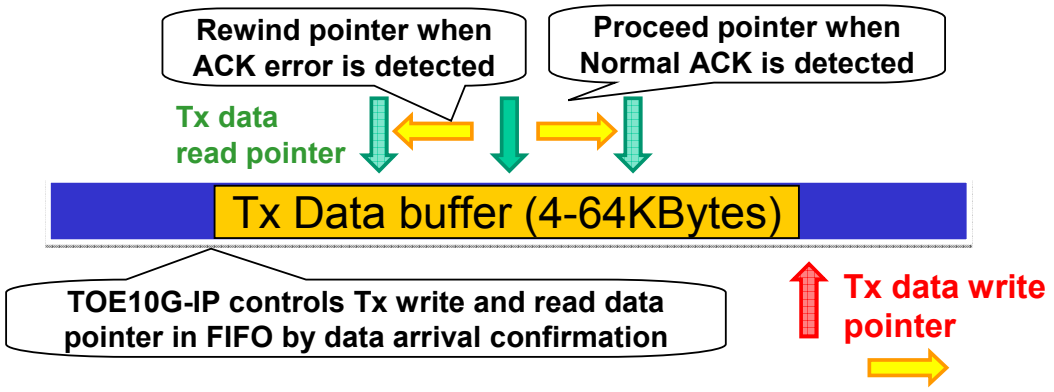
Tx Packet Generation

- Generate header and concatenate it with Tx data
  - TOE10G-IP splits Tx data in the frame size
  - Generate checksum and sequence number in TOE10G-IP



Automatic retransmit

- Retransmit function by dedicated FIFO
  - Proceed pointer by normal ACK reception
  - Rewind pointer by illegal ACK reception
  - TOE10G-IP controls pointer and retransmit operation



High-Speed Rx

- **Rx packet header check**
  - **Ignore packet if destination is not TOE10G-IP or if checksum is wrong**

- **Data reordering**
  - **Reorder when sequence number skip is detected**
  - **Avoid retransmit request for transfer efficiency**
  - **If reordering is not possible, then send duplicate ACK**

- **Duplicate data management**
  - **Check duplicate data in Rx packet**
  - **Retrieve original data by trimming duplicate data part**

Rx Packet Header Check

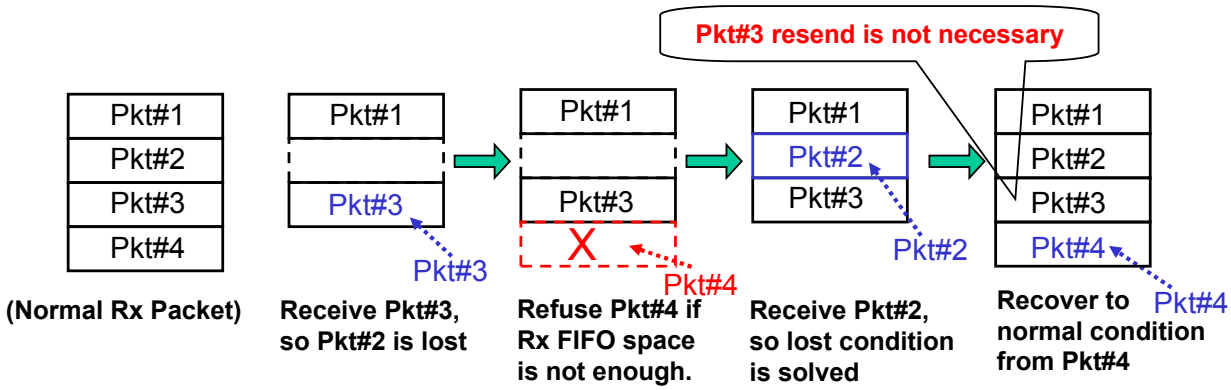
- **Verify header check sum in Rx packet**
  - **Also check following condition in TOE10G-IP**

Byte Offset	Protocol	Description	Check condition
0-5	ICMP	Destination MAC adr	Match with MAC adr set by SML/SMH register
6-11	ICMP	Source MAC adr	Match with target MAC adr set by ARP
12-13	ICMP	Type	= 0x0800 (IP packet)
14	IP	Version/Header	= 0x45 (IPv4, IP header len=20)
20	IP	Flag/Fragment OFS	= b"000000" (no fragment)
23	IP	Protocol Number	= 0x06(TCP packet)
26-29	IP	Source IP adr	Match with IP adr set by DIP register
30-33	IP	Destination IP adr	Match with IP adr set by SIP register
34-35	TCP	Source port number	Match with DPN register or extracted target port number in Passive Open
36-37	TCP	Destination port number	Match with port number set by SPN register
38-41	TCP	Sequence number	Possible value within TOE2-IP core can process this packet

Header check condition in Rx packet

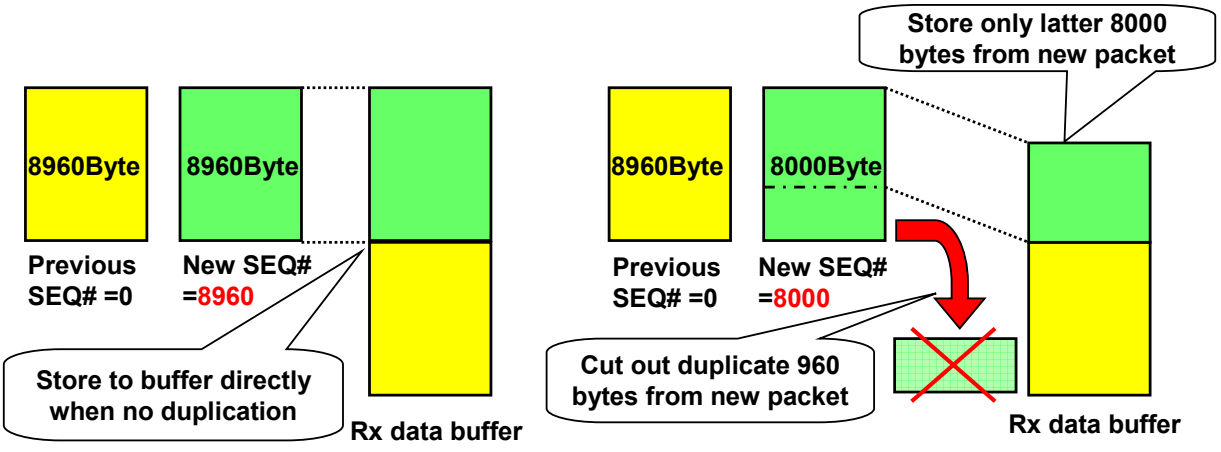
Data Reordering

- **Function when SEQ number skip is detected**
  - Not accept any packet other than that can solve lost condition
- **Data reordering function**
  - Recover data contiguous from lost-solved packet
  - Keep performance by suppress resend request



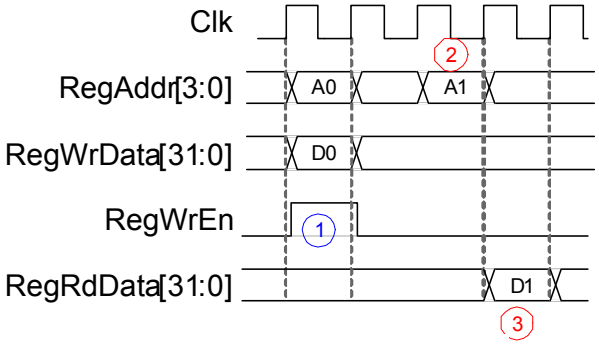
Duplicate data trimming

- **Detect data duplication and correct automatically**
  - Detect Rx data duplication by checking sequence number
  - Trim duplicate block and retrieve contiguous data



User Interface (Control)

- **3 types of Register I/F, Tx FIFO I/F, and Rx FIFO I/F**
  - **Register I/F for initial parameter setting and Tx/Rx command**
  - **Tx FIFO I/F and Rx FIFO I/F is standard FIFO interface**

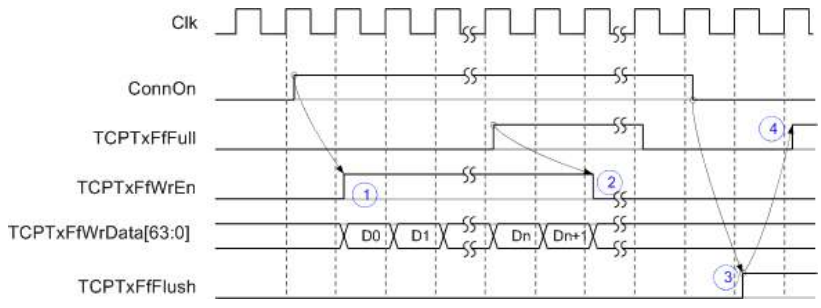


Register I/F timing

[Register Write]
(1) Assert RegWrEn with RegAddr and RegWrData

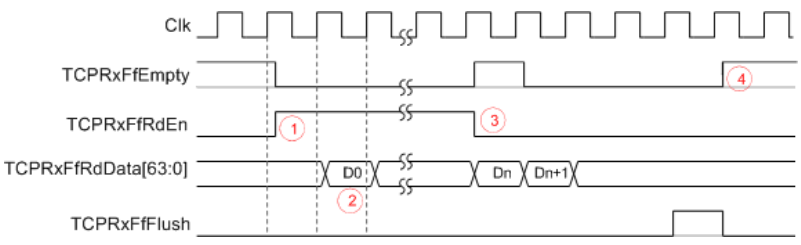
[Register Read]
(2) Set RegAddr
(3) Valid RegRdData output in the next clock

User Interface (Data)



Tx FIFO I/F timing

[Tx data write]
(1) Write data with WrEn
(2) Suspend write within 4 Clk after Full assertion
(3) FIFO clear by Flush



Rx FIFO I/F timing

[Rx data read]
(1) Read by RdEn assertion when not Empty
(2) Read data after 1 Clk
(3) Read is inhibited when Empty
(4) FIFO clear by Flush

Buffer Capacity

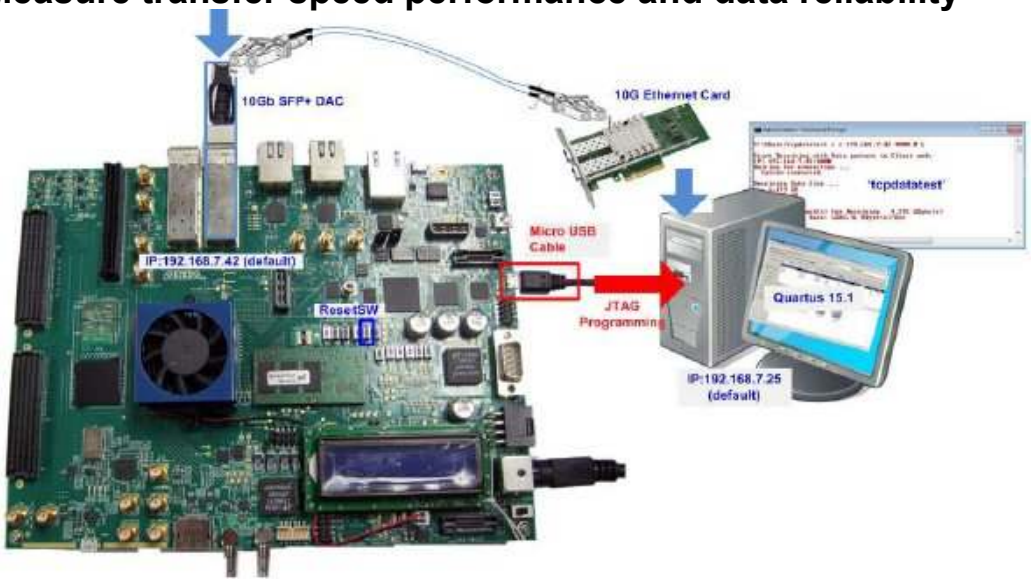
- **Parameterized 3 types of data buffer**
  - **(1) Tx Data Buffer: 4KBytes - 64KBytes**
  - **(2) Tx Packet Buffer: 4KBytes - 16KBytes**
  - **(3) Rx Data Buffer: 4KBytes - 64KBytes**
- **User can optimize resource usage and performance**

Generic Name	Range	Description
TxBufBitWidth	9-13	Set Tx data buffer size in address bit width When set to 9, size is 4KBytes, when 13, 64Kbytes for example.
TxPacBitWidth	9-11	Set Tx packet buffer size in address bit width When set to 9, size is 4Kbytes, when 11, 16KBytes for example
RxBufBitWidth	9-13	Set Rx data buffer size in address bit width When set to 9, size is 4KBytes, when 13, 64KBytes for example.

Buffer size is selectable by parameterization

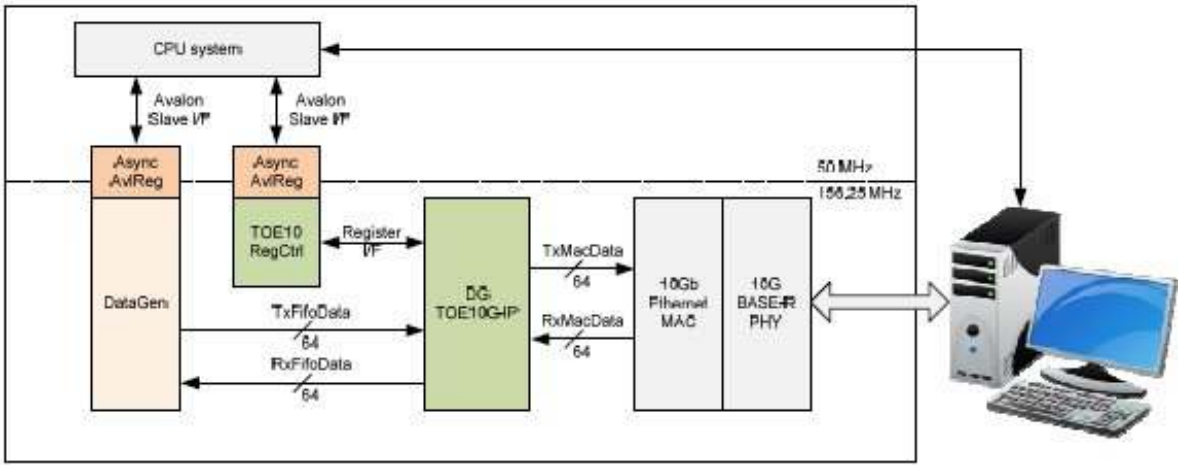
Free SOF File for Evaluation

- **Bit file for evaluation with Intel standard board**
  - **Ready for A10SX,A10GX,C10GX,S10GX, IntelPAC board**
  - **Measure transfer speed performance and data reliability**



Reference Design Overview

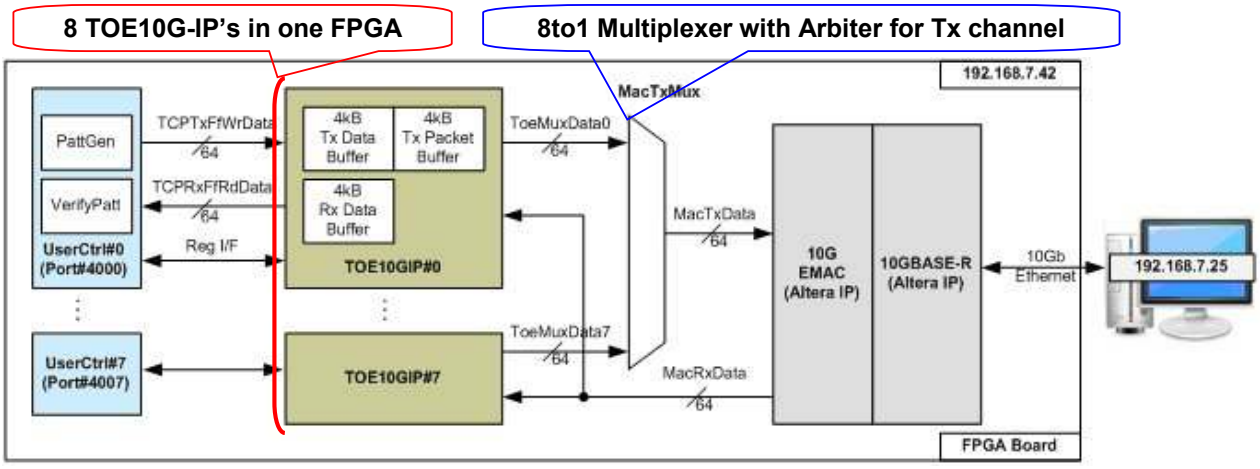
- **QuartusII design project for real operation**
  - **All source code (except IP-core) included in full project**



Reference design block diagram

Multiple Sessions Design

- **Reference design for Server Application**
  - **8 Instances in one FPGA to support 8 sessions operation**



Multiple Sessions reference design block diagram

Effective Development on Ref. Design

- Vivado project is attached to the package
- Full source code (VHDL) except IP core
- Can save user system development duration
  - Confirm real board operation by original reference design.
  - Then modify a little to approach final user product
  - Check real operation in each modification step.

Short-term development is possible without big turn back

Supports 10GBASE-T

- Applicable to low cost CAT6 cable/RJ45 connector
  - Transfer performance is almost equal to 10GBASE-R

Standard	Tx	Rx	Full-Duplex
10GBASE-R	1219MByte/s	1109MByte/s	800-1000MByte/s
10GBASE-T	1205MByte/s	1103MByte/s	800-1000MByte/s

TOE10G-IP core performance test result

Condition: reference design between PC and A10GX board
Packet size: 8960byte (Jumbo Frame)
Use "ASF-10G-T" from 10GTek for 10GBASE-T environment test
PC specification: CPU Inteli5-8500@3.00GHz, DDR4 16GB, Windows10Pro, NIC card: X550-T1(Intel)
*** Performance result varies in the range of 800-1000MB/s with each trial for full-duplex test**

Resource Usage

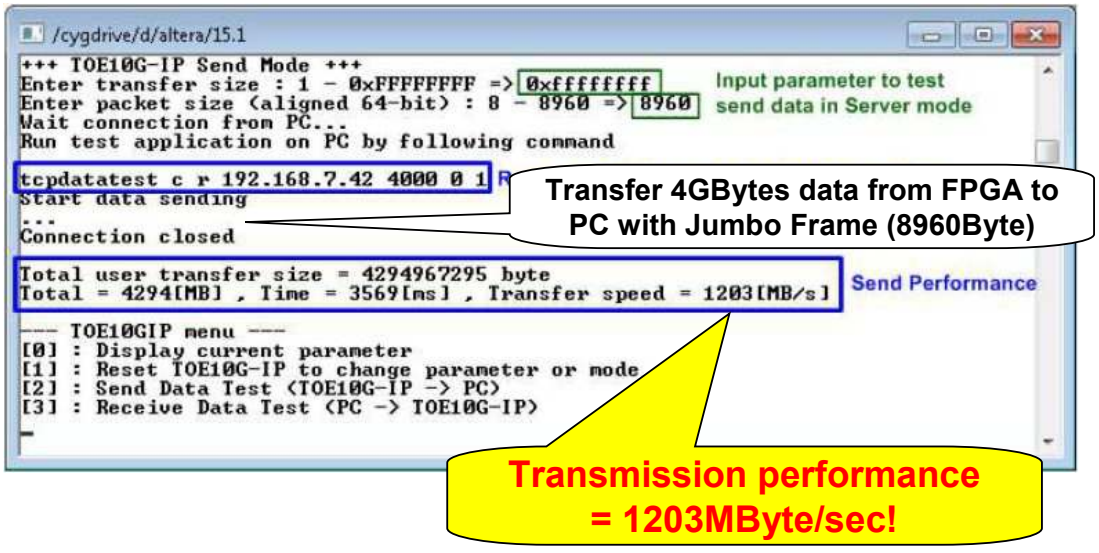
- **TOE10G-IP core standalone resource usage**
  - **Condition = Maximum buffer setting**
    (TxDataBuf=RxDataBuf=64KB, TxPacketBuf=16KB)

Family	Example Device	Fmax (MHz)	ALMs[1]	Registers[1]	Pin	Block Memory bit[2]	Design Tools
Arria 10 SX	10AS066N3F40E2SGE2	156.25	2,566	3,931	-	1,179,648	QuartusII16.0
Arria 10 GX	10AX115S2F45I2SG	156.25	2,453	3,491	-	1,179,648	QuartusII16.0
Cyclone 10 GX	10CX220Y7F80E5G	156.25	2,247	3,446	-	1,179,648	QuartusII18.0
Stratix 10 GX	1SG280HU2F50E2VGS1	156.25	2,928	3,523	-	1,179,648	QuartusII18.0

TOE10G-IP core standalone compilation result

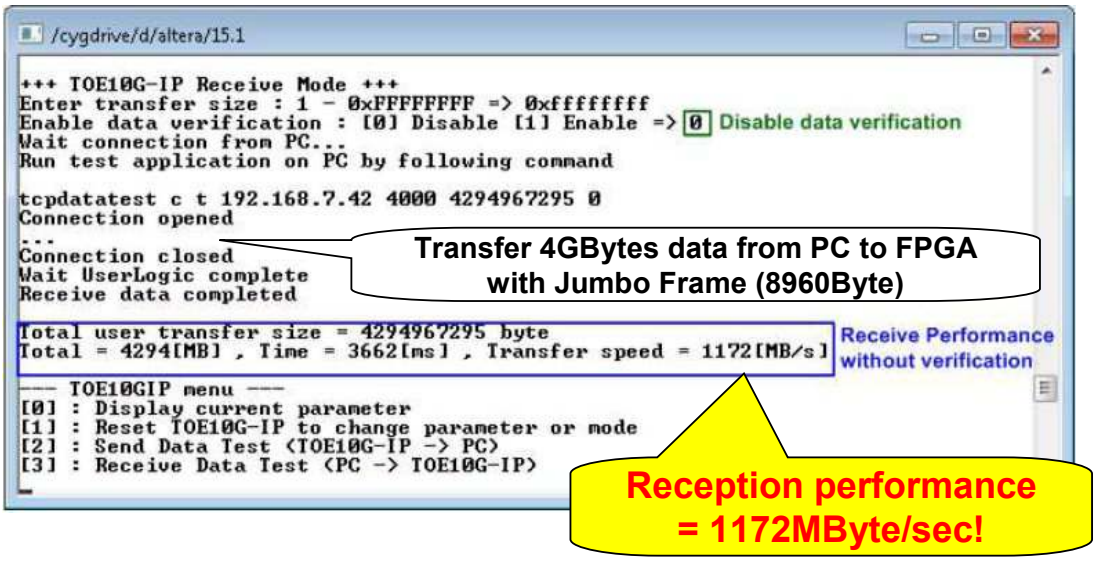
This result is based on maximum buffer size setting.
User can save memory resource by smaller buffer size setting

Transmission Performance



Transmission (FPGA to PC) performance result using Arria10SoC Bd.

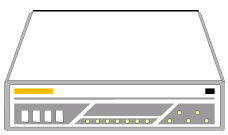
Reception Performance



Reception (PC to FPGA) performance result using Arria10SoC Bd.

TOE10G-IP Application Market

- **Data transfer in FA market**
  - **Medical video processing system**
  - **Sensor data logger measurement instrument**
- **Storage system using TCP such as NAS, iSCSI**
  - **TOE10G-IP replaces CPU for hard TCP processing**
- **Network product**
  - **Network printer for high speed print data download**
  - **Network camera for high speed video data upload**


For more detail

- **Detailed documents available on the web site.**
  - http://www.dgway.com/TOE10G-IP_A_E.html
- **Contact**
  - **Design Gateway Co,. Ltd.**
  - **E-mail : ip-sales@design-gateway.com**
  - **FAX : +66-2-261-2290**

Revision History

Rev.	Date	Description
1.0E	August 1, 2016	English version initial release
1.1E	February 8, 2017	Added multiple sessions design for server application reference
1.2E	February 19, 2021	Added 10GBASE-T support and A10GX,C10GX,S10GX family information