TOE10G-IP Demo Instruction

Rev1.1 18-Nov-16

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between FPGA development board and PC through 10 Gigabit Ethernet. This demo can select to run with supported and unsupported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1-1, to run TOE10G-IP standard demo, please prepare

1) FPGA Development board (Arria10 SoC development board)
2) PC with 10 Gigabit Ethernet support or 10 Gigabit Ethernet card
3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
4) micro USB cable for programming FPGA between FPGA Development board and PC
5) "send_tcp_client_10G.exe" and "recv_tcp_client_10G.exe", provided by Design Gateway, which are test application available on PC

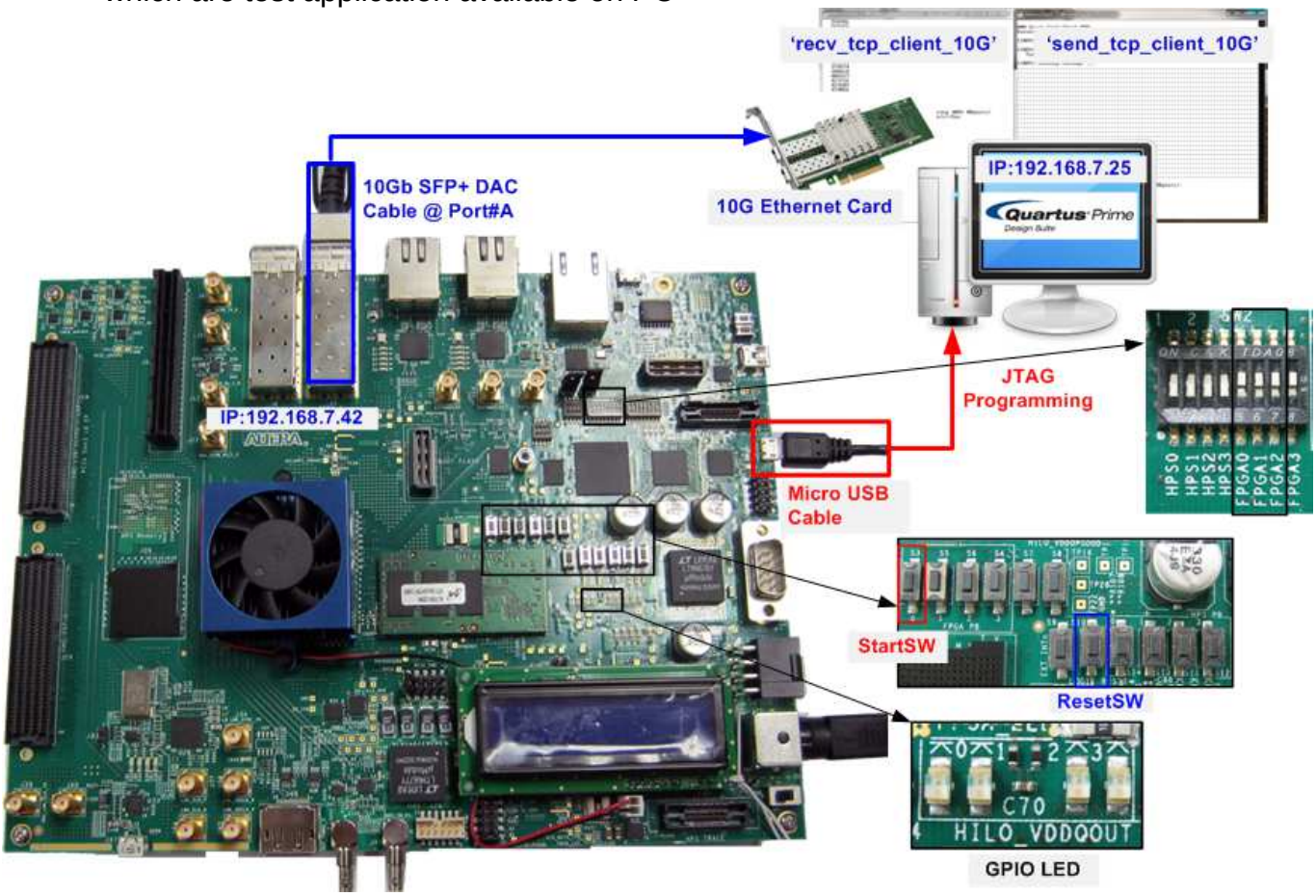

Figure 1-1 TOE10G-IP Demo Environment Setup on Arria10 SoC board

Note: Test result in this document is captured by using following test environment.

[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html

[2] 10-Gigabit SFP+ DAC cable
http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx

[3] PC: Motherboard ASUS H87M-E, 32 GB RAM, 64-bit Windows7 OS

2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC.

To select test mode and test parameter such as transmit packet size, user can set by 3-bit DIPSW at Bit5-7 of SW2 on the board as shown in Figure 2-1. The description of each bit is shown in Table 2-1.

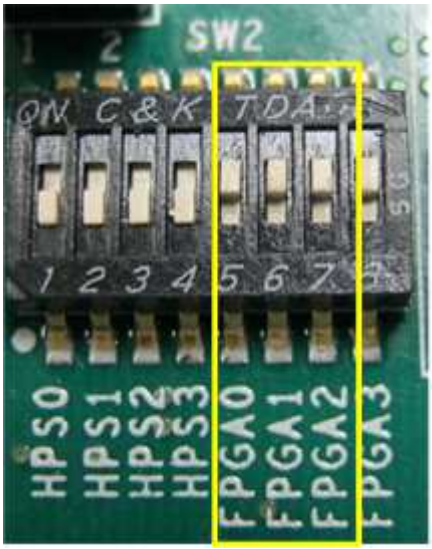

Figure 2-1 FPGA DIPSW to select test mode

Table 2-1 DIPSW Setting Definition

FPGA	ON (Logic '0')	OFF (Logic '1')
Bit 0	Sending mode by using non-Jumbo frame (1456 bytes)	Sending mode by using Jumbo frame (8960 bytes)
Bit 1	Sending mode	Receiving mode
Bit 2	Receiving mode without data verification	Receiving mode with data verification

The status of the demo can be monitored by 4-bit FPGA LED (D25 – D28) as shown in Figure 2-2. The description of each status LED is shown in Table 2-2.

Figure 2-2 FPGA LED to show test status

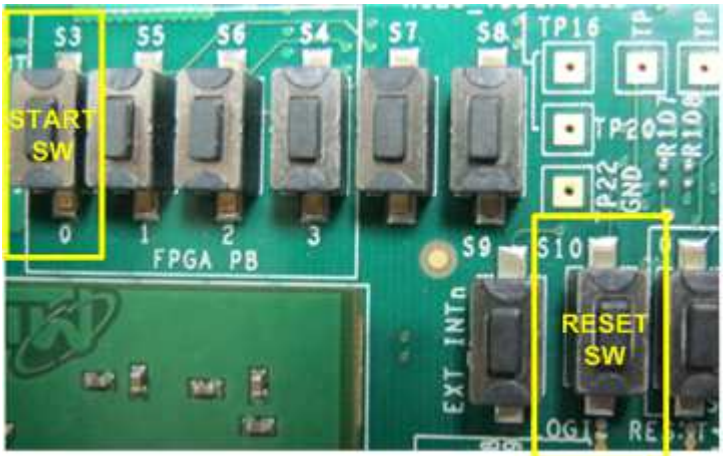

Figure 2-3 Start SW and Reset SW position

Table 2-2 LED Definition

FPGA LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (S3) has already been pressed and confirm IP address setting on PC that is correct.
1	BLINK: Operation timeout	Normal operation
2	Sending mode in jumbo frame	Sending mode in non-jumbo frame
3	BLINK: Data verification is fail in receiving mode ON: Port is established	No operation

Note:
- DIPSW setting must not be changed during operation in processing.

More details about each test mode are follows.

2.1 Sending mode

In this mode, 32 GB data will be transferred from FPGA development board to PC, and "recv_tcp_client_10G.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select 2 transfer packet sizes by DIPSW[1] setting, i.e. 1456 data byte for running with unsupported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting by monitoring LED2 status.

The operation sequence for sending mode is shown as follows.

1) TOE10G-IP within FPGA development board initializes parameters in system such as packet size, transfer size, MAC address, and IP address. Then, the system waits open connection from PC.
2) Test application on PC opens connection to connect with FPGA development board, and then waits data sending.
3) TOE10G-IP starts to send 4 GB data to PC for 8 times (8x4GB = 32 GB) while PC verifies received data that is correct.
4) After all data are transferred, TOE10G-IP sends packet to close connection.
5) PC sends acknowledgement to close connection. Then, operation will repeat from Step2) to Step5). The operation can be cancelled when test application on PC is cancelled by user.

2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By running "send_tcp_client_10G.exe" application on PC, data will be sent out until total numbers of transferred data equal to setting value. This test can run in 2 modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC to reduce PC resource and run in the best performance condition. Verification module within FPGA development board will be OFF to disable data verification module.

In data verification mode, 32-bit increment data will be generated from PC to check data reliability. Verification module within FPGA will be ON to verify all received data. LED error will blink if any error is detected. Verification ON/OFF within hardware is set from DIPSW[2] while test application can set the option in command line to ON/OFF function to generate test pattern.

The operation sequence for receiving mode is follows.

1) Similar to Step 1) in Sending mode.
2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
3) TOE10G-IP receives data and verifies data if enable.
4) After all data are transferred, Test application sends packet to close connection.
5) TOE10G-IP sends acknowledgement to close connection. This mode will run only one time, not in loop like Sending mode.

3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

3.1 IP Setting

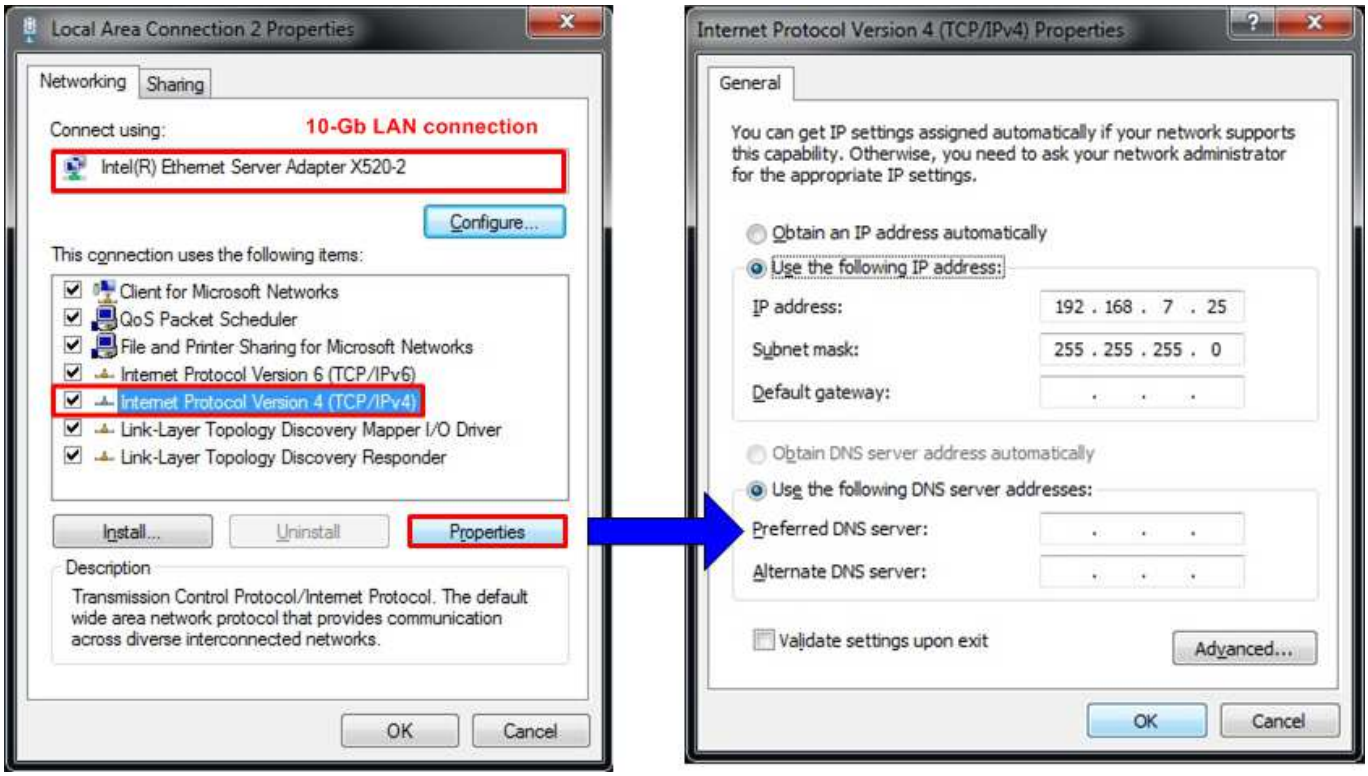

Figure 3-1 IPv4 Setting

- Open Local Area Connection Properties of 10-Gb connection, as shown in left window of Figure 3-1.
- Select “TCP/IPv4” and then click Properties.
- Set IP address = 192.168.7.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 3-1.

3.2 Speed and Frame Setting

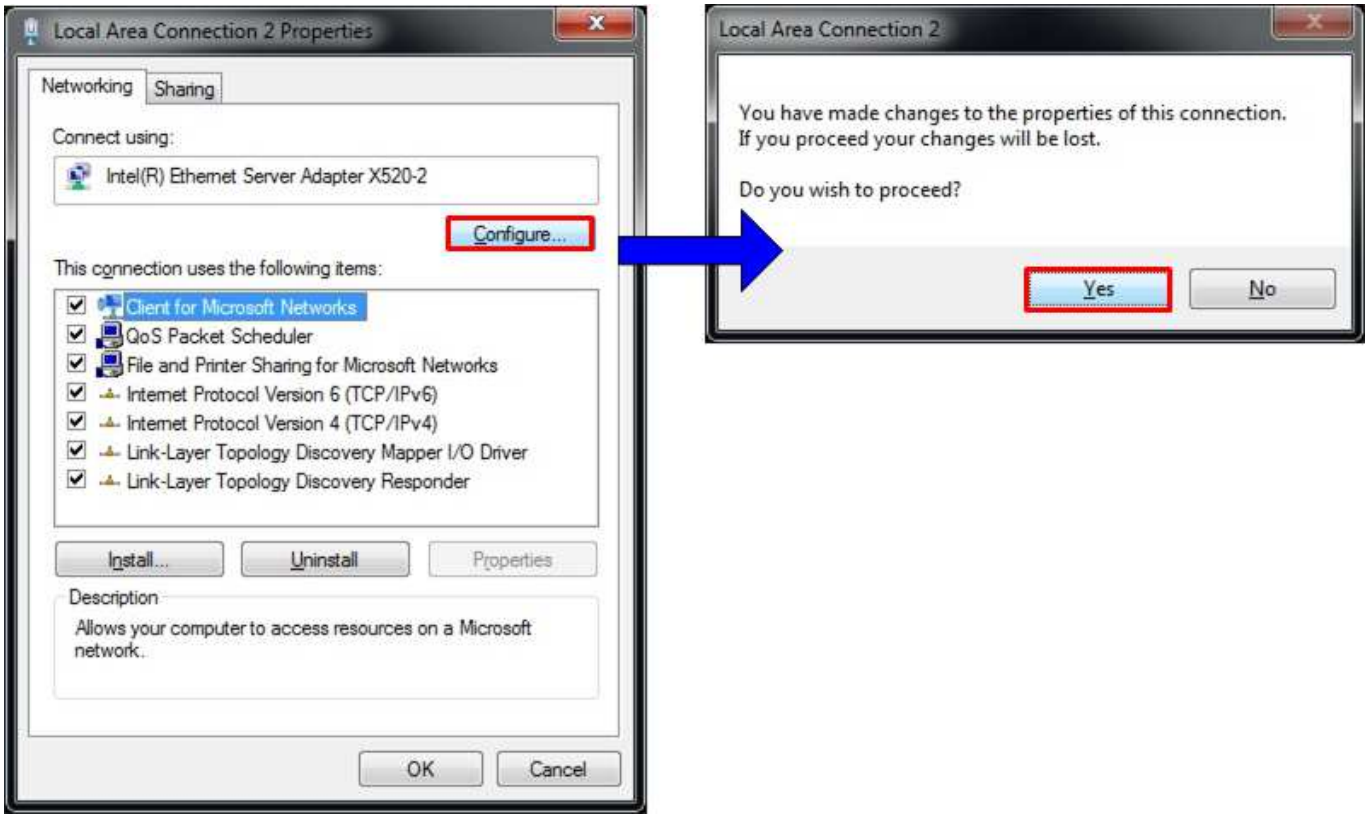

Figure 3-2 Network Configure

- On Local Area Connection Properties window, click “Configure” as shown in Figure 3-2.

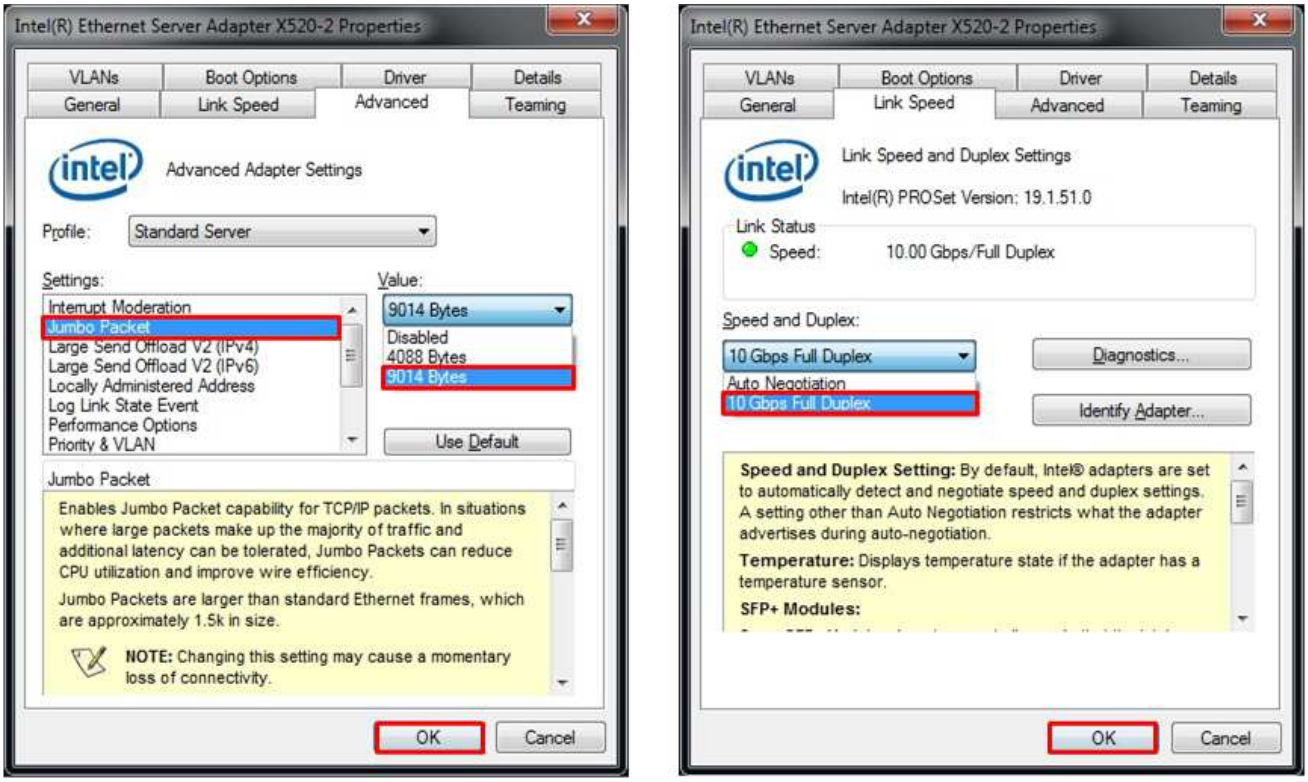

Figure 3-3 Link speed and Jumbo frame setup

- On Advanced Tab, select “Jumbo Packet” and then set Value to “9014 Bytes” for Jumbo Frame support or set value to “Disabled” for non-Jumbo Frame support, as shown in left window of Figure 3-3.
- On Link Speed, select “10 Gbps Full Duplex” for running 10-Gigabit transfer test, as shown in right window of Figure 3-3.

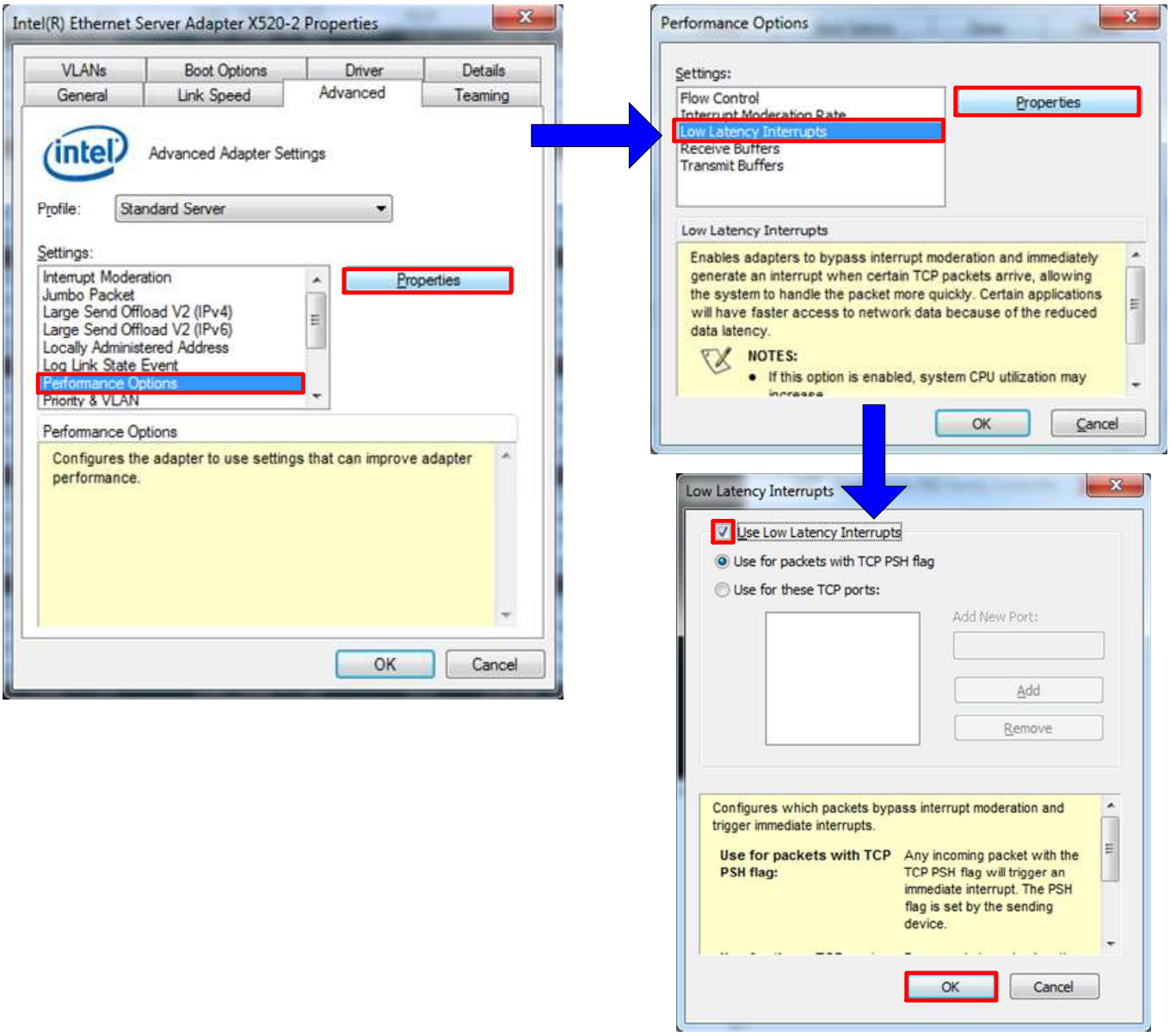

Figure 3-4 Performance Options

- On Advanced Tab, select “Performance Options” and click “Properties” button.
- On “Performance Options” window, select “Low Latency Interrupts” and click “Properties” button.
- On “Low Latency Interrupts” window, select “Use Low Latency Interrupts” and click “OK” button.
- Click “OK” button to save and exit all setting windows.

3.3 Power Option Setting

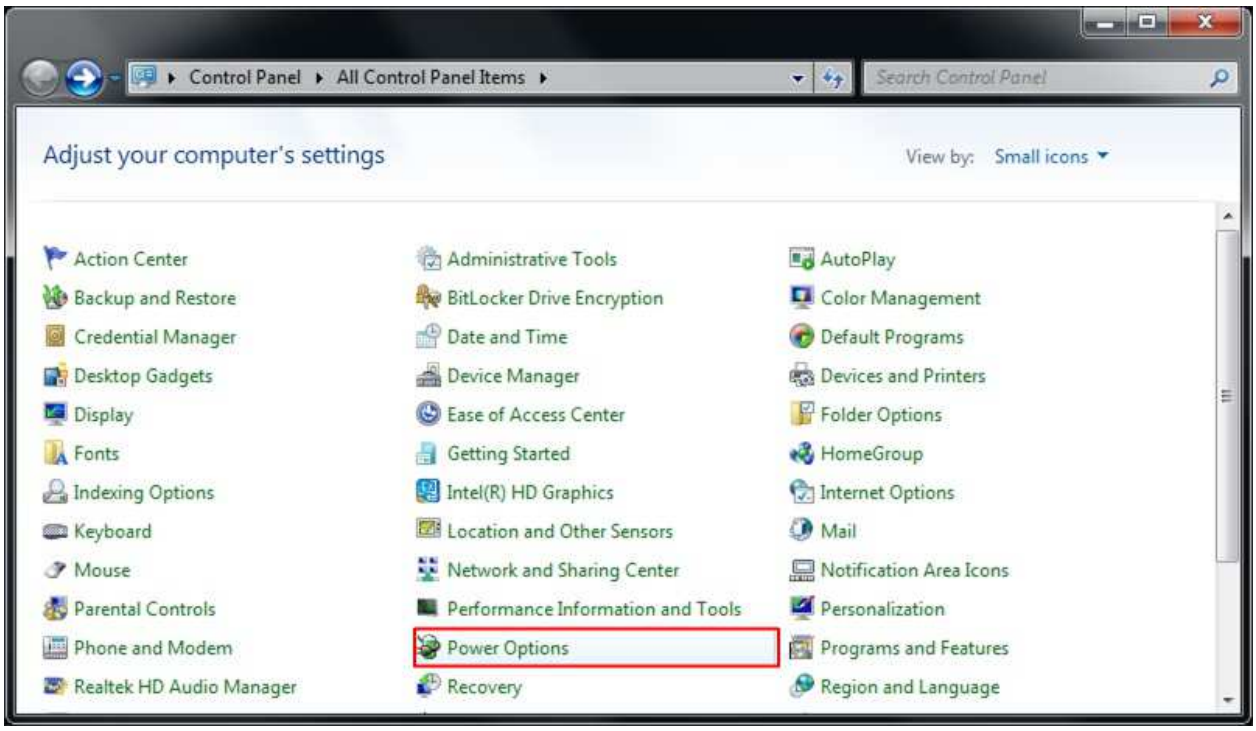

Figure 3-5 Power Options

- Open Control Panel and select Power Options as shown in Figure 3-5.
- Change setting to High Performance as shown in Figure 3-6.

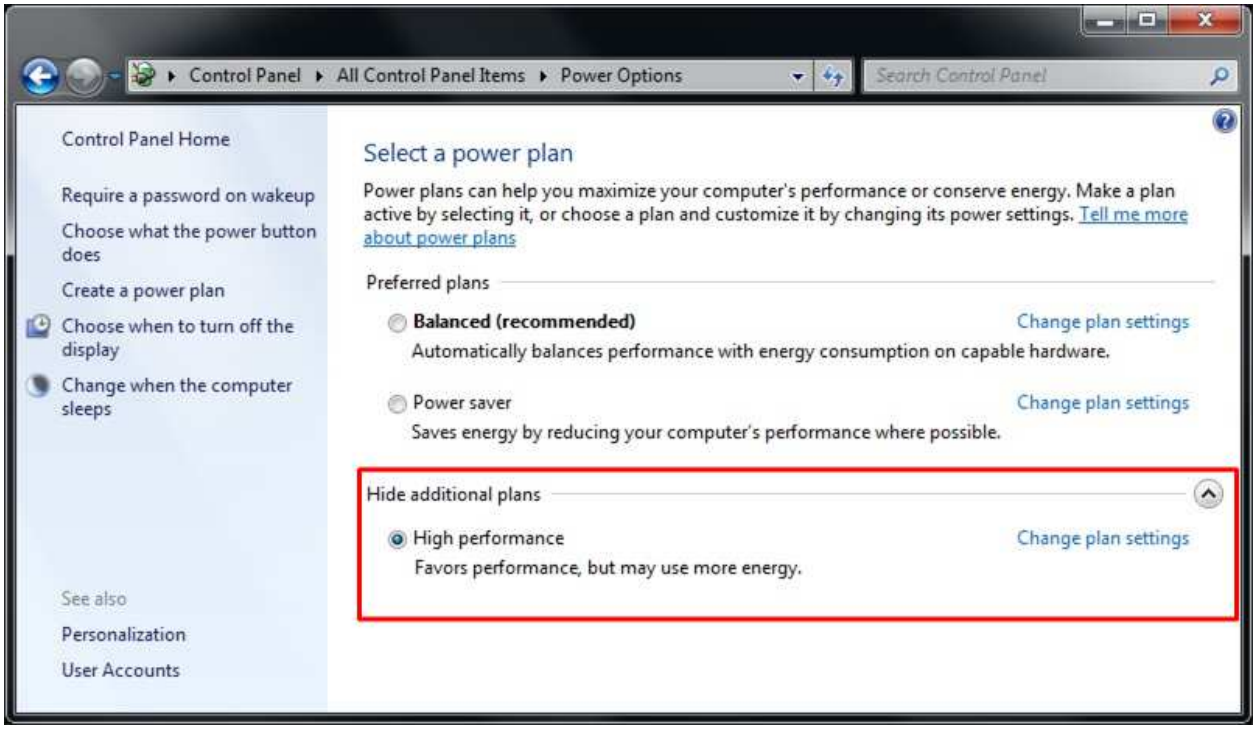

Figure 3-6 High Performance Option

4 How to run demo

Both Sending and Receiving demo requires same steps to set up hardware as follows.

- Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.

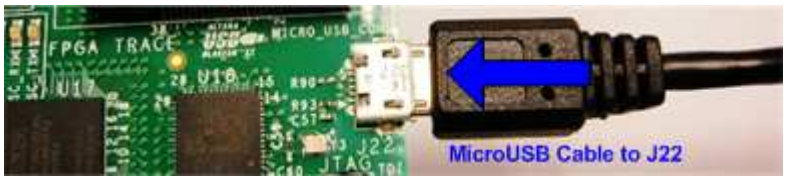

Figure 4-1 MicroUSB connection

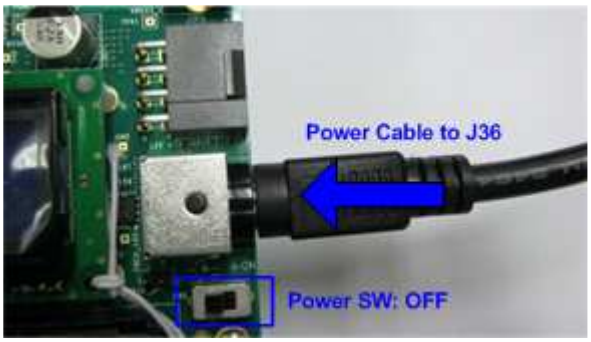

Figure 4-2 Power cable connection

- Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between SFP+ Port A and PC.

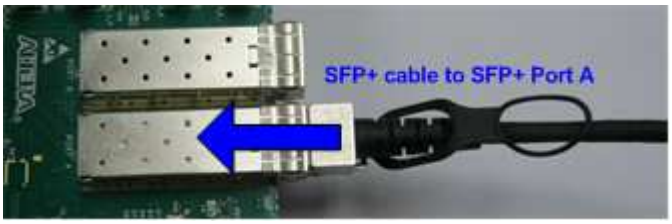

Figure 4-3 SFP+ cable connection

- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.

- Open “Clock Controller” application which is provided in Arria10 SoC release package. Select Si5338(U50) tab, and set CLK3 value to be “322.265625”. Click “Set” button to program clock to be 322.265625 MHz, as shown in Figure 4-4.

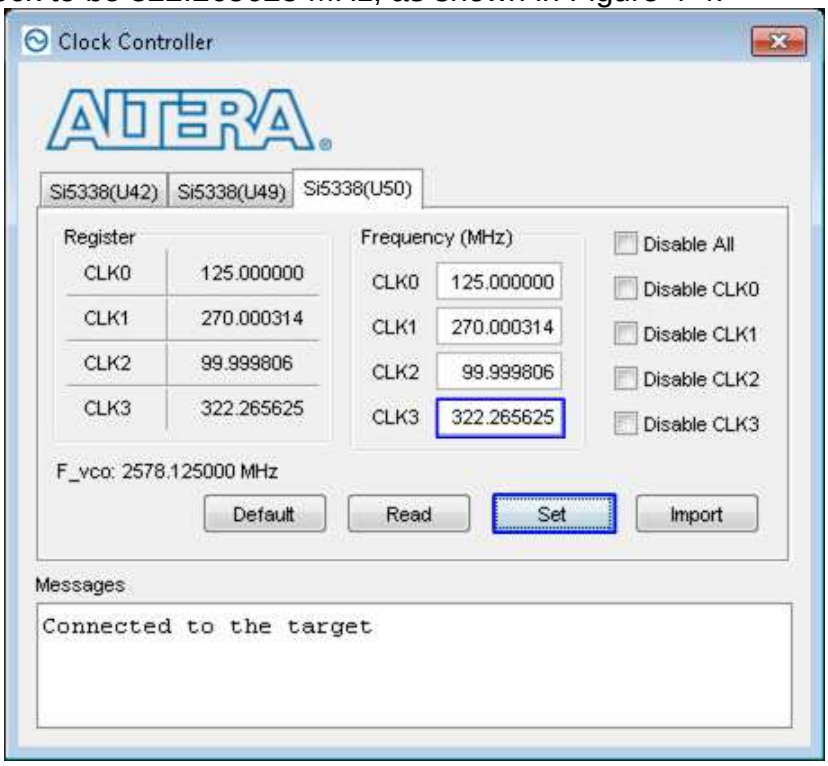

Figure 4-4 Reference clock programming

- Open Quartus Programmer, select SOF file, and program file to FPGA development board, as shown in Figure 4-5.

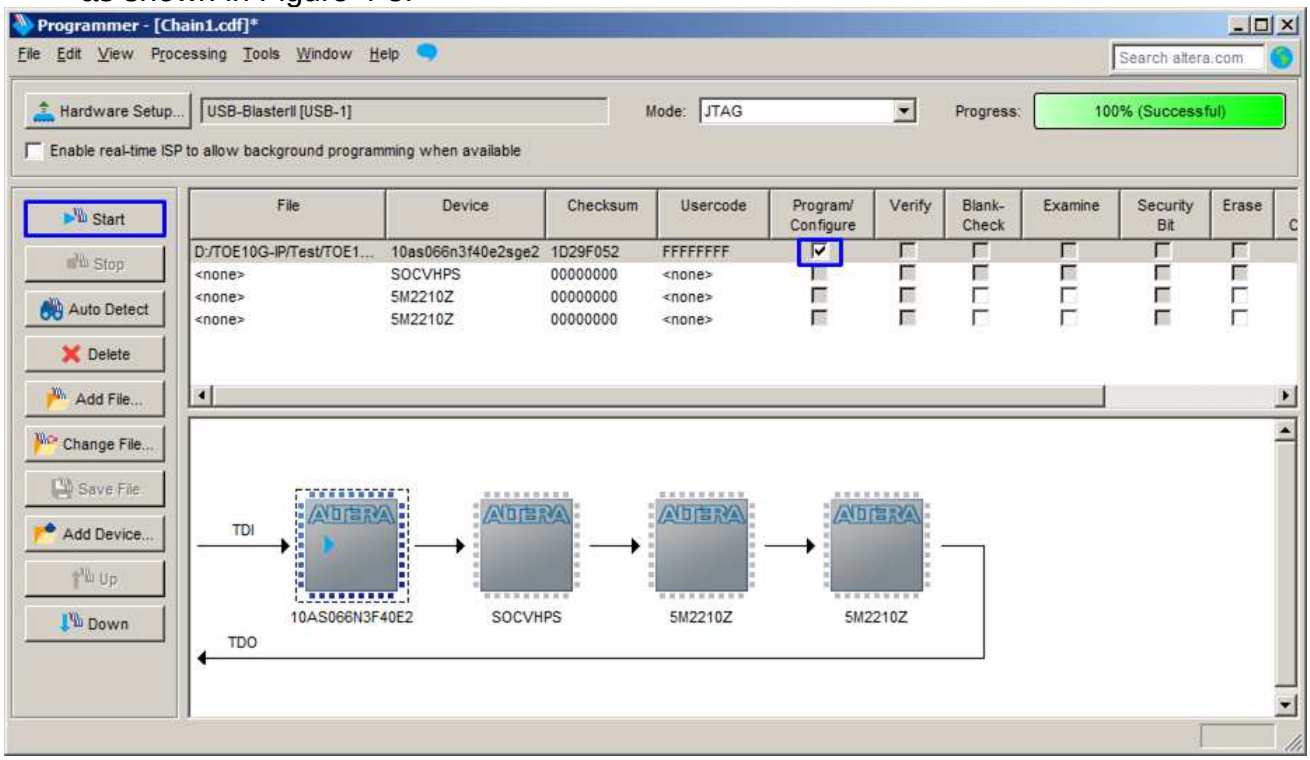

Figure 4-5 Program SOF File

- Since the reference design uses evaluation IP of 10G EMAC, warning message will be displayed after programming completely as shown in Figure 4-6. Reference design can run about 20 mins.

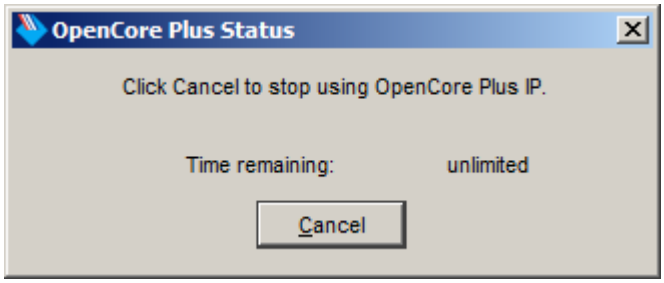

Figure 4-6 Warning message of OpenCore Plus IP

- Press StartSW at S3 position (as shown in Figure 2-3) to initialize parameter in system, and then LED0 will turn on, as shown in Figure 4-7 and Figure 4-8 following DIPSW bit0 setting.

Figure 4-7 LED Status after push StartSW when DIPSW[0]=ON (Non-Jumbo frame)

Figure 4-8 LED Status after push StartSW when DIPSW[0]=OFF (Jumbo frame)

Now system is ready to transfer data. The step to test Sending and Receiving data is described in the next topic.

Note: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.

4.1 Run Sending Demo

Sending demo runs in forever loop and user needs to cancel the application to stop the test.

4.1.1 Non-Jumbo frame mode

- Set DIPSW[1] = ON to run Sending demo.
- Set DIPSW[0] = ON and confirm that LED2 status is OFF.
- Open “command prompt” on PC, and run “recv_tcp_client_10G” test application by following command
  >> recv_tcp_client_10G <FPGA IP address> <FPGA port number> <number of data in packet>
  For example,
  >> recv_tcp_client_10G 192.168.7.42 4000 1456
  Note: This demo fixes IP address, port number, and data transfer size. So, please do not change any value without HDL code modification.
- Test application displays current numbers of packet, and time usage with performance is displayed at the end of each loop transfer, as shown in Figure 4-9.
- User can cancel operation by pressing “Ctrl+C”.

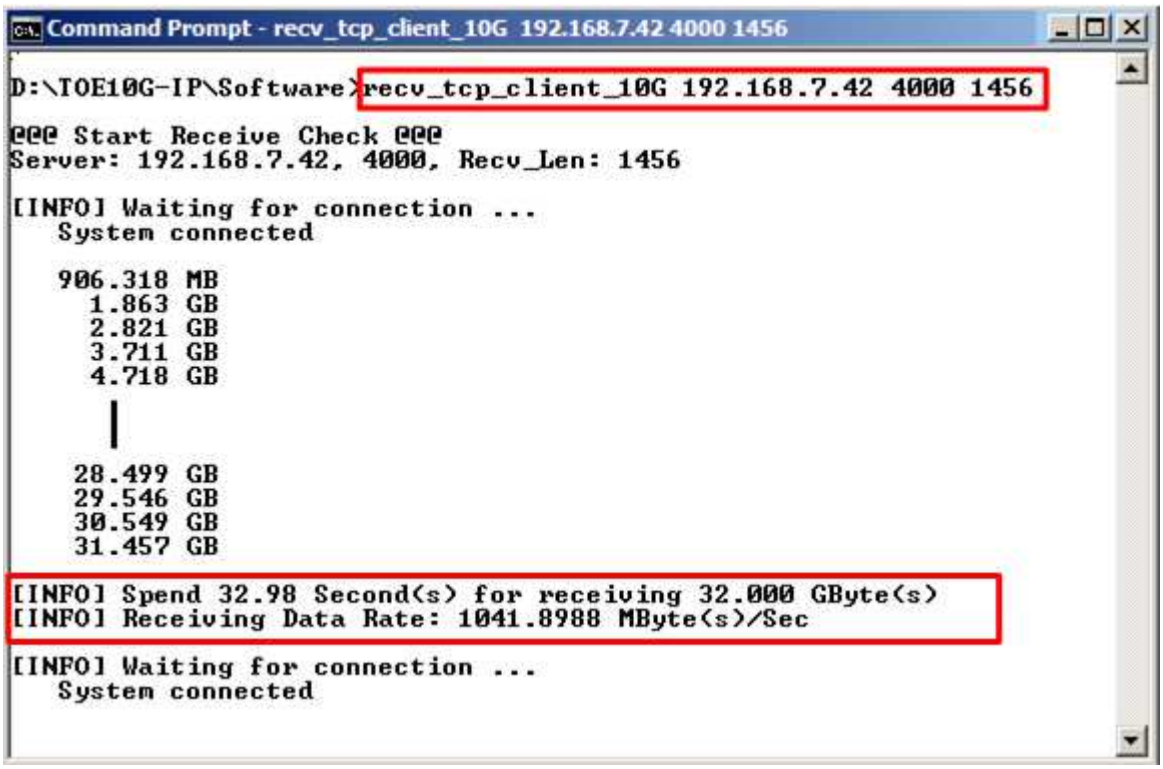

Figure 4-9 Non-Jumbo frame Sending Demo

Figure 4-10 LED Status during running Sending Demo with Non-Jumbo frame

4.1.2 Jumbo frame mode

- Set DIPSW[1] = ON to run Sending demo.
- Set DIPSW[0] = OFF and confirm that LED2 status is ON.
- Open “command prompt” on PC, and run “recv_tcp_client_10G” test application by following command
  >> recv_tcp_client_10G 192.168.7.42 4000 8960
  Note: This demo fixes IP address, port number, and data transfer size. So, please do not change any value without HDL code modification.
- Message during test application and how to cancel operation are similar to Non-Jumbo frame mode.

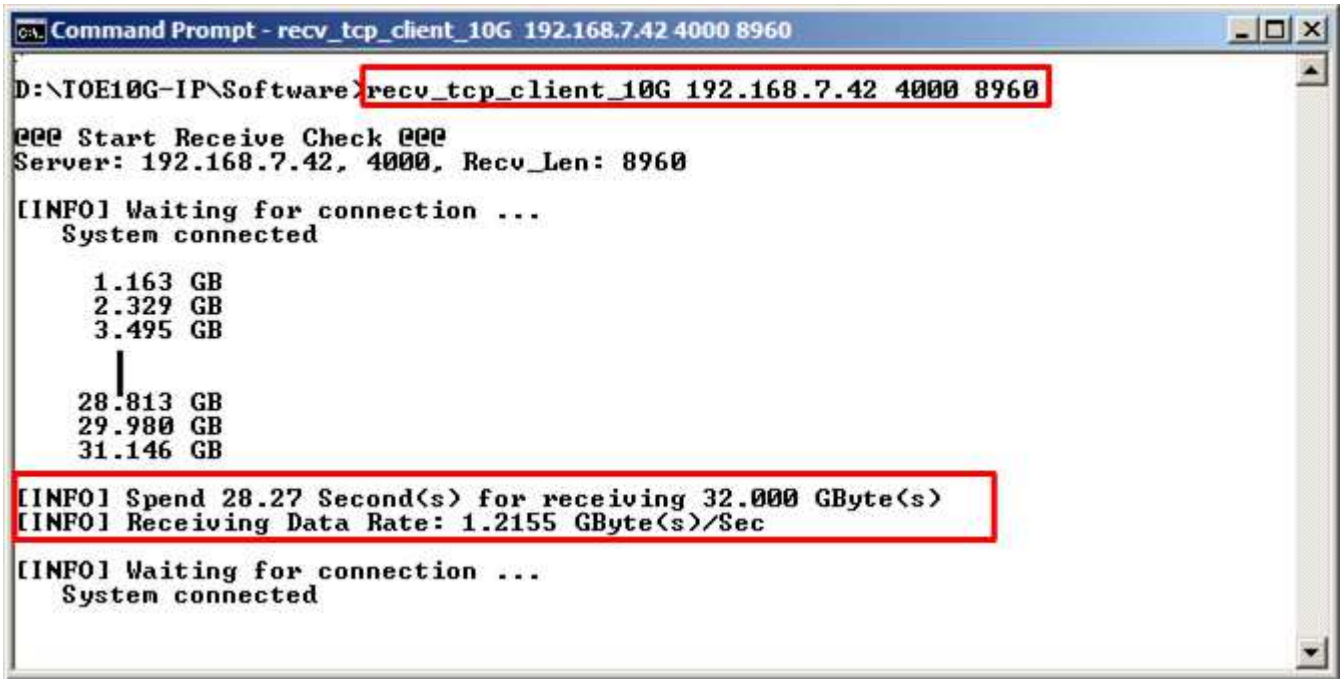

Figure 4-11 Jumbo frame Sending Demo

Figure 4-12 LED Status when running Sending Demo with Jumbo frame

4.2 Run Receiving Demo

4.2.1 Performance test mode

- Set DIPSW[1] = OFF to run Receiving demo.
- Set DIPSW[2] = ON to disable verification module.
- Open “command prompt” on PC, and run “send_tcp_client_10G” test application by following command
  >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without HDL code modification.
  - User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
  - Mode: ‘0’- All ‘0’ patterns are sent for performance test.

  For example,
  >> send_tcp_client_10G 192.168.7.42 4000 559241 0

- Test application displays “…” during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 4-14.

Figure 4-13 Command line for receiving demo on Performance test mode

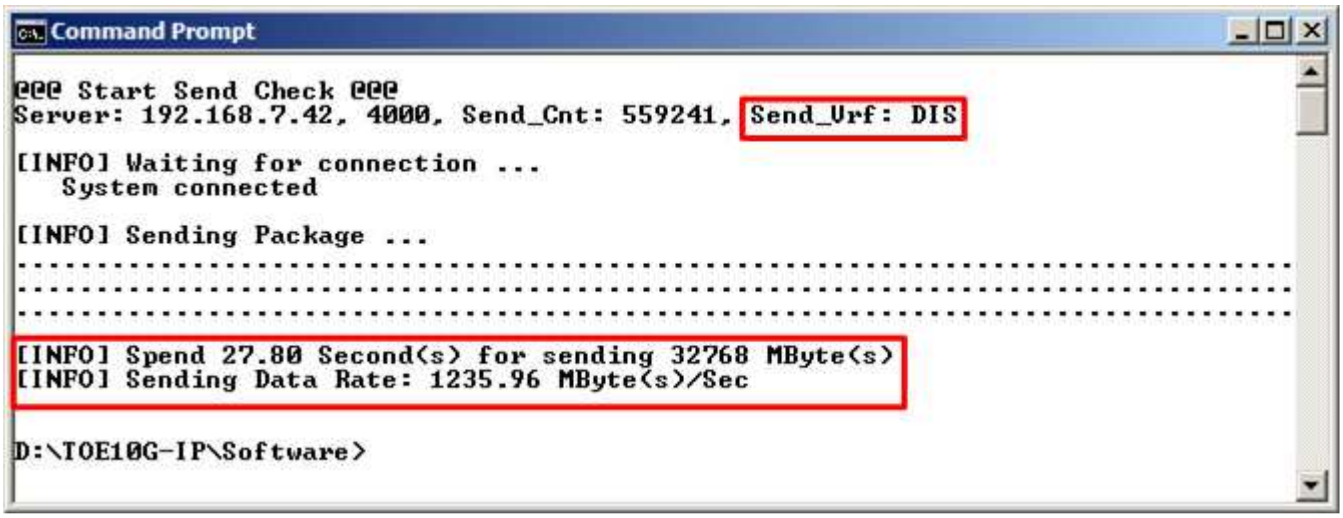

Figure 4-14 Receiving Demo on Performance test mode

4.2.2 Verification mode

- Set DIPSW[2] = OFF to run Receiving demo.
- Set DIPSW[3] = OFF to enable verification module.
- Open “command prompt” on PC, and run “send_tcp_client_10G” test application by following command
  >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without HDL code modification.
  - User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
  - Mode: ‘1’- 32-bit increment data are sent for data verification.

  For example,
  >> send_tcp_client_10G 192.168.7.42 4000 559241 1
- Test application displays “…” during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 4-16.
- LED3 will blink if any error data detects from Verification module.

Figure 4-15 Command line for receiving demo on Verification mode

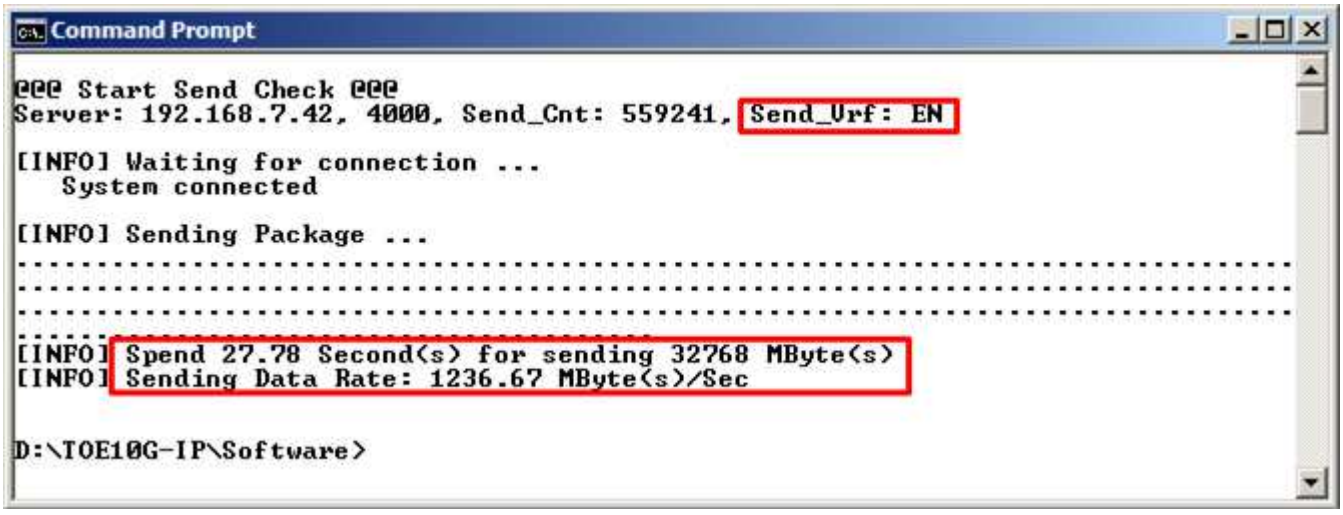

Figure 4-16 Receiving Demo on Verification mode

5 Revision History

Revision	Date	Description
1.0	19-May-16	Initial version release
1.1	18-Nov-16	Update Figure 1-1