

# **TOE10G-IP Demo Instruction**

Rev1.2 24-Aug-15

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between FPGA development board and PC through 10Gigabit Ethernet. This demo can select to run with supported and unsupported Jumbo frame PC.

# 1 Environment Setup

As shown in Figure 1 - Figure 3, to run TOE10G-IP standard demo, please prepare

- 1) FPGA Development board (KC705/VC707/ZC706)
- 2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
- 3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
- 4) micro USB cable for programming FPGA between FPGA Development board and PC
- 5) "send\_tcp\_client\_10G.exe" and "recv\_tcp\_client\_10G.exe", provided by Design Gateway, which are test application available on PC



Figure 1 TOE10G-IP Demo Environment Setup on KC705





Figure 3 TOE10G-IP Demo Environment Setup on ZC706

Note: Test result in this document is captured by using following test environment.

- [1] 10G Network Adapter: Intel X520-DA2 <u>http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/</u> <u>ethernet-x520-server-adapters-brief.html</u>
- [2] 10-Gigabit SFP+ DAC cable http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx
   [2] DO Mathedrated ACHO HOLES ACCESSION (2019)
- [3] PC: Motherboard ASUS H87M-E, 8 GB RAM, 64-bit Windows7 OS



# 2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC and different DIPSW setting on FPGA development board. The definition of DIPSW and LED on FPGA development board are described in Table 1 and Table 2.

#### Table 1 DIPSW Setting Definition

DIPSW	OFF	ON
Bit 1	Sending mode by using non-Jumbo frame	Sending mode by using Jumbo frame
	(1456 bytes)	(8960 bytes)
Bit 2	Sending mode	Receiving mode
Bit 3	Receiving mode without data verification	Receiving mode with data verification

#### Table 2 LED Definition

GPIO LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (CenterSW) has already been pressed and confirm IP address setting on PC that is correct.
1/R	BLINK: Operation timeout	Normal operation
2/C	Sending mode in jumbo frame	Sending mode in non-jumbo frame
3/L	BLINK: Data verification is fail in receiving mode ON: Port is established	No operation

Note:

- DIPSW setting must not be changed during operation in processing.

More details about each test mode are follows.



#### 2.1 Sending mode

In this mode, 32 GB data will be transferred from FPGA development board to PC, and "recv\_tcp\_client\_10G.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select 2 transfer packet sizes by DIPSW[1] setting, i.e. 1456 data byte for running with unsupported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting by monitoring LED2/C status.

The operation sequence for sending mode is follows.

- 1) TOE10G-IP within FPGA development board initializes parameters in system such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
- 2) Test application on PC opens connection to connect with FPGA development board, and then waits data sending.
- 3) TOE10G-IP starts to send 32 GB data to PC while PC verifies received data that is correct.
- 4) After all data are transferred, TOE10G-IP sends packet to close connection.
- 5) PC sends acknowledgement to close connection. Then, operation will repeat from Step2) to Step5) until operation cancelled.

#### 2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By running "send\_tcp\_client\_10G.exe" application on PC, data will be sent out until total numbers of transferred data equal to setting value. This test can run in 2 modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC to reduce PC task and run in the best performance condition. Verification module within FPGA development board will be OFF to not verify dummy data from PC.

In data verification mode, 32-bit increment data will be generated from PC to check data reliability. Verification module within FPGA will be ON to verify all received data. LED error will blink if any error is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can set the option in command line to ON/OFF test pattern generator.

The operation sequence for receiving mode is follows.

- 1) Similar to Step 1) in Sending mode.
- 2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
- 3) TOE10G-IP receives data and verifies data if enable.
- 4) After all data are transferred, Test application sends packet to close connection.
- 5) TOE10G-IP sends acknowledgement to close connection. This mode will run only one time, not in loop like Sending mode.



# 3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

# 3.1 IP Setting

Connect using: 10-Gb LAN connection	You can get IP settings assigned	automatically if your network supports
Market Server Adapter X520-2	for the appropriate IP settings,	eed to ask your network administrator
Configure	Obtain an IP address autom	atically
his connection uses the following items:	<ul> <li>Use the following IP address</li> </ul>	51
✓ Client for Microsoft Networks ✓ Boos Packet Scheduler	IP address:	192.168.7.25
Brile and Printer Sharing for Microsoft Networks	Subnet mask:	255 . 255 . 255 . 0
	Default gateway:	e
Link-Layer Topology Discovery Mapper I/O Driver	Obtain DNS server address	automatically
	Use the following DNS serve	r addresses:
Install Properties	Preferred DNS server:	
Description	Alternate DNS server:	
Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication		
somes diverse interconnected natworks	Validate settings upon exit	Advanced
acioss diverse interconnected networks.		

Figure 4 IPv4 Setting

- Open Local Area Connection Properties of 10-Gb connection, as shown in left window of Figure 4.
- Select "TCP/IPv4" and then click Properties.
- Set IP address = 192.168.7.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 4.



# 3.2 Speed and Frame Setting

H Local Area Connection 2 Properties	Local Area Connection 2
Networking     Sharing       Connect using:	You have made changes to the properties of this connection. If you proceed your changes will be lost. Do you wish to proceed?
This connection uses the following items: Client for Microsoft Networks QoS Packet Scheduler File and Printer Sharing for Microsoft Networks File and Printer Sharing for Microsoft	<u>Y</u> es <u>No</u>
Install Uninstall Properties Description Allows your computer to access resources on a Microsoft network. OK Cancel	

Figure 5 Network Configure

- On Local Area Connection Properties window, click "Configure" as shown in Figure 5.



A PULLAS	Boot Options	Driver	Details	VLANs	Boot Options	Driver	Details
General	Link Speed	Advanced	Teaming	General	Link Speed	Advanced	Teaming
ofile: Sta	Advanced Adapter Se ndard Server	ttings		Link Status Speed:	Link Speed and Duples Intel(R) PROSet Versio 10.00 Gbps/Full	x Settings n: 19.1.51.0 Duplex	
nterrupt Moder umbo Packet	ation	A 9014 Bytes	-	Speed and Du	olex:		
arge Send Off arge Send Off	load V2 (IPv4) load V2 (IPv6)	E 4088 Bytes		10 Gbps Full [	)uplex 👻	<u>D</u> iagno	stics
ocally Adminis og Link State erformance Op nority & VLAN	tered Address Event ptions	• Use	Default	Auto Negotiati 10 Gbps Full 0	on Jupiex	Identify /	∖dapter
umbo Packet				Speed and	Duplex Setting: By de	fault, Intel® adapte	rs are set
Enables Jumb where large p	o Packet capability for backets make up the ma	TCP/IP packets. In si ajority of traffic and	tuations	A setting oth advertises d	er than Auto Negotiation uring auto-negotiation.	restricts what the	adapter
CPU utilization	and improve wire effi	ciency.	educe	Temperature	re: Displays temperatur	e state if the adapt	er has a
Jumbo Packet	s are larger than stand	lard Ethernet frames	, which	SFP+ Modu	les:		
	E: Changing this setting	g may cause a mome	entary				

Figure 6 Link speed and Jumbo frame setup

- On Advanced Tab, select "Jumbo Packet" and then set Value to "9014 Bytes" for Jumbo Frame support or set value to "Disabled" for non-Jumbo Frame support, as shown in left window of Figure 6.
- On Link Speed, select "10 Gbps Full Duplex" for running 10-Gigabit transfer test, as shown in right window of Figure 6.



VLANs	Boot Options	Driver	Details	Sett	nas:	
eneral	Link Speed Advanced Adapter Se	Advanced ttings	Teaming	Flot Inter Rec Tra	v Control rrupt Moderation Rate Latency Interrupts eive Buffers nsmit Buffers	Propertie
Sta	andard Server	•		Lov	Latency Interrupts	munt moderation and immedia
pt Moder o Packet Send Off Send Off ly Adminis ink State manuel 0 y & VLAN	ration Noad V2 (IPv4) Noad V2 (IPv6) tered Address Event Nons		perties	ga th w da	Increases	ain TCP packets arrive, allow more quickly. Certain applica ork data because of the redu led, system CPU utilization ma
figuree th	ptions	on that can improve	adaptar			
figures the	ptions le adapter to use settin	gs that can improve	adapter *		w Latency Interrupts	
ifigures the	ptions le adapter to use settin	gs that can improve	adapter	Lo	w Latency Interrupts Use Low Latency Interrupt Use for packets with TCP P: Use for these TCP ports:	SH flag Add New Port:
figures the	ptions le adapter to use settin	gs that can improve	adapter	Lo	w Latency Interrupts Use Low Latency Interrupt Use for packets with TCP P Use for these TCP ports:	SH flag Add New Port: Add Remove
figures th formance	ptions le adapter to use settin	gs that can improve	adapter		W Latency Interrupts Use Low Latency Interrupt Use for packets with TCP Pi Use for these TCP ports: Configures which packets byp triager immediate interrupts.	SH flag Add New Port: Add Add Remove Add
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Figure 7 Performance Options

- -
- On Advanced Tab, select "Performance Options" and click "Properties" button. On "Performance Options" window, select "Low Latency Interrupts" and click "Properties" button.
- On "Low Latency Interrupts" window, select "Use Low Latency Interrupts" and click "OK" button.
- Click "OK" button to save and exit all setting windows. -



# 3.3 Power Option Setting

			×
🖉 💽 🗝 📭 🕨 Control Panel 🕨 A	All Control Panel Items 🔸	✓ 4y Search Control Panel	Q
Adjust your computer's sett	ings	View by: Small icons 🔻	
Action Center	Administrative Tools		ŕ
Backup and Restore	BitLocker Drive Encryption	Color Management	
Credential Manager	Date and Time	Default Programs	
Desktop Gadgets	Device Manager	B Devices and Printers	
🜉 Display	Sase of Access Center	🔓 Folder Options	1
K Fonts	🔠 Getting Started	🜏 HomeGroup	
🚇 Indexing Options	🕎 Intel(R) HD Graphics	💮 Internet Options	
Ceyboard Keyboard	Location and Other Sensors	Mail	
J Mouse	Network and Sharing Center	Rotification Area Icons	
🐻 Parental Controls	Performance Information and Tools	Personalization	
Phone and Modem	Power Options	Programs and Features	
👺 Realtek HD Audio Manager	P Recovery	🔗 Region and Language	

Figure 8 Power Options

- Open Control Panel and select Power Options as shown in Figure 8.
- Change setting to High Performance as shown in Figure 9.

Control Paller	
Control Panel Home Require a password on wakeup Choose what the power button does Create a power plan Choose when to turn off the display Change when the computer	Select a power plan Power plans can help you maximize your computer's performance or conserve energy. Make a plan active by selecting it, or choose a plan and customize it by changing its power settings. <u>Tell me more about power plans Preferred plans O Balanced (recommended) Change plan settings Automatically balances performance with energy consumption on capable hardware. O Power caver Change plan settings</u>
See also	Saves energy by reducing your computer's performance where possible. Hide additional plans <ul> <li>High performance</li> <li>Favors performance, but may use more energy.</li> </ul>

#### Figure 9 High Performance Option



# 4 How to run demo

Both Sending and Receiving demo requires same steps to set up hardware as follows.

- Insert jumper to enable SFP+ (J4 for KC705, J17 for ZC706, or J6 for VC707), as shown in Figure 10.



Figure 10 Insert jumper to enable SFP+

- For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 11 - Figure 12.



Figure 11 SW11 setting to configure PS from JTAG on ZC706 board



Figure 12 SW4 setting to use USB-to-JTAG on ZC706 board



- Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.
- Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- Open iMPACT and download bit file to FPGA development board, as shown in Figure 13.

😓 ISE iMPACT (P.68d) - [Boundary Scan]	
<u>File Edit View Operations Output</u> <u>Output</u>	Debug <u>W</u> indow <u>H</u> elp
IMPACT Flows       ↔ □ ⓓ ×         ⊕       Boundary Scan         Boundary Scan       SystemACE         Create PROM File (PROM File Format)         ⊕       B WebTalk Data         IMPACT Processes       ↔ □ ⓓ ×         Available Operations are:	Right click device to select operations
Console	Boundary Scan ↔ □ 륜 ×
<pre>'1': Loading file 'D:/TOE10G_1 done.</pre>	IP/Test/2014.1/SFPOnBoard/TOE10GTest_VC

Figure 13 Programmer Environment



- Press StartSW at Center-SW as shown in Figure 1 - Figure 3 to initialize parameter in system, and then LED0 will turn on, as shown in Figure 14 and Figure 15 following DIPSW[1] setting.



Now system is ready to transfer data. The step to test Sending and Receiving data is described in the next topic.

<u>Note</u>: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.



# 4.1 Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test.

- 4.1.1 Non-Jumbo frame mode
  - Set DIPSW[2] = OFF to run Sending demo.
  - Set DIPSW[1] = OFF and confirm that LED2/C status is OFF.
  - Open "command prompt" on PC, and run "recv\_tcp\_client\_10G" test application by following command

>> recv\_tcp\_client\_10G <FPGA IP address> <FPGA port number> <number of data in packet>

For example,

>> recv\_tcp\_client\_10G 192.168.7.42 4000 1456

Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without HDL code modification.

- Test application displays current numbers of packet, and time usage with performance is displayed at the end of each loop transfer, as shown in Figure 16.
- User can cancel operation by pressing "Ctrl+C".



Figure 17 LED Status when running Sending Demo with Non-Jumbo frame



# 4.1.2 Jumbo frame mode

- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = ON and confirm that LED2/C status is ON.
- Open "command prompt" on PC, and run "recv\_tcp\_client\_10G" test application by following command

>> recv\_tcp\_client\_10G 192.168.7.42 4000 8960

Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without HDL code modification.

- Message during test application and how to cancel operation are similar to Non-Jumbo frame mode.

Administrator: C:\Windows\system32\cmd.exe - recv_tcp_client_10G 192.168.7.42 4000 8960	
C:\SW.recv_tcp_client_10G 192.168.7.42 4000 8960	*
CCC Start Receive Check CCC Server: 192.168.7.42, 4000, Recv_Len: 8960	
[INFO] Waiting for connection System connected	=
1.059 GB 2.169 GB 3.257 GB	
28.759 GB 29.877 GB 30.991 GB	
[INFO] Spend 29.94 Second(s) for receiving 34359.736 MByte(s) [INFO] Receiving Data Rate: 1147.6964 MByte(s)/Sec	
[INFO] Waiting for connection System connected	
1.113 GB 2.215 GB 3.332 GB 4.209 GB	
5.319 GB 6.422 GB	-

Figure 18 Jumbo frame Sending Demo



Figure 19 LED Status when running Sending Demo with Jumbo frame

# 4.2 Run Receiving Demo

- 4.2.1 Performance test mode
  - Set DIPSW[2] = ON to run Receiving demo.
  - Set DIPSW[3] = OFF to disable verification module.
  - Open "command prompt" on PC, and run "send\_tcp\_client\_10G" test application by following command

>> send\_tcp\_client\_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>

- Similar to Sending demo, IP address and port number cannot change without HDL code modification.
- User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
- Mode: '0'- All '0' patterns are sent for performance test.

>> send\_tcp\_client\_10G 192.168.7.42 4000 559241 0

- Test application displays "..." during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 21.



Figure 20 Command line for receiving demo on Performance test mode

Administrator: C:\Windows\system32\cmd.exe	
000 Start Send Check 000 Server: 192.168.7.42, 4000, Send_Cnt: 559241, Send_Vrf: DIS	Â
[INFO] Waiting for connection System connected	
[INFO] Sending Package	
[INFO] Spend 29.35 Second(s) for sending 32768 MByte(s)	
THE ST SENATING Data Mate. 1170.01 HByte(\$775ec	+

Figure 21 Receiving Demo on Performance test mode



For example,



# 4.2.2 Verification mode

- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = ON to enable verification module.
- Open "command prompt" on PC, and run "send\_tcp\_client\_10G" test application by following command

>> send\_tcp\_client\_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>

- Similar to Sending demo, IP address and port number cannot change without HDL code modification.
- User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
- o Mode: '1'- 32-bit increment data are sent for data verification.

# For example,

>> send\_tcp\_client\_10G 192.168.7.42 4000 559241 1

- Test application displays "..." during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 23.



Figure 22 Command line for receiving demo on Verification mode

Administrator: C:\Windows\system32\cmd.exe	
CCC Start Send Check CCC Server: 192.168.7.42, 4000, Send_Cnt: 559241, Send_Vrf: EN	â
[INFO] Waiting for connection System connected	
[INFO] Sending Package	
[INFO] Spend 29.82 Second(s) for sending 32768 MByte(s) [INFO] Sending Data Rate: 1152.05 MByte(s)/Sec	
	2

Figure 23 Receiving Demo on Verification mode

- LED3/L will blink if any error data detects from Verification module.



# 5 Revision History

Revision	Date	Description
1.0	05-Sep-14	Initial version release
1.1	10-Nov-14	Add ZC706 support
1.2	24-Aug-15	Add 3.3 Power Option Setting