TOE10G-IP Demo Instruction

Rev1.2 24-Aug-15

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between FPGA development board and PC through 10Gigabit Ethernet. This demo can select to run with supported and unsupported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1 - Figure 3, to run TOE10G-IP standard demo, please prepare

1) FPGA Development board (KC705/VC707/ZC706)
2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
4) micro USB cable for programming FPGA between FPGA Development board and PC
5) “send_tcp_client_10G.exe” and “recv_tcp_client_10G.exe”, provided by Design Gateway, which are test application available on PC

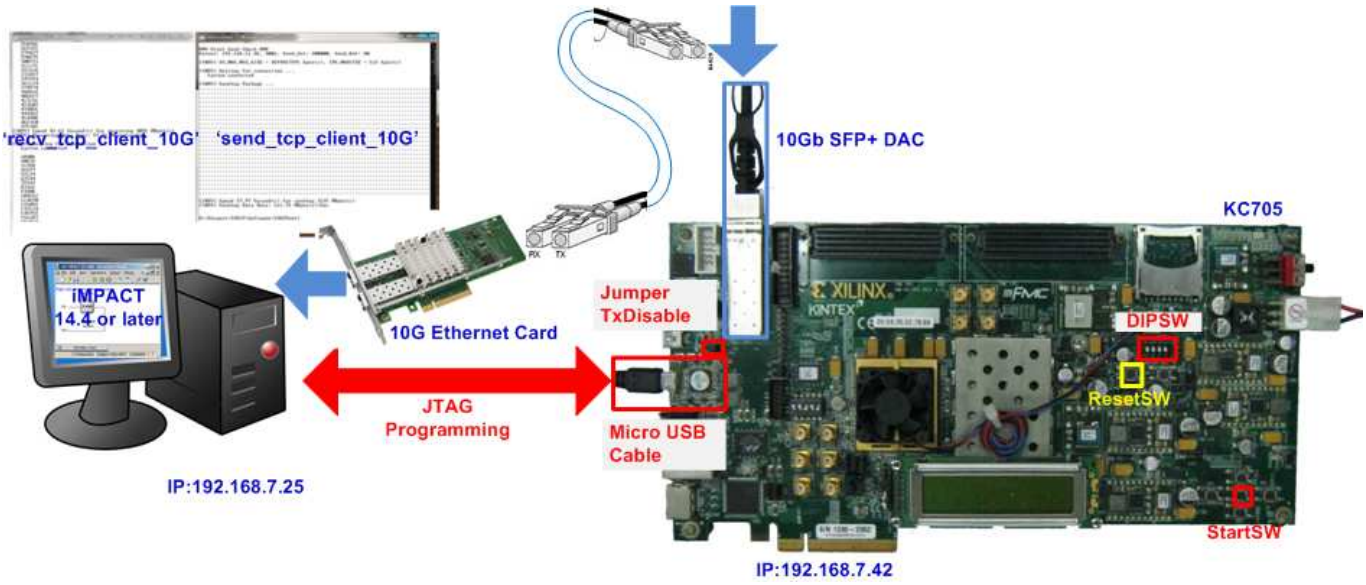

Figure 1 TOE10G-IP Demo Environment Setup on KC705

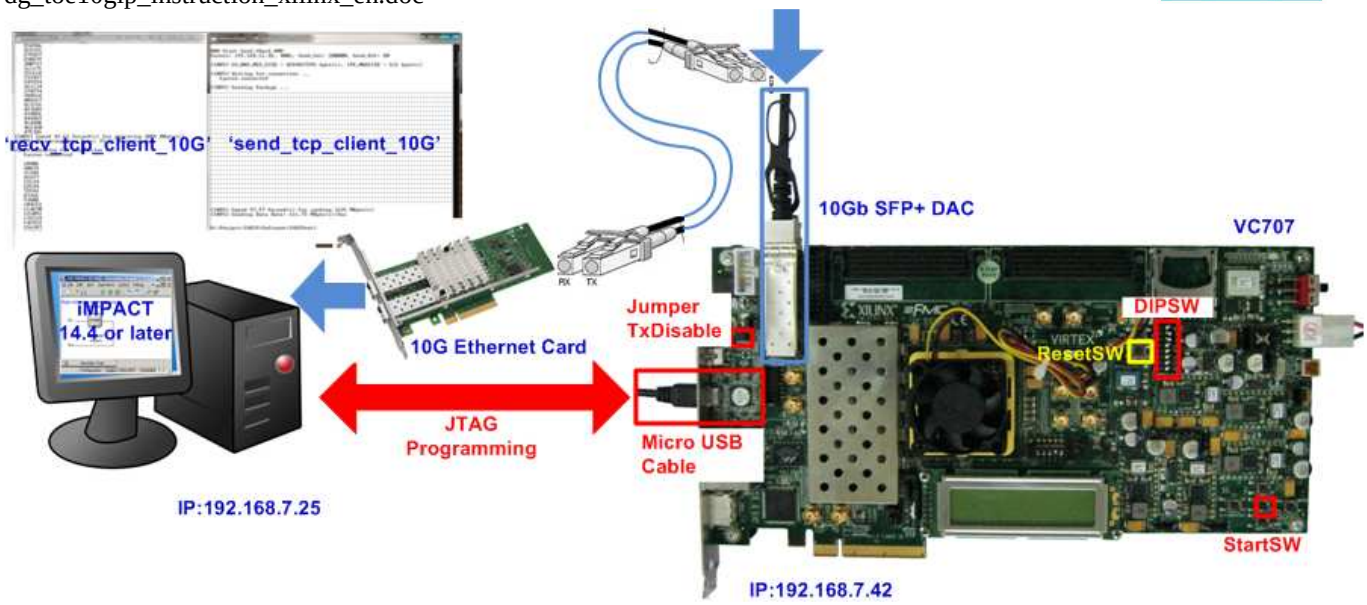

Figure 2 TOE10G-IP Demo Environment Setup on VC707

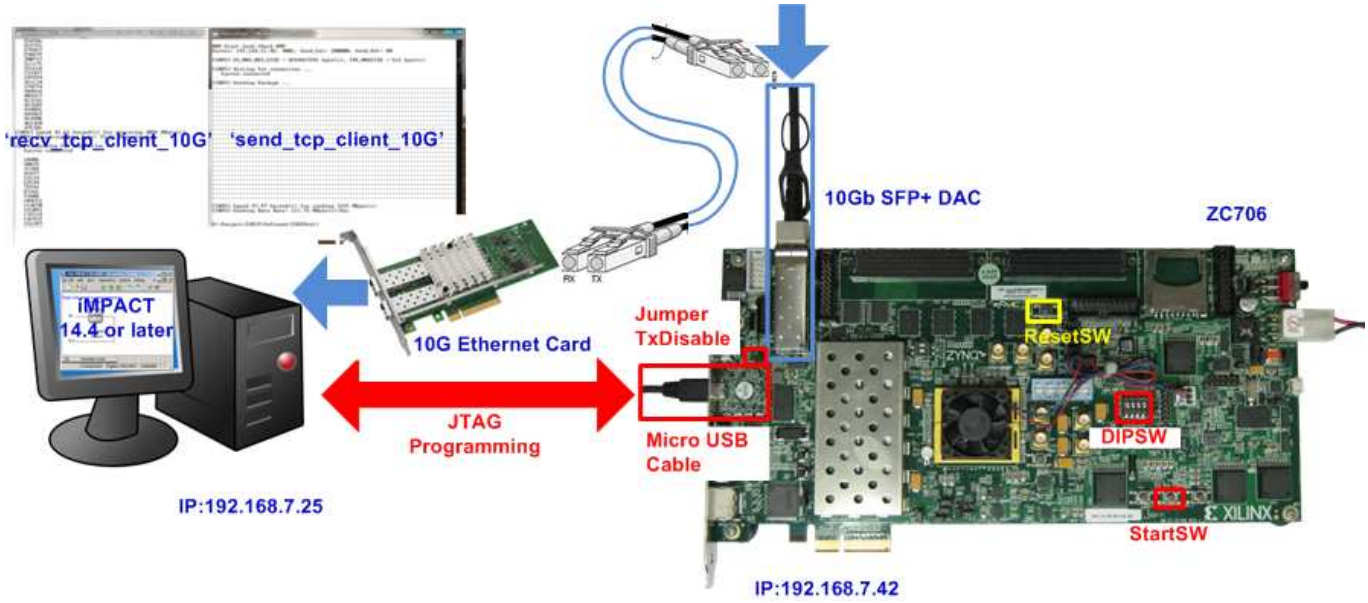

Figure 3 TOE10G-IP Demo Environment Setup on ZC706

Note: Test result in this document is captured by using following test environment.
[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html
[2] 10-Gigabit SFP+ DAC cable
http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx
[3] PC: Motherboard ASUS H87M-E, 8 GB RAM, 64-bit Windows7 OS

2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC and different DIPSW setting on FPGA development board. The definition of DIPSW and LED on FPGA development board are described in Table 1 and Table 2.

Table 1 DIPSW Setting Definition

DIPSW	OFF	ON
Bit 1	Sending mode by using non-Jumbo frame (1456 bytes)	Sending mode by using Jumbo frame (8960 bytes)
Bit 2	Sending mode	Receiving mode
Bit 3	Receiving mode without data verification	Receiving mode with data verification

Table 2 LED Definition

GPIO LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (CenterSW) has already been pressed and confirm IP address setting on PC that is correct.
1/R	BLINK: Operation timeout	Normal operation
2/C	Sending mode in jumbo frame	Sending mode in non-jumbo frame
3/L	BLINK: Data verification is fail in receiving mode ON: Port is established	No operation

Note:
- DIPSW setting must not be changed during operation in processing.

More details about each test mode are follows.

2.1 Sending mode

In this mode, 32 GB data will be transferred from FPGA development board to PC, and "recv_tcp_client_10G.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select 2 transfer packet sizes by DIPSW[1] setting, i.e. 1456 data byte for running with unsupported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting by monitoring LED2/C status.

The operation sequence for sending mode is follows.

1) TOE10G-IP within FPGA development board initializes parameters in system such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
2) Test application on PC opens connection to connect with FPGA development board, and then waits data sending.
3) TOE10G-IP starts to send 32 GB data to PC while PC verifies received data that is correct.
4) After all data are transferred, TOE10G-IP sends packet to close connection.
5) PC sends acknowledgement to close connection. Then, operation will repeat from Step2) to Step5) until operation cancelled.

2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By running "send_tcp_client_10G.exe" application on PC, data will be sent out until total numbers of transferred data equal to setting value. This test can run in 2 modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC to reduce PC task and run in the best performance condition. Verification module within FPGA development board will be OFF to not verify dummy data from PC.
In data verification mode, 32-bit increment data will be generated from PC to check data reliability. Verification module within FPGA will be ON to verify all received data. LED error will blink if any error is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can set the option in command line to ON/OFF test pattern generator.

The operation sequence for receiving mode is follows.

1) Similar to Step 1) in Sending mode.
2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
3) TOE10G-IP receives data and verifies data if enable.
4) After all data are transferred, Test application sends packet to close connection.
5) TOE10G-IP sends acknowledgement to close connection. This mode will run only one time, not in loop like Sending mode.

3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

3.1 IP Setting

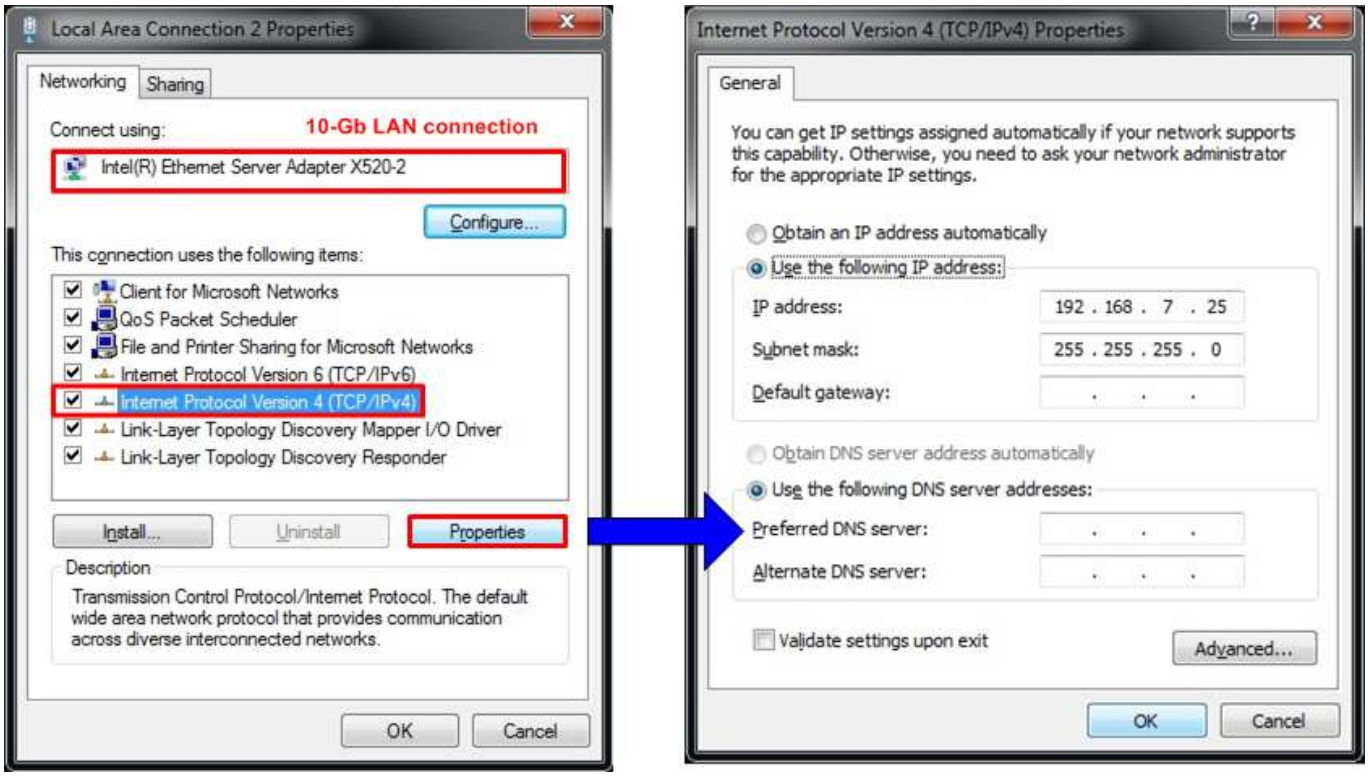

Figure 4 IPv4 Setting

- Open Local Area Connection Properties of 10-Gb connection, as shown in left window of Figure 4.
- Select “TCP/IPv4” and then click Properties.
- Set IP address = 192.168.7.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 4.

3.2 Speed and Frame Setting

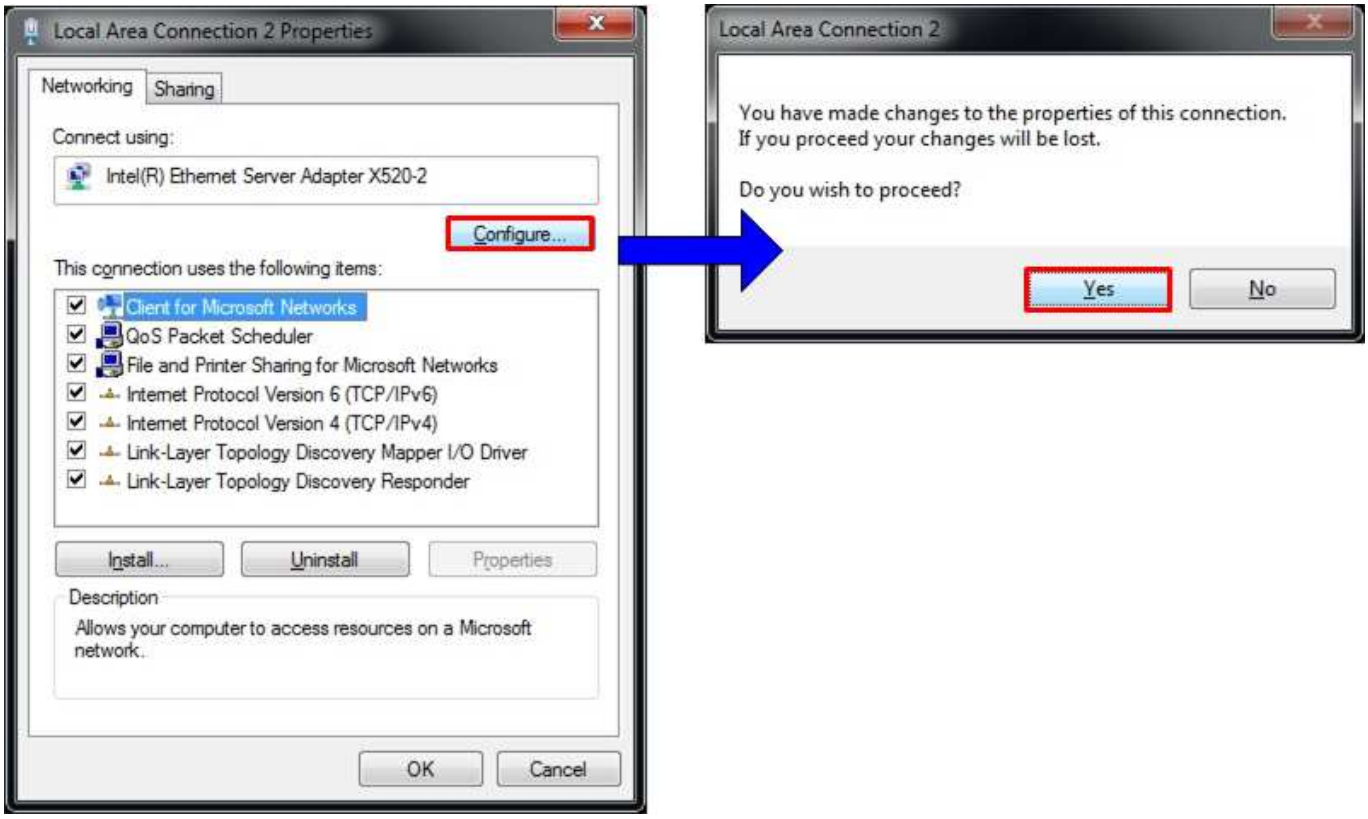

Figure 5 Network Configure

- On Local Area Connection Properties window, click “Configure” as shown in Figure 5.

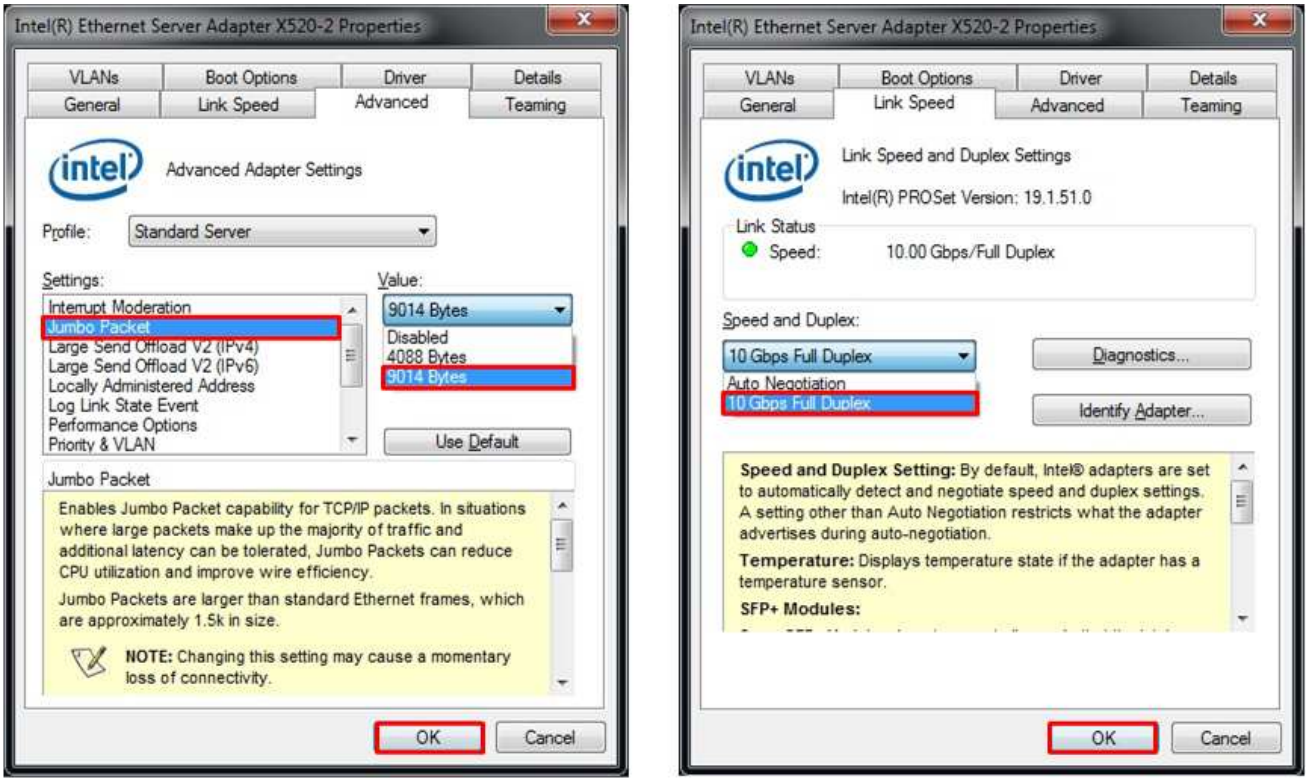

Figure 6 Link speed and Jumbo frame setup

- On Advanced Tab, select “Jumbo Packet” and then set Value to “9014 Bytes” for Jumbo Frame support or set value to “Disabled” for non-Jumbo Frame support, as shown in left window of Figure 6.
- On Link Speed, select “10 Gbps Full Duplex” for running 10-Gigabit transfer test, as shown in right window of Figure 6.

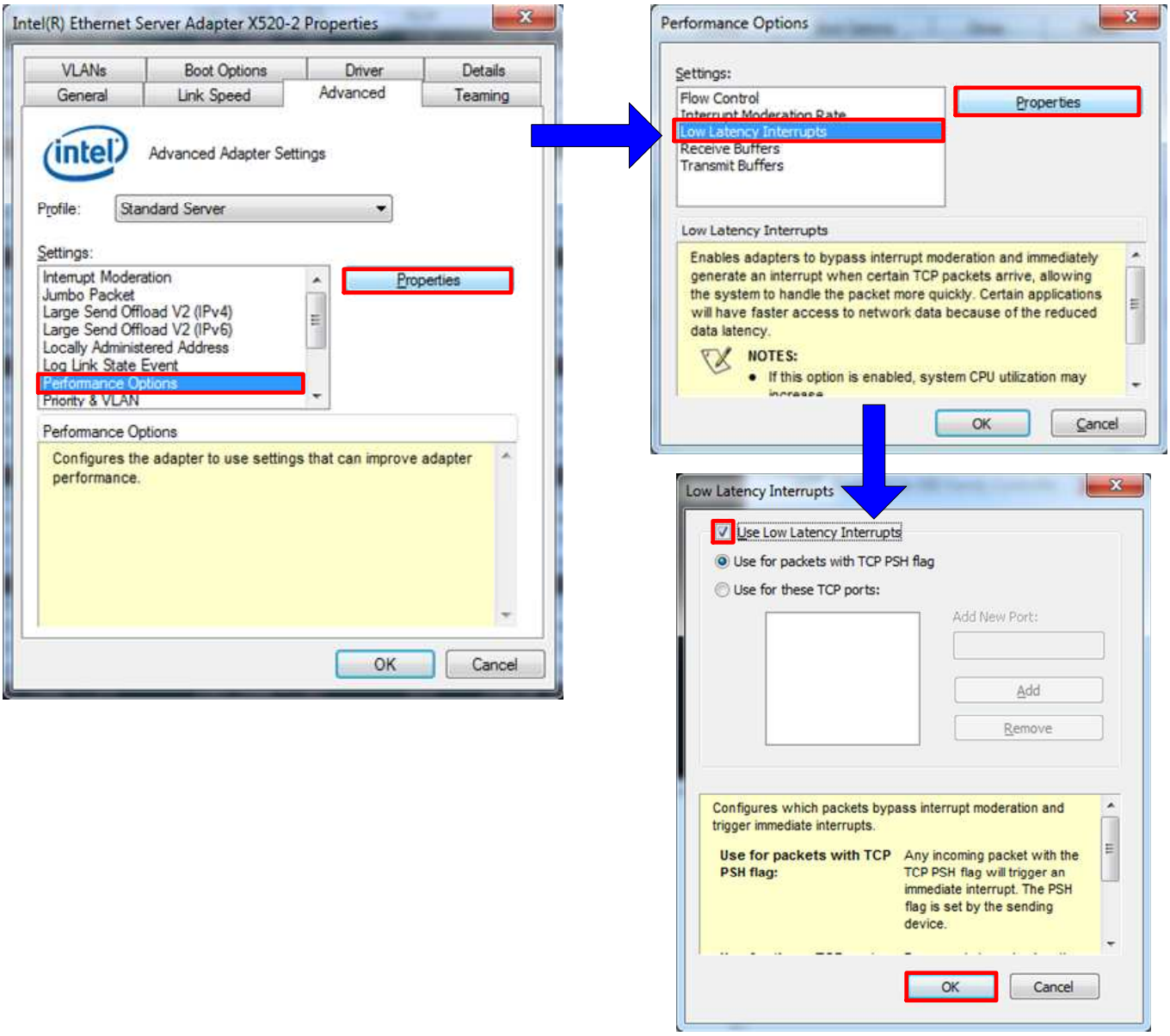

Figure 7 Performance Options

- On Advanced Tab, select “Performance Options” and click “Properties” button.
- On “Performance Options” window, select “Low Latency Interrupts” and click “Properties” button.
- On “Low Latency Interrupts” window, select “Use Low Latency Interrupts” and click “OK” button.
- Click “OK” button to save and exit all setting windows.

3.3 Power Option Setting

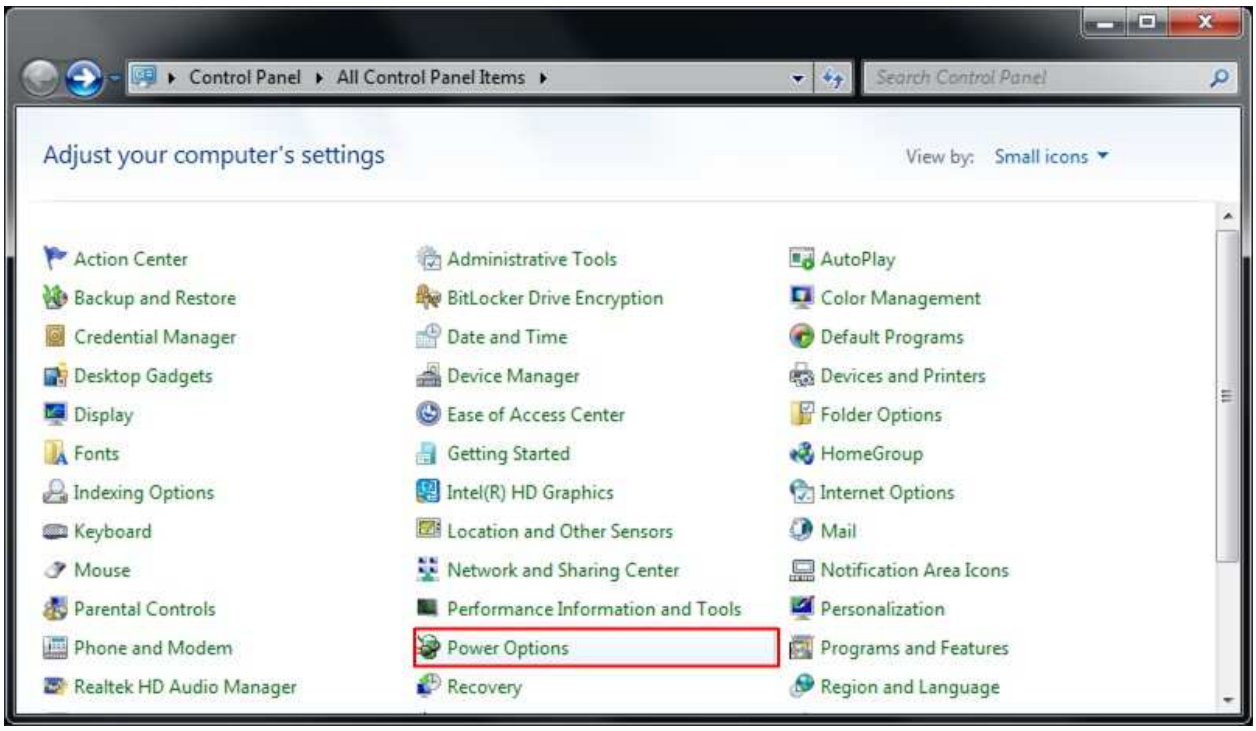

Figure 8 Power Options

- Open Control Panel and select Power Options as shown in Figure 8.
- Change setting to High Performance as shown in Figure 9.

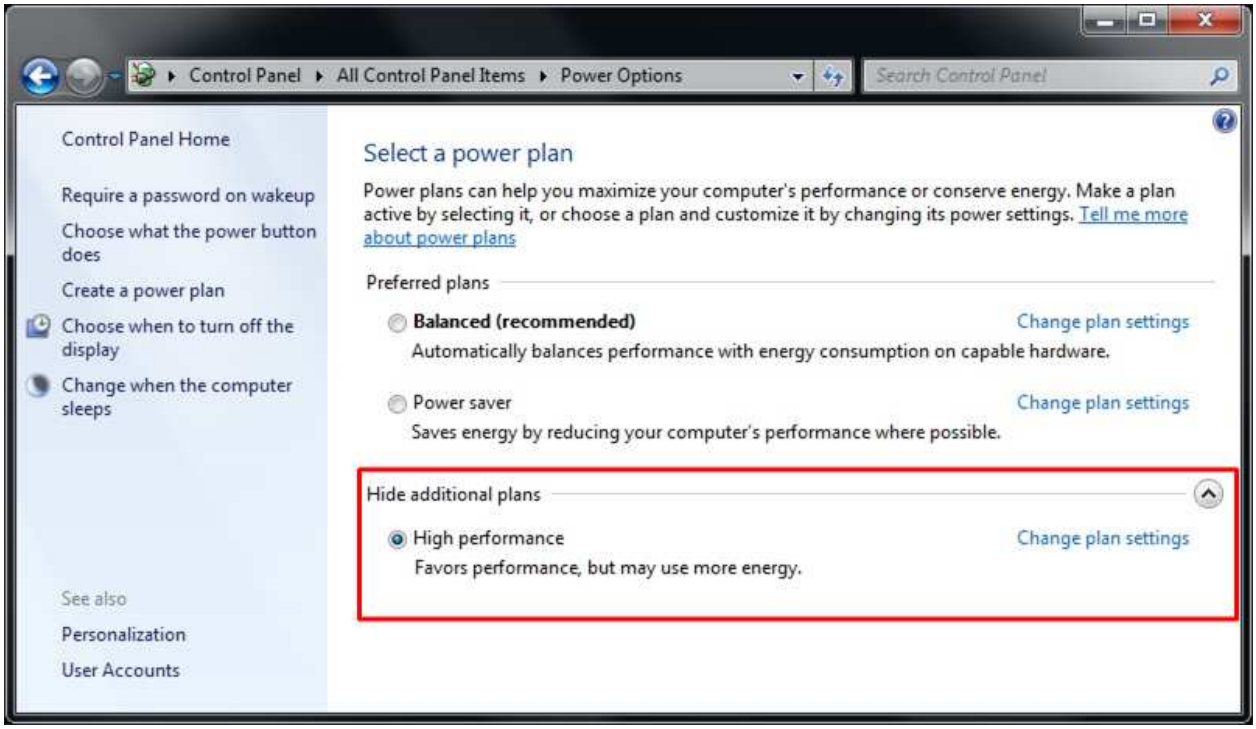

Figure 9 High Performance Option

4 How to run demo

Both Sending and Receiving demo requires same steps to set up hardware as follows.

- Insert jumper to enable SFP+ (J4 for KC705, J17 for ZC706, or J6 for VC707), as shown in Figure 10.

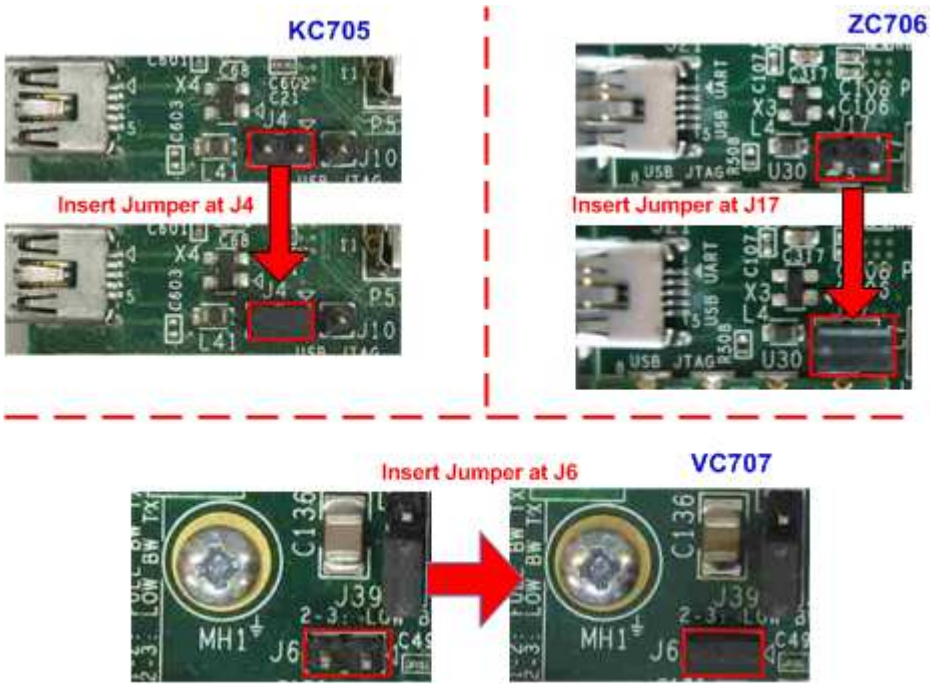

Figure 10 Insert jumper to enable SFP+

- For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 11 - Figure 12.

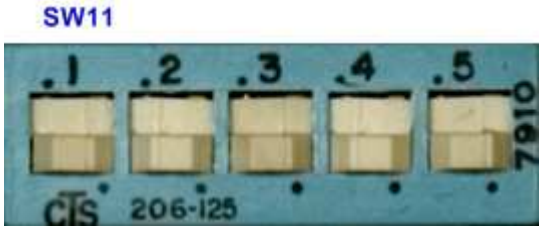

Figure 11 SW11 setting to configure PS from JTAG on ZC706 board

Figure 12 SW4 setting to use USB-to-JTAG on ZC706 board

- Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.
- Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- Open iMPACT and download bit file to FPGA development board, as shown in Figure 13.

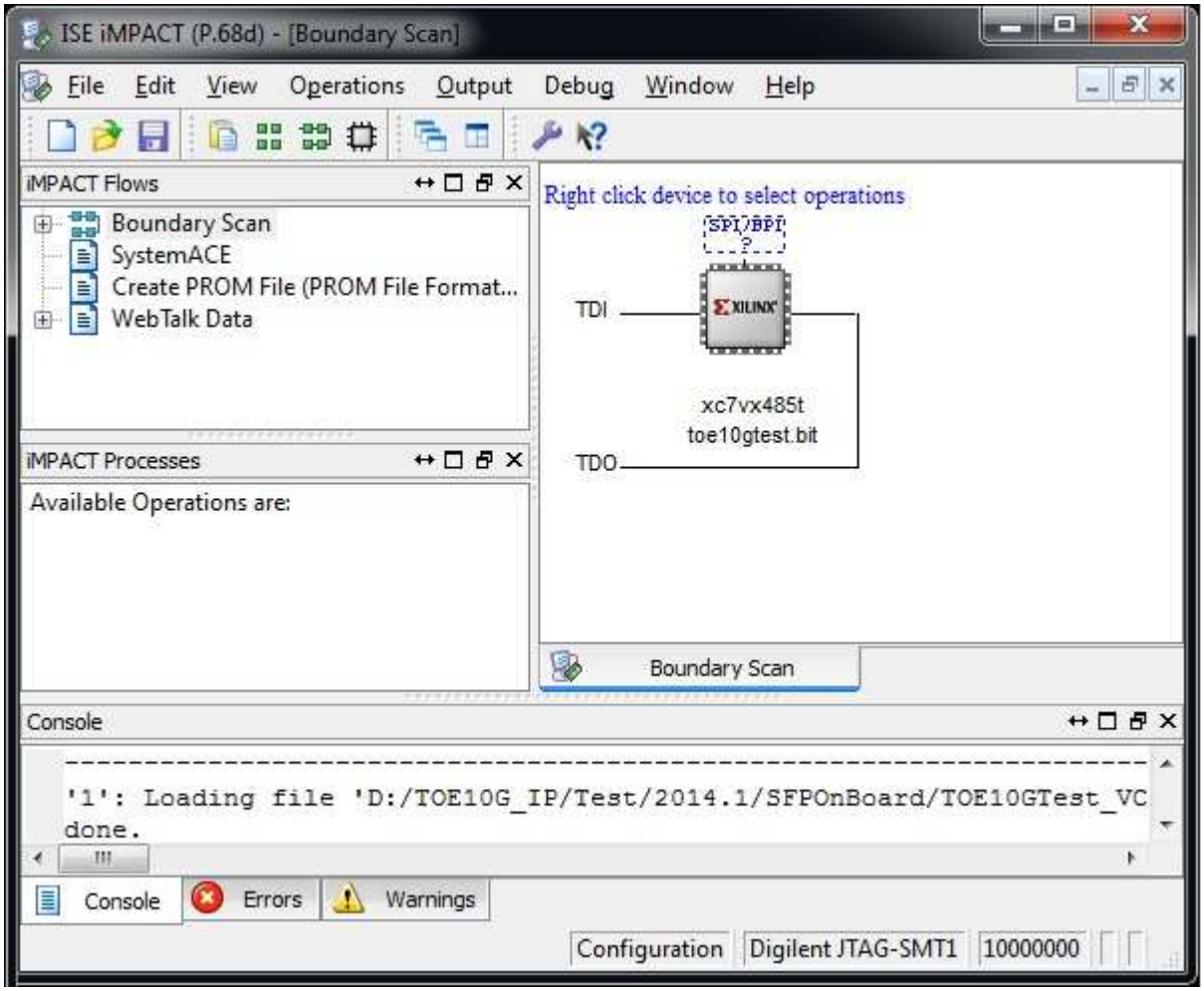

Figure 13 Programmer Environment

- Press StartSW at Center-SW as shown in Figure 1 - Figure 3 to initialize parameter in system, and then LED0 will turn on, as shown in Figure 14 and Figure 15 following DIPSW[1] setting.

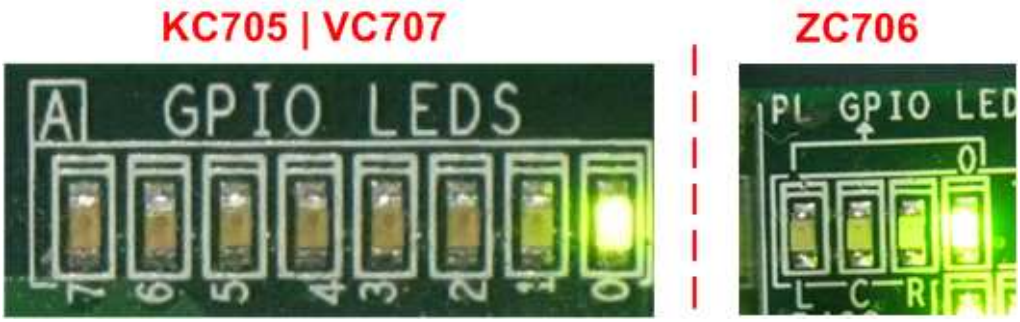

Figure 14 LED Status after push StartSW when DIPSW[1]=OFF

Figure 15 LED Status after push StartSW when DIPSW[1]=ON

Now system is ready to transfer data. The step to test Sending and Receiving data is described in the next topic.

Note: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.

4.1 Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test.

4.1.1 Non-Jumbo frame mode

- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = OFF and confirm that LED2/C status is OFF.
- Open “command prompt” on PC, and run “recv_tcp_client_10G” test application by following command
  >> recv_tcp_client_10G <FPGA IP address> <FPGA port number> <number of data in packet>
  For example,
  >> recv_tcp_client_10G 192.168.7.42 4000 1456
  Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without HDL code modification.
- Test application displays current numbers of packet, and time usage with performance is displayed at the end of each loop transfer, as shown in Figure 16.
- User can cancel operation by pressing “Ctrl+C”.

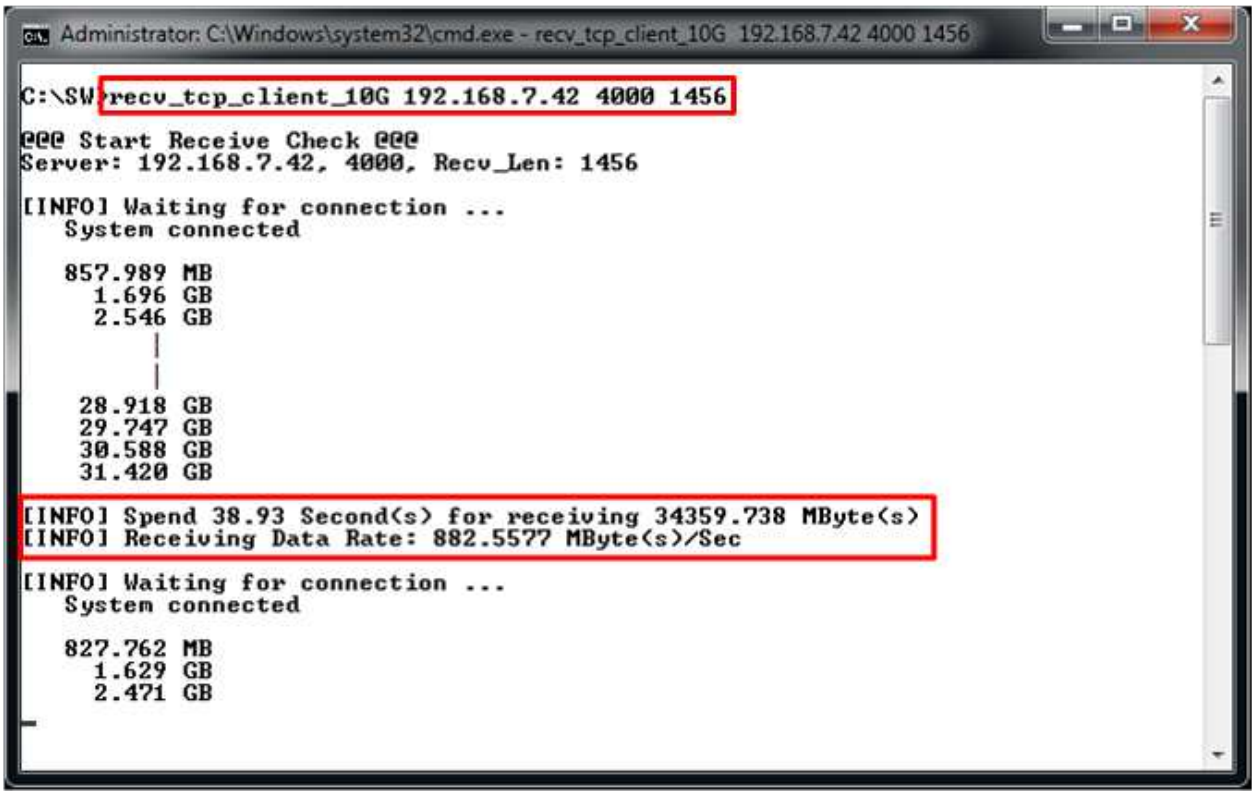

Figure 16 Non-Jumbo frame Sending Demo

Figure 17 LED Status when running Sending Demo with Non-Jumbo frame

4.1.2 Jumbo frame mode

- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = ON and confirm that LED2/C status is ON.
- Open “command prompt” on PC, and run “recv_tcp_client_10G” test application by following command
  >> recv_tcp_client_10G 192.168.7.42 4000 8960
  Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without HDL code modification.
- Message during test application and how to cancel operation are similar to Non-Jumbo frame mode.

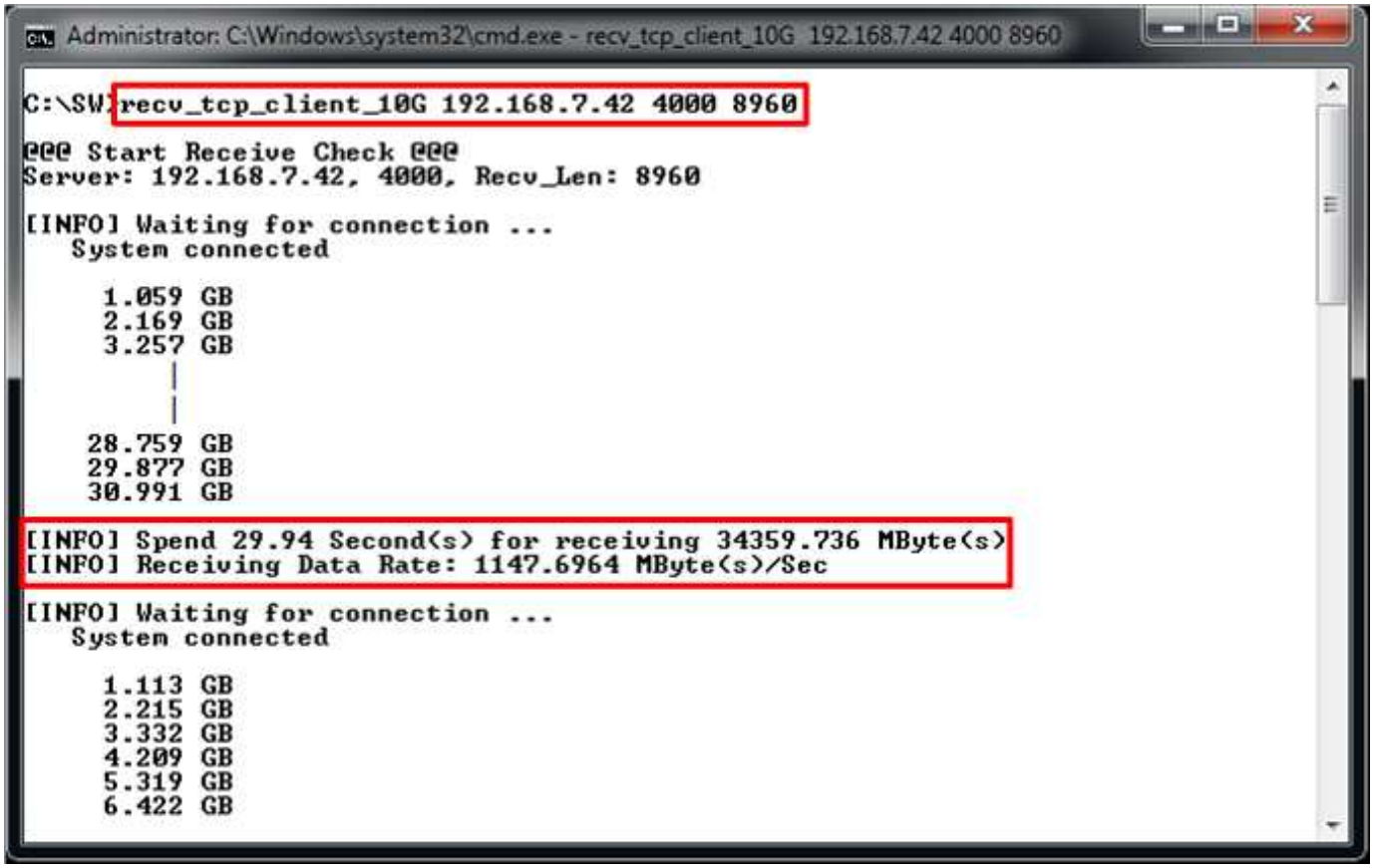

Figure 18 Jumbo frame Sending Demo

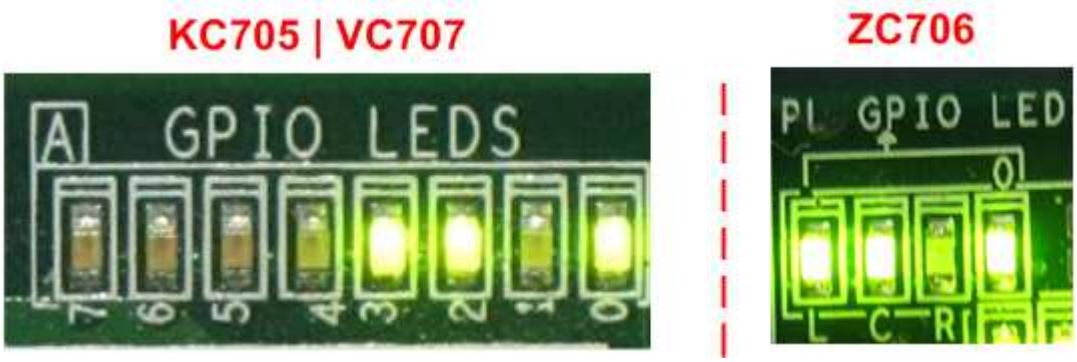

Figure 19 LED Status when running Sending Demo with Jumbo frame

4.2 Run Receiving Demo

4.2.1 Performance test mode

- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = OFF to disable verification module.
- Open “command prompt” on PC, and run “send_tcp_client_10G” test application by following command
  >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without HDL code modification.
  - User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
  - Mode: ‘0’- All ‘0’ patterns are sent for performance test.

  For example,
  >> send_tcp_client_10G 192.168.7.42 4000 559241 0

- Test application displays “…” during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 21.

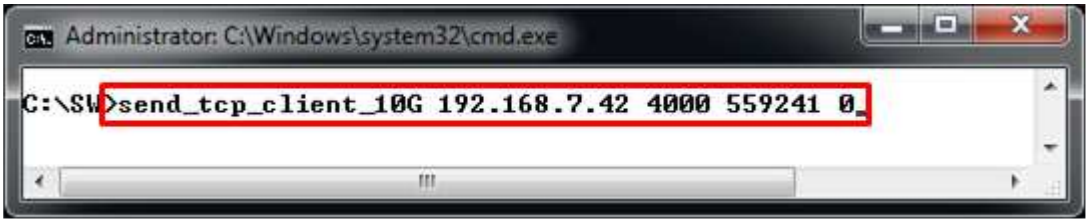

Figure 20 Command line for receiving demo on Performance test mode

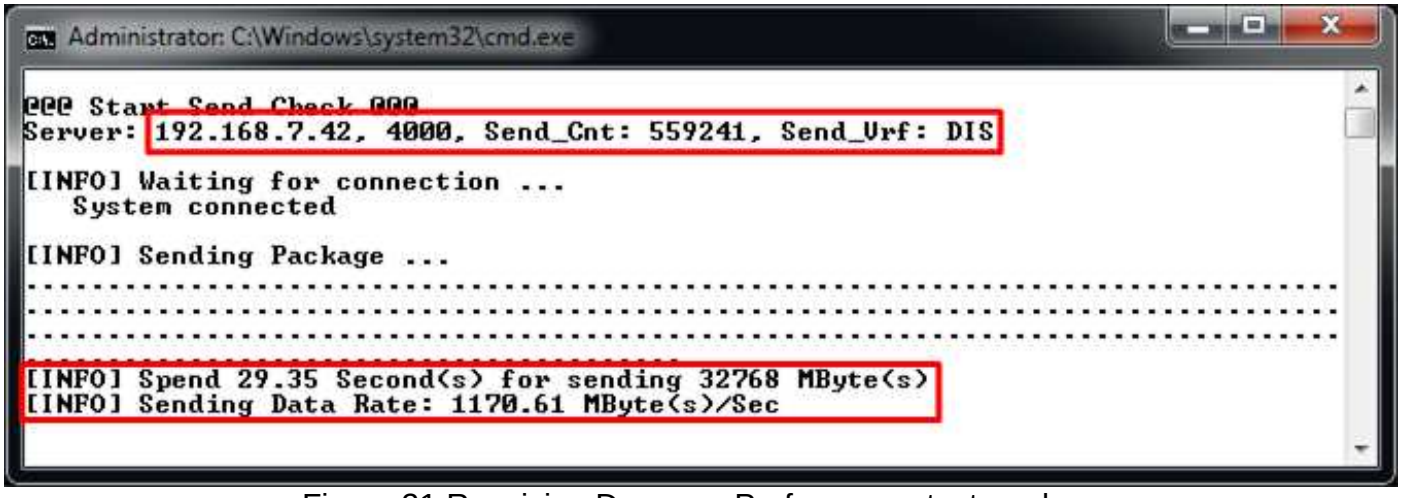

Figure 21 Receiving Demo on Performance test mode

4.2.2 Verification mode

- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = ON to enable verification module.
- Open “command prompt” on PC, and run “send_tcp_client_10G” test application by following command
  >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 60kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without HDL code modification.
  - User can set transfer size in 60kByte unit which is buffer size in test application. In this example, 559241 means 32 GB data is transferred. Valid range of transfer size is 1 – 559241.
  - Mode: ‘1’- 32-bit increment data are sent for data verification.

  For example,
  >> send_tcp_client_10G 192.168.7.42 4000 559241 1
- Test application displays “…” during transferring packet, and time usage with performance is displayed when complete data transfer, as shown in Figure 23.

Figure 22 Command line for receiving demo on Verification mode

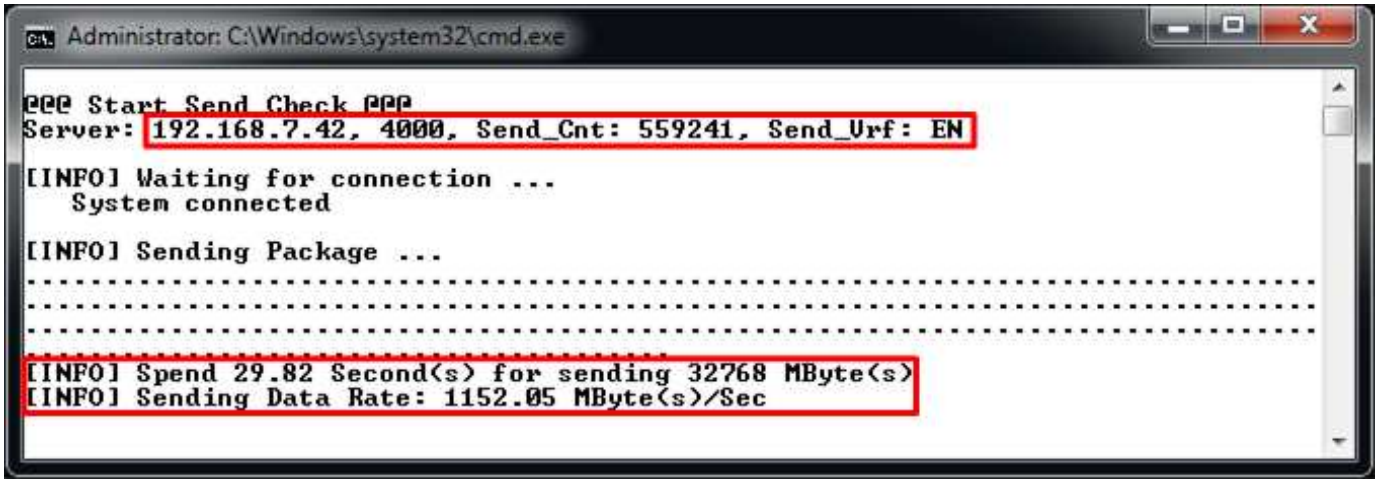

Figure 23 Receiving Demo on Verification mode

- LED3/L will blink if any error data detects from Verification module.

5 Revision History

Revision	Date	Description
1.0	05-Sep-14	Initial version release
1.1	10-Nov-14	Add ZC706 support
1.2	24-Aug-15	Add 3.3 Power Option Setting