

TOE10G-IP Multisession Demo Instruction

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This document describes the instruction to show 10Gb Ethernet data transfer between FPGA board and PC. PC can run up to eight test applications for transferring data through eight sessions at the same time. Packet size in the demo is not Jumbo frame size.

1 Environment Setup

As shown in Figure 1-1 to run the demo, please prepare

- 1) FPGA Development board (Arria10 SoC development board)
- 2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
- Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
- 4) micro USB cable for programming FPGA between FPGA Development board and PC
- 5) Test application available on PC: "tcpdatatest.exe" provided by Design Gateway



Figure 1-1 TOE10G-IP Multisession Demo Environment Setup on Arria10 SoC board

Note: Test result in this document is captured by using following test environment. [1] 10G Network Adapter: Intel X520-DA2

- http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ ethernet-x520-server-adapters-brief.html
- [2] 10-Gigabit SFP+ DAC cable http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx
 [3] PC: Motherboard Z170-K, 32 GB RAM, 64-bit Windows7 OS, CPU i7-6700K@4.00 GHz



2 Demo description

Up to eight sessions can be operated at the same time for sending or receiving data with PC. Each session can be set transfer direction from 4-bit GPIO DIPSW on FPGA board. One bit is used to set for two sessions as follows.



Figure 2-1 4-bit DIPSW in the demo

DIPSW	OFF (Logic='1')	ON (Logic='0')			
5	Port#4000 and #4001 receive data from PC	Port#4000 and #4001 send data to PC			
6	Port#4002 and #4003 receive data from PC	Port#4002 and #4003 send data to PC			
7	Port#4004 and #4005 receive data from PC	Port#4004 and #4005 send data to PC			
8	Port#4006 and #4007 receive data from PC	Port#4006 and #4007 send data to PC			
Table 2-1 4-bit DIPSW Definition					



Figure 2-2 4-bit LED to show demo status

4-bit LED is used to show hardware status. The definition of LED on FPGA development board is described in Table 2-2.

LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete.
		Please check that StartSW (S3) has already been pressed and confirm IP address setting on PC that is correct.
1	BLINK: Timeout is found in	Normal operation
	some session.	
2	N/A	N/A
3	ON: Connection of some	No operation
	sessions are established	

Table 2-2 LED Definition



3 Demo setup

To set up the demo, please follow these steps.

1) Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.



Figure 3-2 Power cable connection

 Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between SFP+ Port A and PC.



Figure 3-3 SFP+ cable connection

3) Setup network setting on PC, following Topic 3 in "dg_toe10gip_instruction_altera" document.

http://www.dgway.com/products/IP/TOE10G-IP/dg_toe10gip_instruction_altera_en.pdf

4) Power on FPGA development board.



5) Open "Clock Controller" application which is provided in Arria10 SoC release package. Select Si5338(U50) tab, and set CLK3 value to be "322.265625". Click "Set" button to program clock to be 322.265625 MHz, as shown in Figure 3-4.

Register	Anna contraction of the second of	Frequen	cy (MHz)	🗾 Disable All
CLK0	125.000000	CLK0	125.000000	Disable CLK0
CLK1	270.000314	CLK1	270.000314	Disable CLK1
CLK2	99.999806	CLK2	99.999806	Disable CLK2
CLK3	322.265625	CLK3	322.265625	Disable CLK3
F_vco: 2578	.125000 MHz			
	Default	Read	Set	Import
ssanes				

6) Open Quartus Programmer, select SOF file, and program file to FPGA development board, as shown in Figure 3-5.

dware Setup	SB-Blasterll [USB-1] ow background program	nming when available		lode: JTAG			Progress:	100)% (Success	ful)
Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase
Stop Constant St	OE10G-IP/Test/TOE1 ne> ne> ne>	10as066n3140e2sge2 SOCVHPS 5M2210Z 5M2210Z	1D29F052 00000000 00000000 00000000	FFFFFFF <none> <none> <none></none></none></none>						
dd File			×	ADTERIA		TRA -				
Down	10AS066N3F TDO	40E2 SOCVH	PS	5M2210Z	5M2	210Z				



7) Press StartSW at S3 position as shown in Figure 3-6 to initialize parameter in system, and then LED0 will turn on, as shown in Figure 3-7.



Figure 3-6 StartSW position



<u>Note</u>: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.



4 Run the demo

Please confirm that LED0 status now is ON to confirm that IP completes initialization process. In this reference design, "tcpdatatest" application is called in client mode to establish the new connection and send/receive data with the server which is implemented by TOE10G-IP. More details to run send or receive data test in each session are described as follows.

4.1 Send data test

This topic describes the step to run data sending test from FPGA to PC. Transfer size is fixed to be 32 GB. User can run up to eight sessions at the same time by running eight "tcpdatatest" with setting port number to be 4000 - 4007. DIPSW of selected port must be set to 'ON' for send data test.

Type following command to run "tcpdatatest" in this test. >> tcpdatatest c r 192.168.7.42 <4000-4007> 0 1

LED3 will turn on to show that port 4000-4007 is established. On PC console, total transfer size will be displayed every second. Test performance will be displayed after end of operation.

Figure 4-1 shows the example when running send data test by using Port#4000. DIPSW bit 5 must be set to 'ON'. Performance is about 1/4 times of standard demo because the IP in this demo uses only 4Kbyte buffer size while standard demo uses 64 Kbyte buffer size.

C:\Windows\system32\cmd.exe		
:\Share\Pat\SW>tcpdatatest c r 192.168.	Port 4000-4001: F	PGA -> P
tart Receiving with Data pattern in Clic P: 192.168.7.42:4000 aiting for connection System connected	ent mode 1 2 5 2 2 5 2 2 5 2 2 5 2 2 5 2 2 5 2 2 5 2 2 5 2	0A08
eceiving Data Size 180.556 MB 367.192 MB 552.361 MB 735.433 MB		6 7 8
33.742 GB 33.980 GB 34.227 GB	HPS0 HPS1 HPS2 HPS3 PGA0	PGA1 PGA2 PGA3
pend 152.10 Second(s) for Receiving 34 eceiving Data Rate: 225.90 MByte(s)/Sec	.360 GByte(s)	
:\Share\Pat\SW>_		*



Figure 4-2 shows the example when running send data test by using 8 sessions (Port 4000 - 4007) at the same time. Bit5-8 of DIPSW must be all set to 'ON'. Performance in Figure 4-3 for one session is about 127-143 MB/sec, and total performance is about 1046 MB/sec.





Figure 4-4 shows the example when running send data test by using 4 sessions (Port 4000 - 4003) at the same time. Performance of one session is about 194-198 MB/sec which is about 10% less than running only one session in Figure 4-1.

C:\Windows\system32\cmd.exe	
27.114 GB 27.314 GB 27.314 GB 27.304 GB 28.110 GB 28.110 GB 28.517 GB 28.517 GB 29.528 GB 29.528 GB 29.528 GB 29.528 GB 30.542 GB 30.548 GB 30.548 GB 31.565 GB 31.555 GB 32.552 GB 32.552 GB 32.553 GB 33.544 GB 34.360 GByte(s)/Sec	
Spend 174.72 Second(s) for Receiving 34.360 Receiving Data Rate: 196.66 MByte(s)/Sec	jØ GByte(s)
Spend 176.83 Second(s) for Rec Receiving Data Rate: 194.31 MB	eceiving 34.360 GByte(s) MByte(s)/Sec +

Figure 4-4 Performance when run send data test using 4 sessions at the same time



4.2 Receive data test

This topic describes the step to run the test to receive data from PC. User can set total transfer size from application. Up to eight sessions can run at the same time by running eight "tcpdatatest" with setting port number to be 4000 - 4007. DIPSW of selected port must be set to 'OFF' for receive data test.

Type following command to run "tcpdatatest" in this test. >> tcpdatatest c t 192.168.7.42 <4000-4007> <byte length> 1

LED3 will turn on to show that port 4000-4007 is established. On PC console, total transfer size will be displayed every second. Test performance will be displayed after end of operation.

Figure 4-5 shows the example when running receive data test by using Port#4000. DIPSW bit 5 must be set to 'OFF'. Performance is about 1/4 times of standard demo because the IP in this demo uses only 4Kbyte buffer size while standard demo uses 64 Kbyte buffer size.

Port number: Valid valu	e = 4000 - 4007	Transfer len	gth = 34.36 GByte
C:\Windows\system32\cmd.exe			
D:\Share\Pat\SW tcpdatatest c t 192. Start Sending with Data pattern in C IP: 192.168.7.42:4000 Waiting for connection System connected Sending Data Size 236.978 MB 473.956 MB 710.935 MB 33.624 GB 33.875 GB	168.7.42 (4000) (4		Port 4000-4001: PC -> FPGA
Spend 138.84 Second(s) for Sending Sending Data Rate: 247.48 MByte(s)/S D:\Share\Pat\SW>_	34.360 GByte(s) ec	SdH	LT LL LL

Figure 4-5 Receive data test by using Port#4000 and DIPSW setting



Figure 4-6 shows the example when running send data test by using 8 sessions (Port 4000 - 4007) at the same time. Bit5-8 of DIPSW must be all set to 'OFF'. Performance in Figure 4-7 for one session is about 148-158 MB/sec, and total performance is about 1221 MB/sec.



Figure 4-8 shows the example when running send data test by using 4 sessions (Port 4000 - 4003) at the same time. Performance of one session is about 215-222 MB/sec which is about 10% less than running only one session in Figure 4-5.

C:\Windows\system32\cmd.exe			
26.221 GB 26.445 GB 26.699 GB 27.188 GB 27.303 GB 27.303 GB 27.754 GB 28.200 GB 28.423 GB 28.423 GB 28.647 GB 29.694 GB 29.994 GB 29.545 GB 29.769 GB 29.769 GB 30.218 GB 30.667 GB 30.891 GB 31.115 GB 31.340 GB 31.560 GB 32.233 GB 32.458 GB 32.609 GB 32.233 GB 32.458 GB 33.575 GB 33.575 GB 33.575 GB 33.575 GB			
Spend 154.77 Second(s) for Sending 34.360 GByte(s) Sending Data Rate: 222.01 MByte(s)/Sec Spend 159.12 Second(s) for Sending 34.360 GByte(s) Sending Data Rate: 215.94 MByte(s)/Sec Spend 159.00 Second(s) for Sending 34.366 Sending Data Rate: 216.11 MByte(s)/Sec Spend 156.69 Second(s) for Sending Data Rate: 219.29 M	∂ GByte(s) Sending 34.36 Byte(s)∕Sec	eØ GByte(s)	 THE STREET

Figure 4-8 Performance when run receive data test using 4 sessions at the same time

4.3 Send and Receive data test

User can set 4-bit DIPSW to be different value to run send and receive data test by using different port number.

Figure 4-9 and Figure 4-10 shows the test result when running send and receive data test by using two and eight sessions sequentially.

Figure 4-9 Send/Receive data test using two sessions

5 Revision History

Revision	Date	Description
1.0	18-Nov-16	Initial version release