

# FPGA set up for TOE/UDP10G-IP with CPU Demo

Rev3.3 13-Mar-23

## 1 Overview

This guide provides instructions on how to setup an FPGA board and create a test environment for running the TOE10G-IP or UDP10G-IP demo. The user has the option to create two test environments for transferring TCP or UDP data via a 10G Ethernet connection using either TOE10G-IP or UDP10G-IP. Figure 1-1 illustrates these two options.

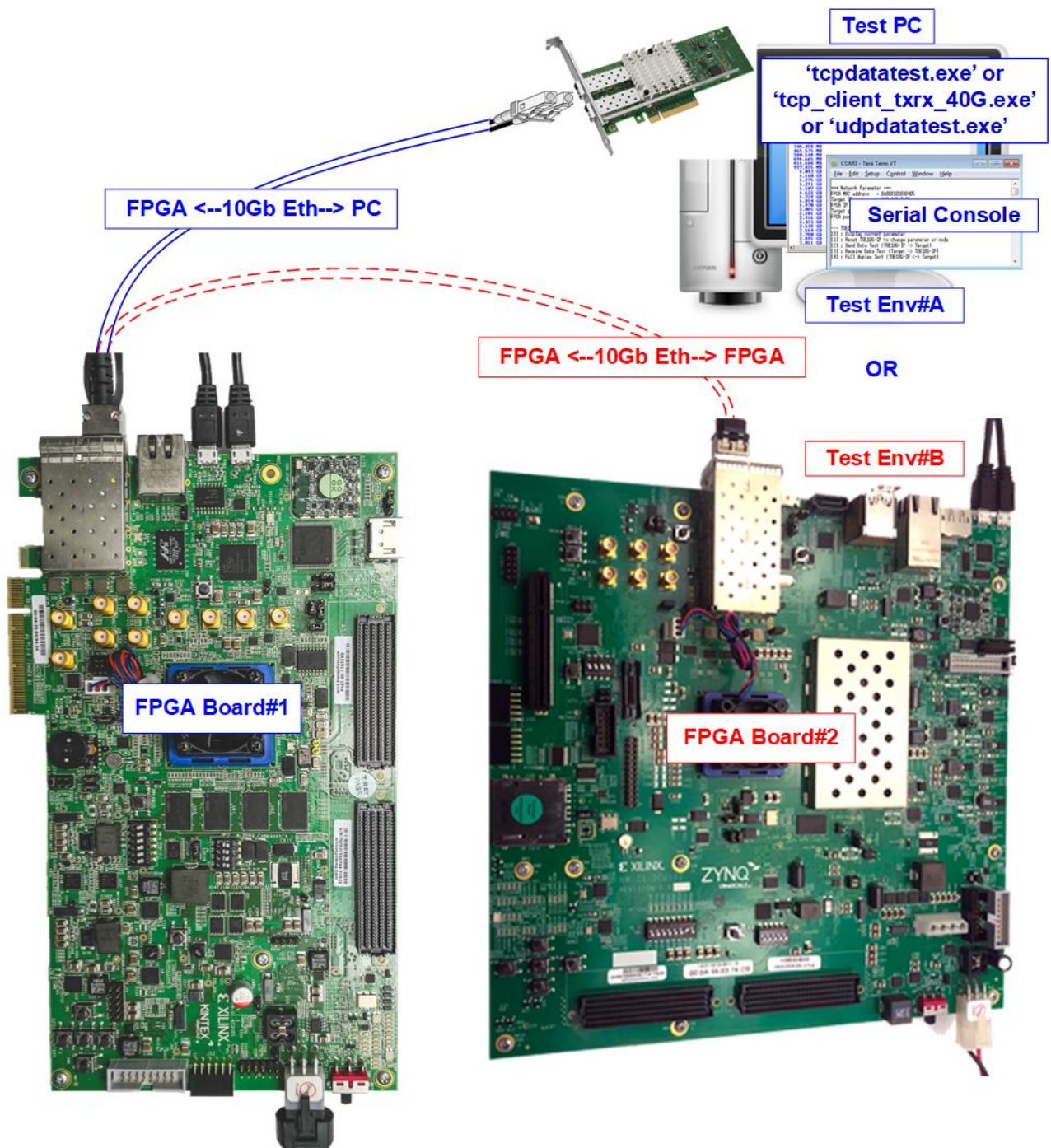


Figure 1-1 Two test environments for running the demo



dg\_toeudp10gip\_fpgasetup\_xilinx.doc

The first test environment requires one FPGA board and a PC with a 10G Ethernet card for data transfer. The PC runs a test application, such as tcpdatatest (half-duplex test for TOE10G-IP), tcp\_client\_txrx\_40G (full-duplex test for TOE10G-IP), or udpdatatest (test application for UDP10G-IP). The Serial console is also run on the PC to act as the user interface console.

The second test environment involves two FPGA boards which may be different from each other. Both boards run the TOE10G-IP or UDP10G-IP demo, with different initialization mode assigned (Client or Server).

## 2 Test environment setup using an FPGA and PC

Before running the demo using an FPGA and PC, please prepare the following.

- FPGA development boards: ZC706/ZCU102/ZCU106/KCU105/VCU118/KCU116/ZCU111 board
- PC with a 10 Gigabit Ethernet or 10 Gigabit Ethernet card installed
- 10 Gb Ethernet cable:
  - a) 10 Gb SFP+ Passive Direct Attach Cable (DAC) with a length of 1-m or less
  - b) 10 Gb SFP+ Active Optical Cable (AOC)
  - c) 2x10 Gb SFP+ transceiver (10G BASE-R) with an optical cable (LC to LC, Multimode)
  - d) For VCU118 board only, QSFP+ to four SFP+ cable
- USB cable for connecting the FPGA board to the PC
  - a) ZCU102, ZCU106, KCU105, VCU118 and KCU116: 2 micro USB cables for programming FPGA and Serial console
  - b) ZC706: 1 mini USB cable for programming FPGA and 1 micro USB cables for Serial console.
  - c) ZCU111: 1 micro USB cable for programming FPGA and Serial console.
- Test application provided by Design Gateway for running on PC:
  - a) TOE10G-IP: “tcpdatatest.exe” and “tcp\_client\_txrx\_40G.exe”
  - b) UDP10G-IP: “udpdatatest.exe”
- Serial console software such as TeraTerm installed on the PC. The console settings are Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming FPGA, installed on the PC

*Note: The hardware listed below is an example for running the demo.*

[1] 10G Network Adapter: Intel X710-DA2

<https://ark.intel.com/content/www/us/en/ark/products/83964/intel-ethernet-converged-network-adapter-x710da2.html>

[2] a) 10-Gigabit SFP+ AOC cable (AOC-S1S1-001)

<https://www.10gtek.com/10gsfp+aoc>

b) 40-Gigabit QSFP to 4x10-Gigabit SFP+ cable

<https://www.digikey.sg/htmldatasheets/production/1756903/0/0/1/fcbn510qe2cxx-preliminary.html>

[3] Test PC:

Motherboard: ASUS PRIME Z690M-Plus D4

CPU: Intel i5-12600K CPU 3.7 GHz

RAM: 64 GB DDR4

OS: 64-bit Windows10 OS

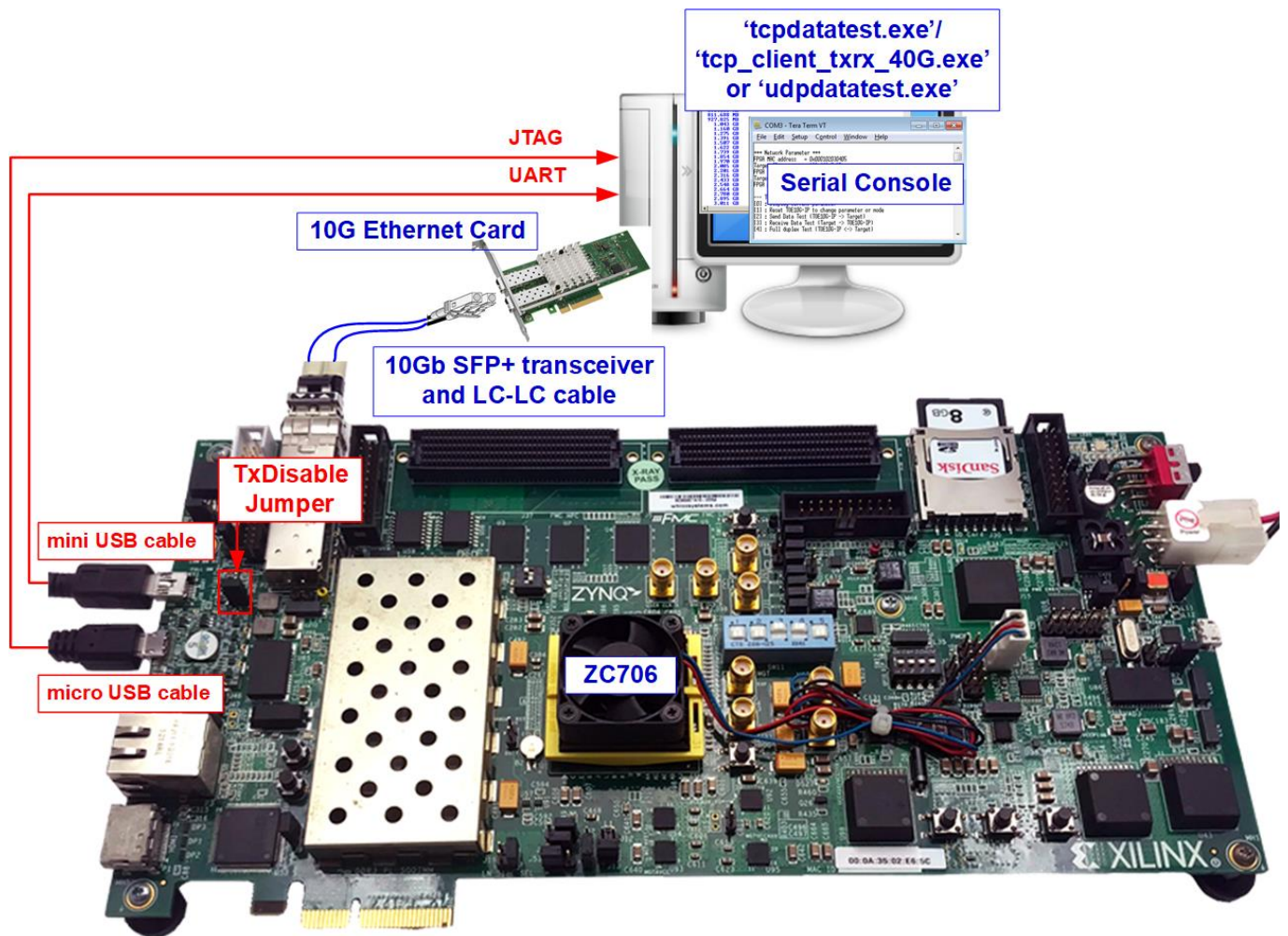


Figure 2-1 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZC706

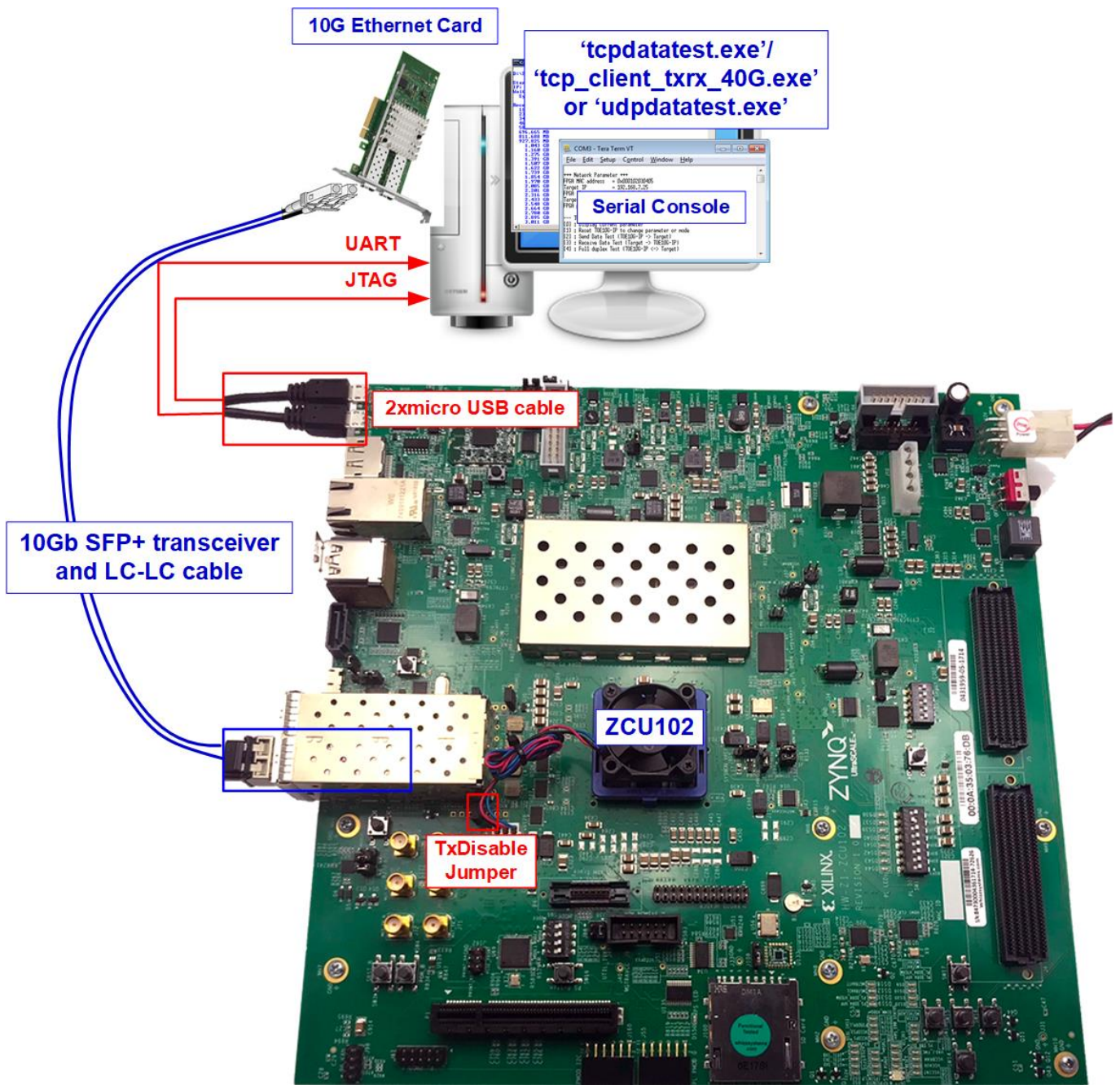


Figure 2-2 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZCU102

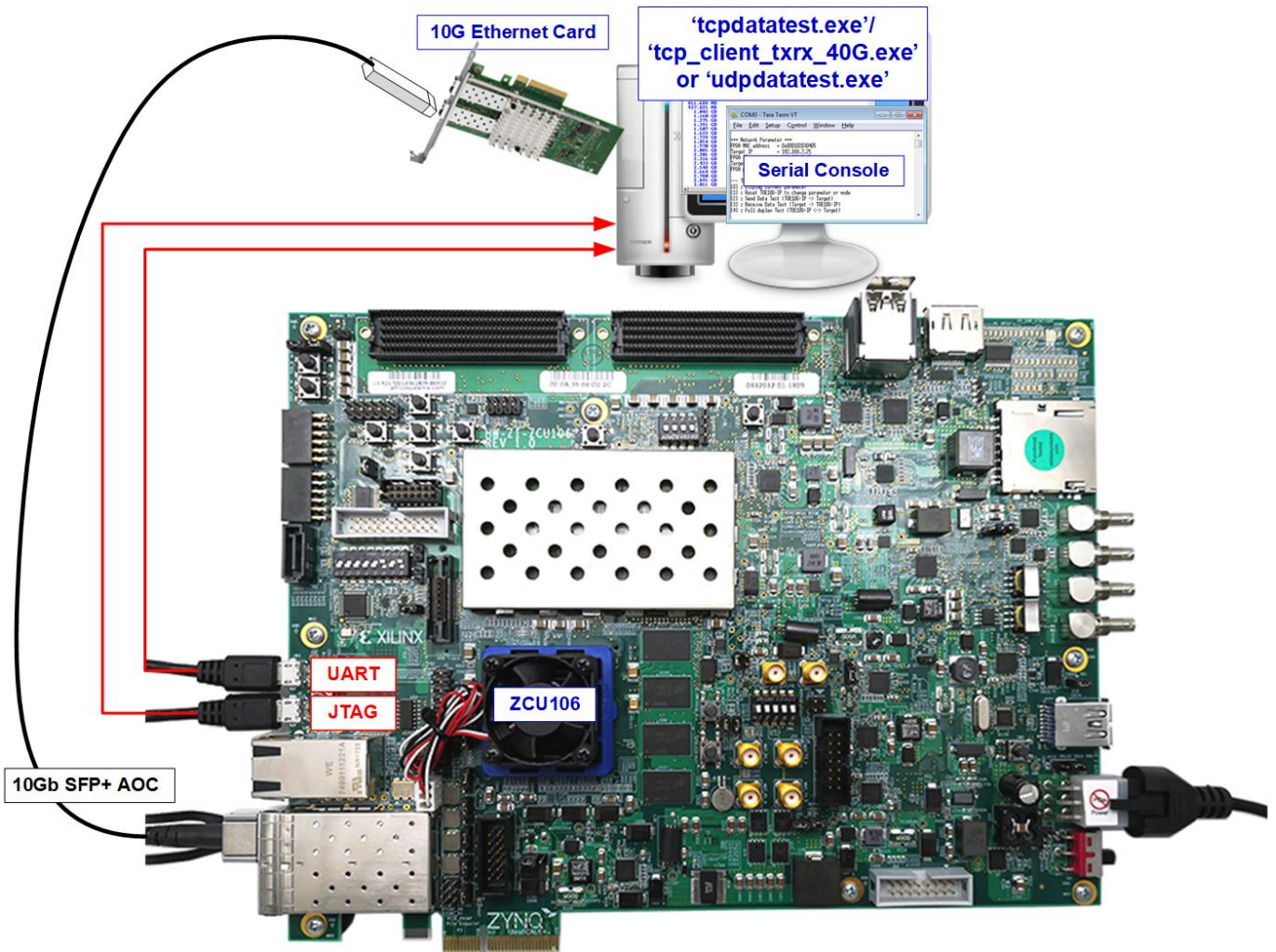


Figure 2-3 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZCU106

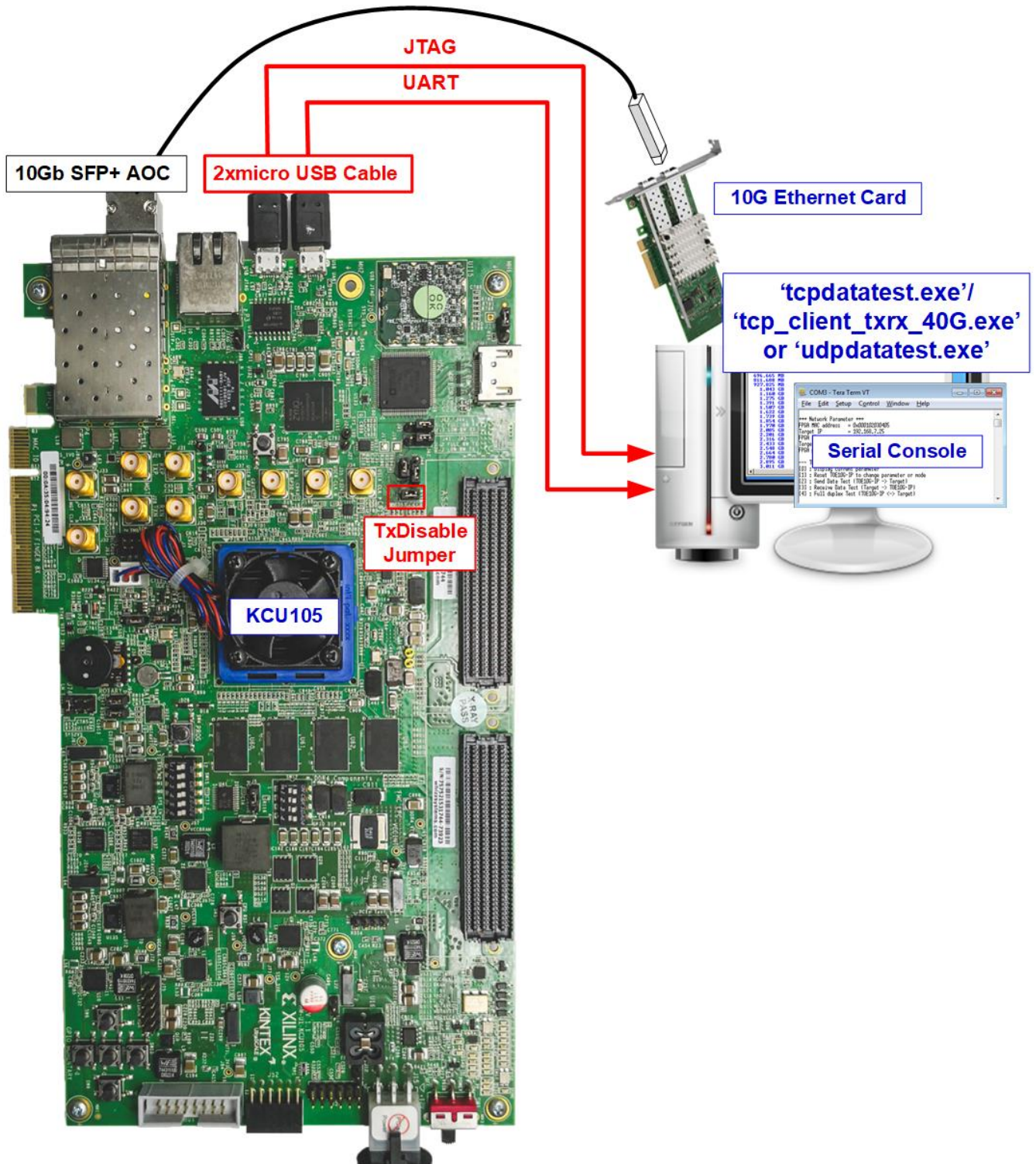


Figure 2-4 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on KCU105

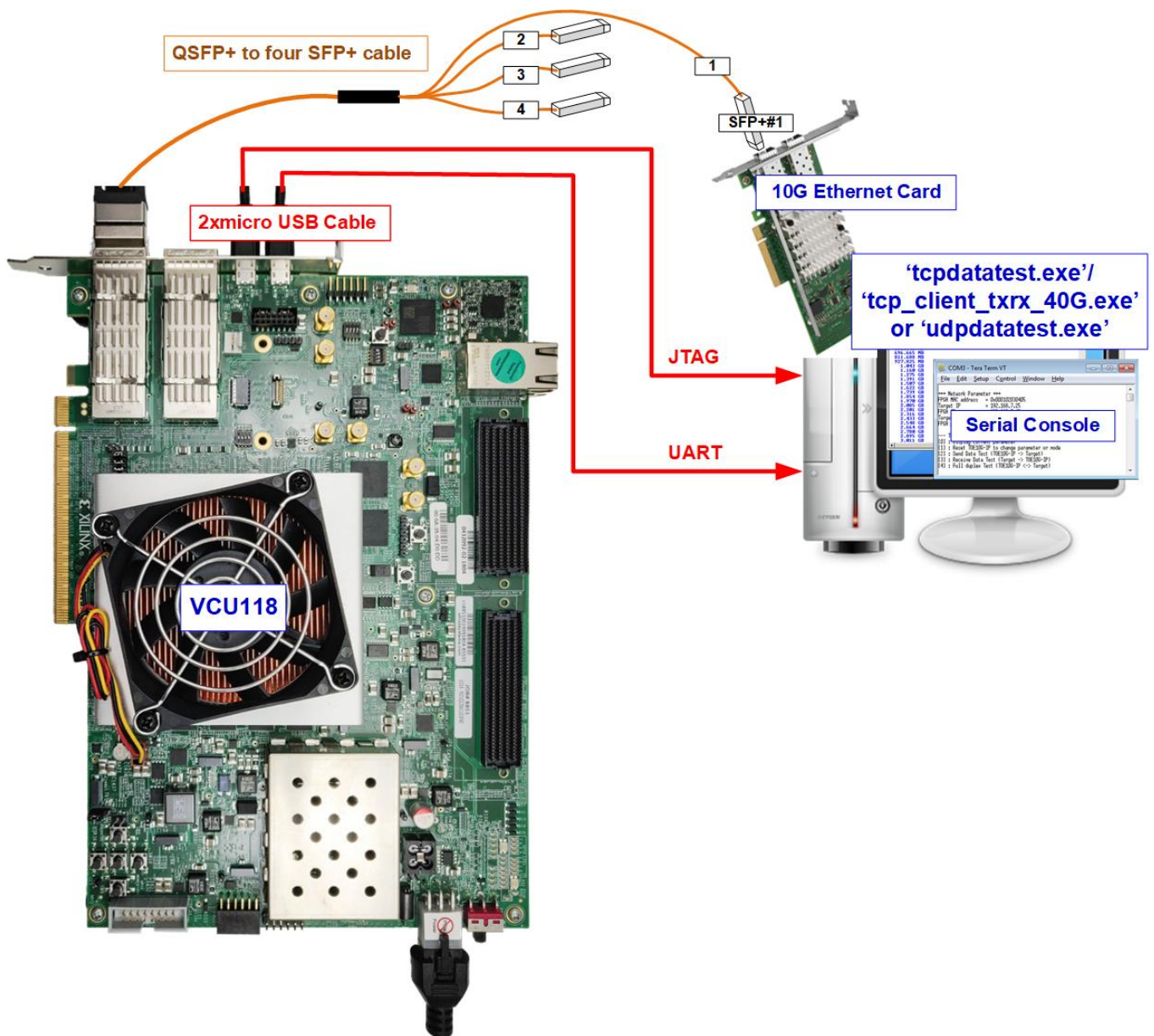


Figure 2-5 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on VCU118



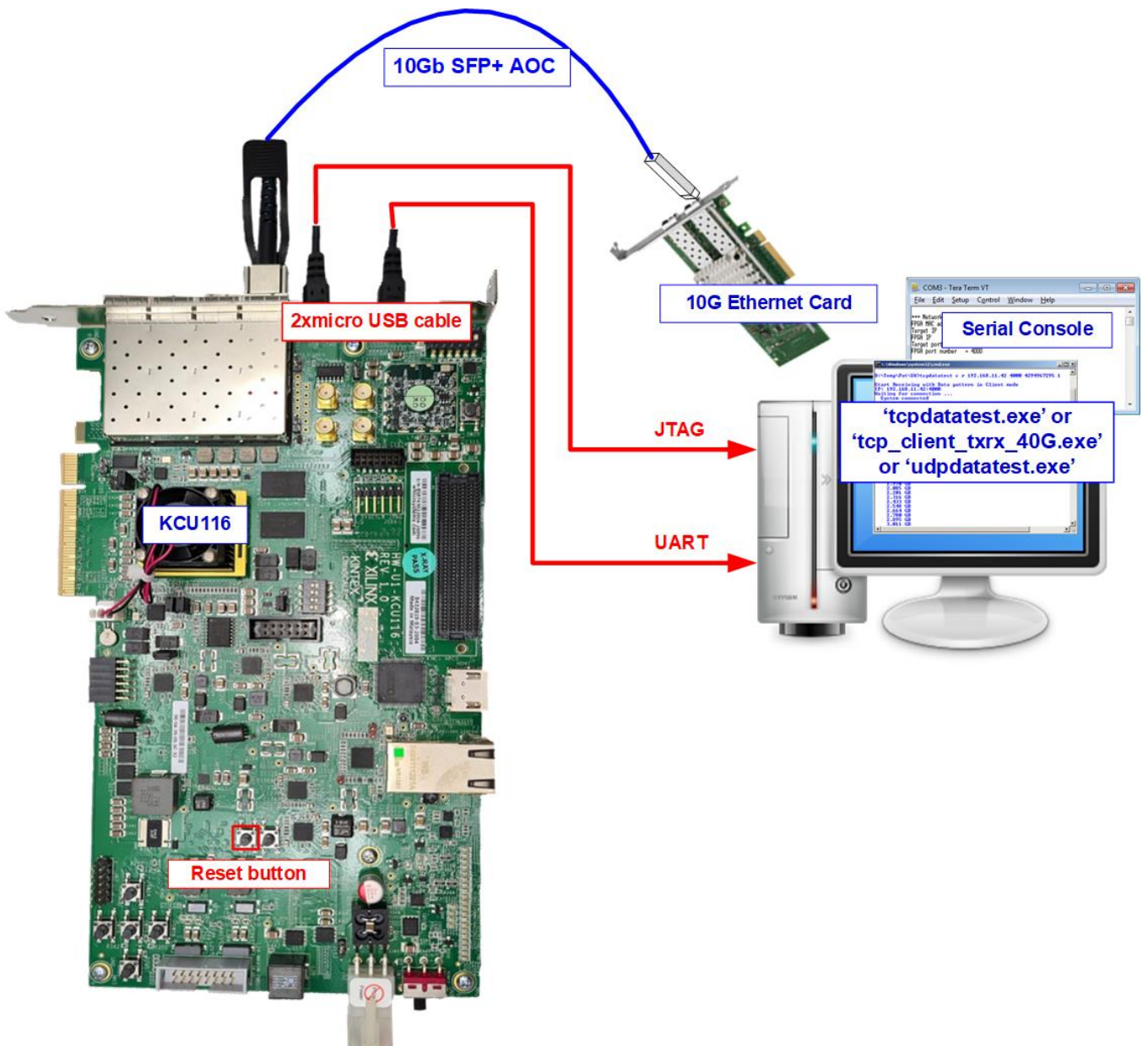


Figure 2-6 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on KCU116

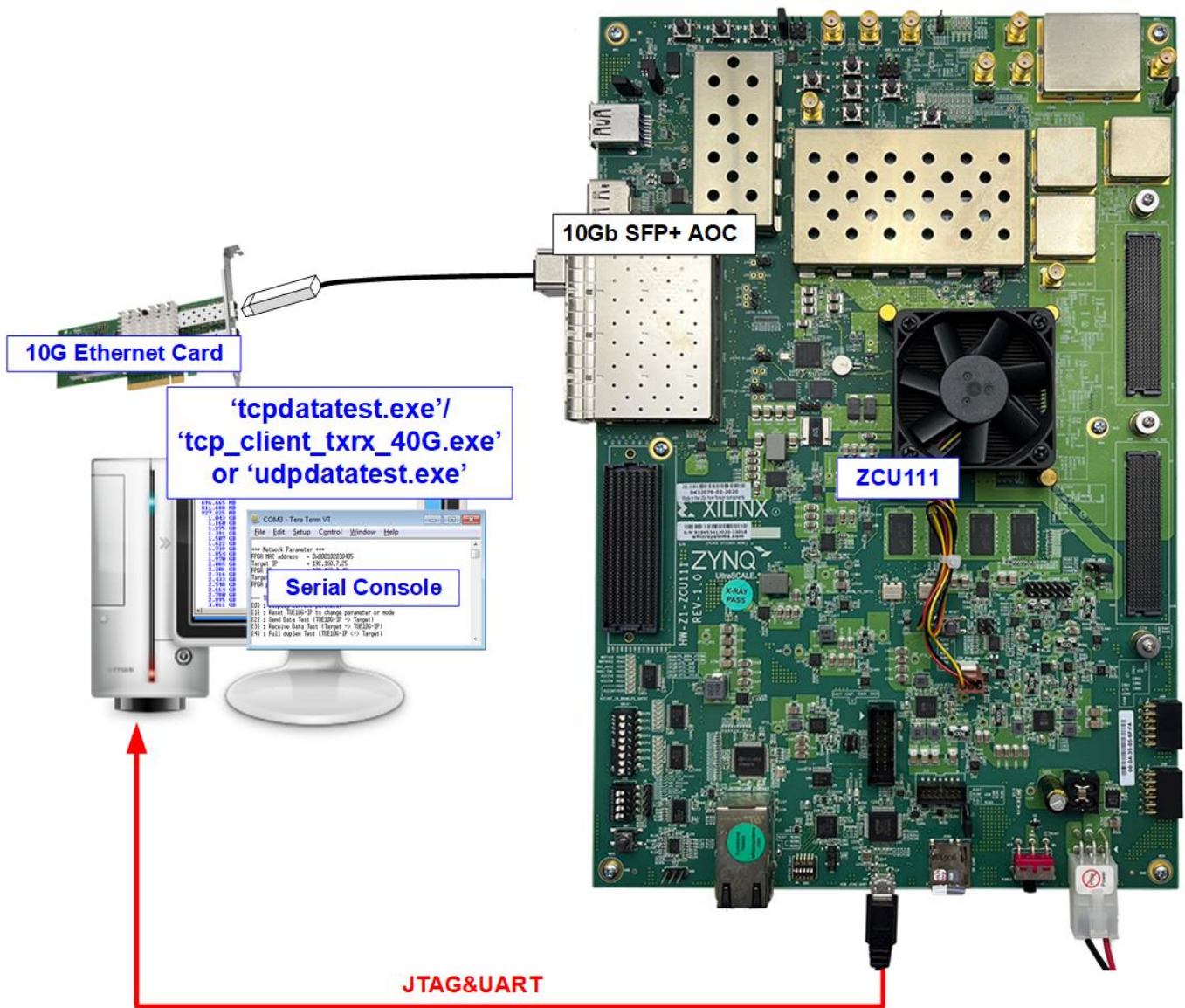


Figure 2-7 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZCU111

The steps for setting up a test environment using an FPGA and a PC are described below.

- 1) Check the DIPSW and jumper settings on the FPGA board.
  - a) The board setting on ZC706 board is shown in Figure 2-8.
    - Insert jumper to J17 to enable Tx SFP+
    - Set SW11 to configure PS from JTAG
    - Set SW4 to use USB-JTAG.

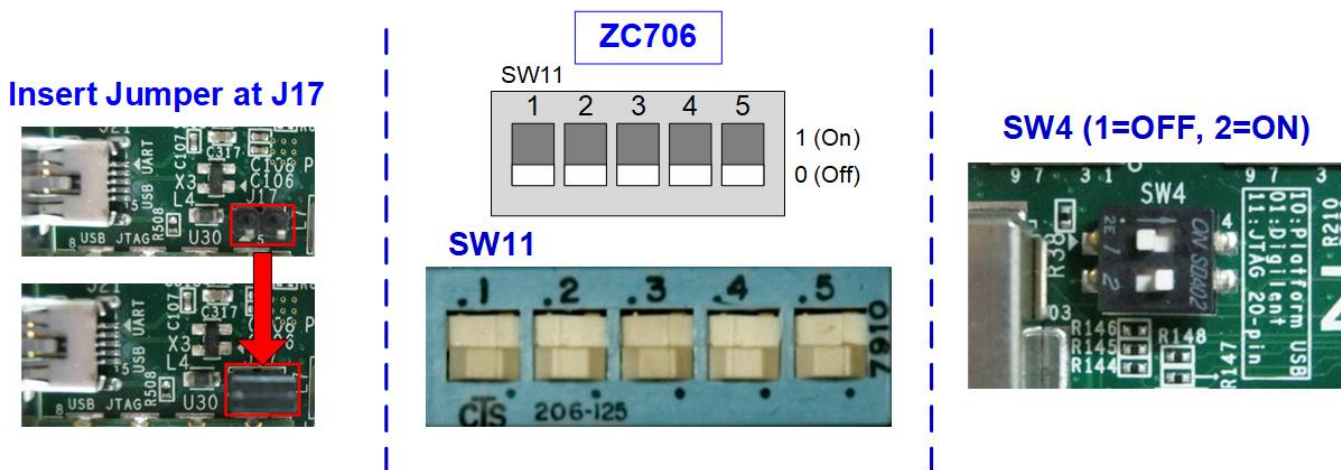


Figure 2-8 ZC706 board setting

- b) The board setting on ZCU102/ZCU106/ZCU111 boards is shown in Figure 2-9.
  - Set SW6=all ONs to use USB-JTAG
  - Only ZCU102, insert jumper to J16 to enable Tx SFP+

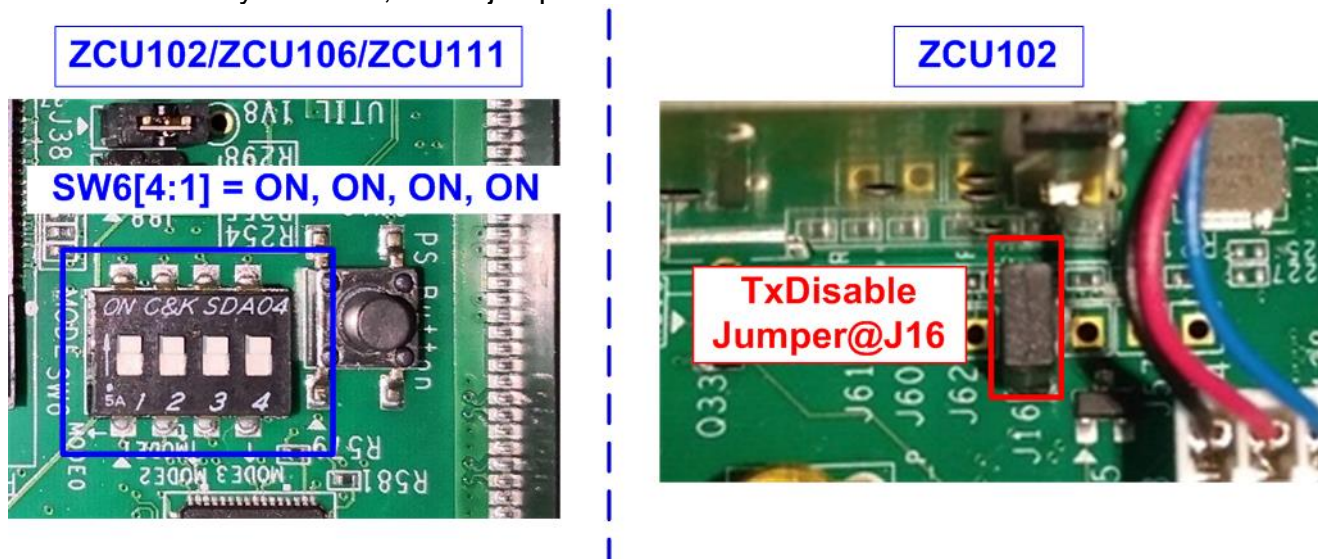


Figure 2-9 ZCU102/ZCU106/ZCU111 board setting

- c) The board setting on KCU105 board is shown in Figure 2-10. Insert jumper to J6 to enable Tx SFP+.

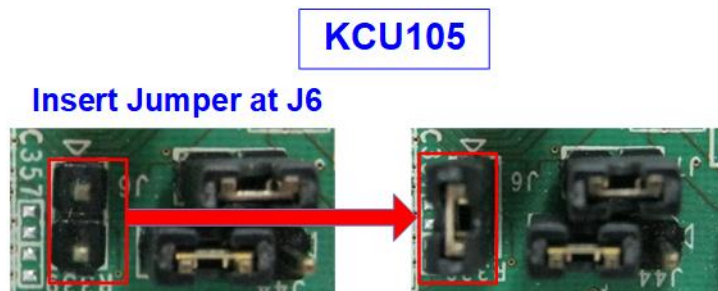


Figure 2-10 Insert jumper to enable SFP+ on KCU105

- 2) Connect a micro USB cable from the FPGA board to the PC for JTAG programming.
- 3) Connect a micro USB cable (for ZCU102/KCU105/VCU118/KCU116 boards) or a mini USB cable (ZC706 board) from the FPGA board to the PC for USB UART.
- 4) Connect the power supply to the FPGA development board.
- 5) Connect the 10G Ethernet cable between the FPGA board and the PC.
  - a) For ZCU102/ZCU106/KCU105/ZC706/KCU116/ZCU111 boards, insert a 10 Gb SFP+ DAC (Length<1m), AOC, or SFP+ transceiver with an LC-LC cable. Some boards have multiple SFP connectors, so use the appropriate channel as shown in Figure 2-11.

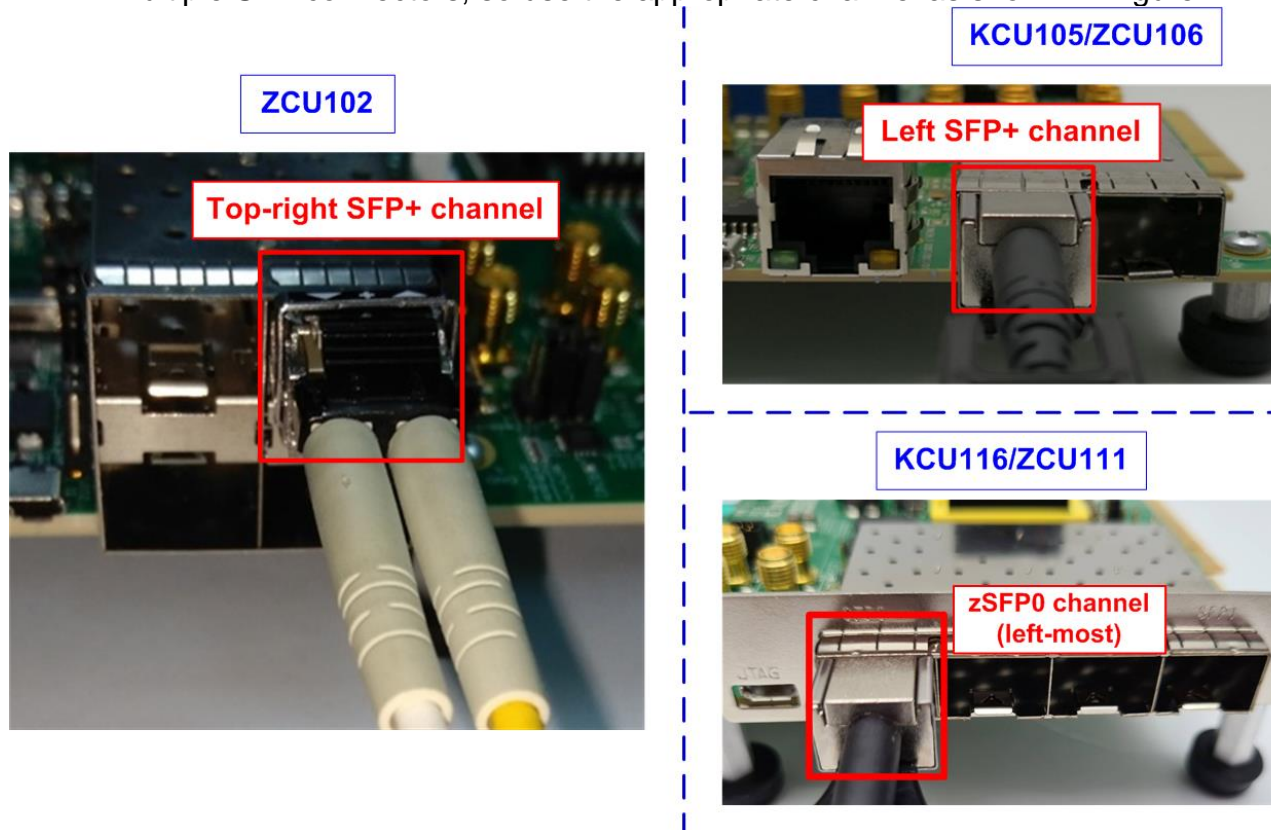


Figure 2-11 SFP+ channel using on ZCU102/ZCU106/KCU105 board

- b) For VCU118, insert QSFP+ to 4 SFP+ cable between the FPGA board and the PC. Use SFP+ no.1 to connect to QSFP1, connector on the right side, as shown in Figure 2-12.

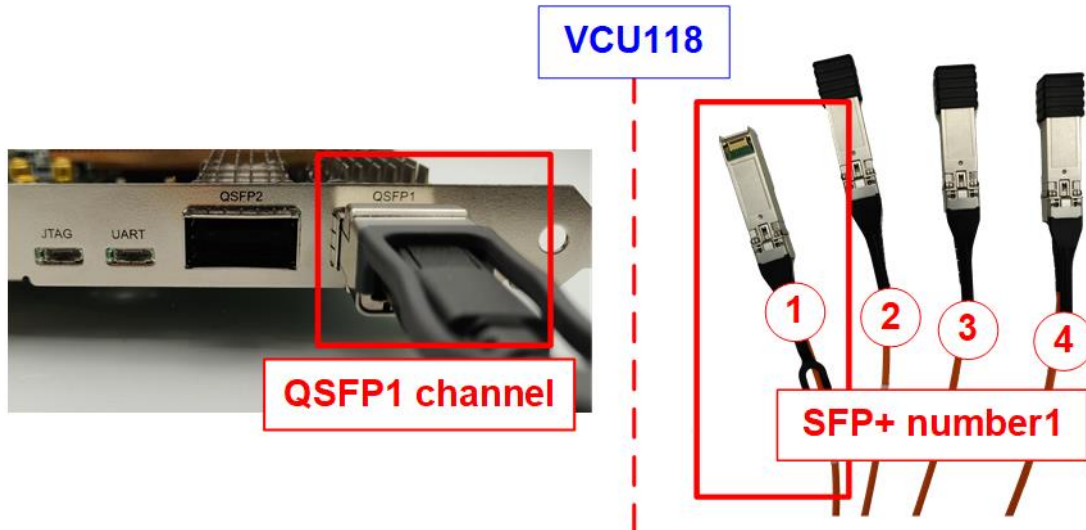


Figure 2-12 QSFP+ channel using on VCU118 board

- 6) Power on the FPGA board.
- 7) Open the Serial console. When the FPGA board is connected to the PC, multiple COM ports from the FPGA connection are detected and displayed in the Device Manager. For KCU105/VCU118/KCU116 boards, select the Standard COM port. For ZCU102/ZCU106, select the COM port number of Interface0. For ZCU111, select the lowest value of USB Serial port. Use following setting on the Serial console: Baud rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

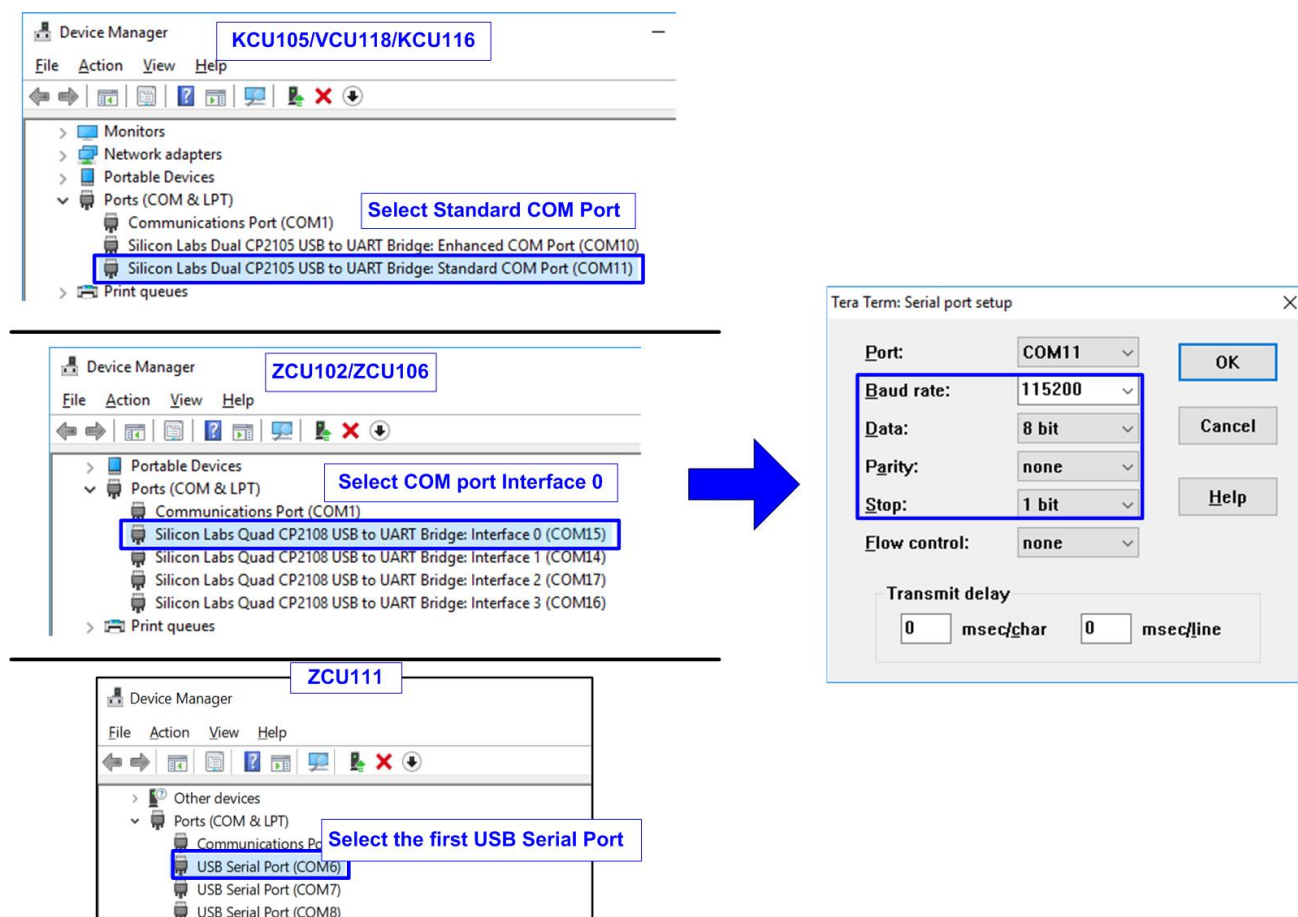


Figure 2-13 COM port number for Serial console

- 8) Download configuration file and firmware to the FPGA board
- a) For ZCU102/ZCU106/ZC706/ZCU111 boards, open the Vivado TCL shell and change the current directory to the download folder that includes the demo configuration file. Type “XXX10gtest\_boardname.bat”, as shown in Figure 2-14.

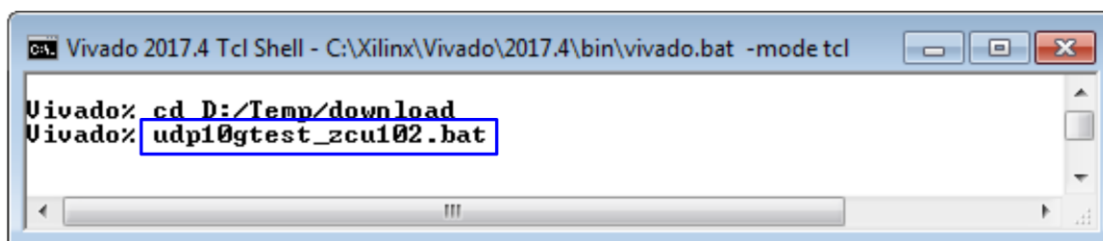


Figure 2-14 Example command script for download to ZCU102/ZCU106/ZC706 by Vivado tool

- b) For KCU105/VCU118/KCU116 boards, use the Vivado tool to program the configuration file, as shown in Figure 2-15.

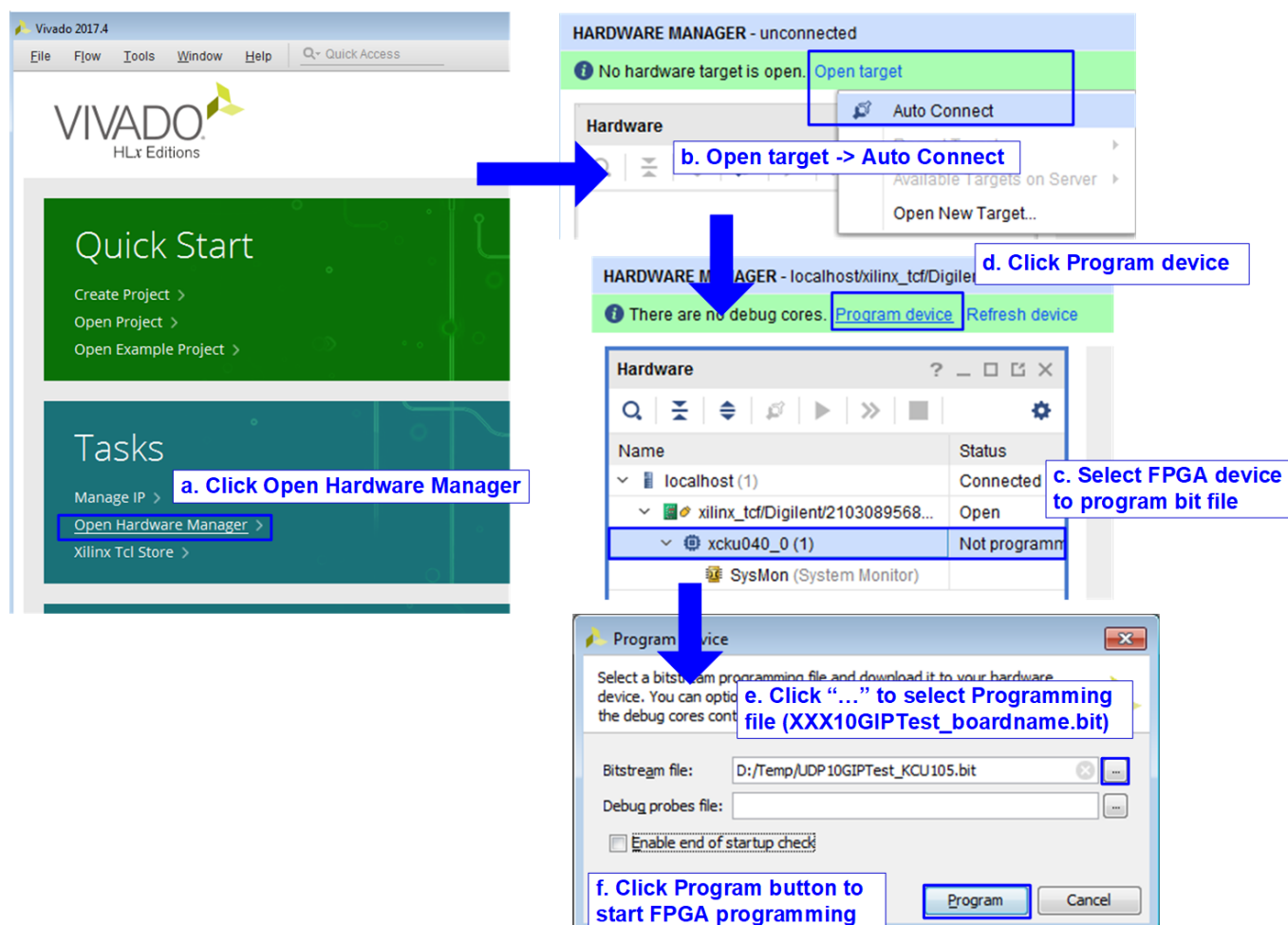


Figure 2-15 Program FPGA by Vivado

- 9) Upon opening the Serial console, a welcome message will be displayed.
  - i) Input '0' to initialize the TOE10G-IP/UDP10G-IP in Client mode that asks for the PC MAC address through sending ARP request packet.
  - ii) The default parameter in Client mode will be shown on the console.

TOE10G-IP	UDP10G-IP
<pre> +++ TOE10GIP with CPU Demo [IPVer = 1.17] Input mode : [0] Client [1] Server =&gt; 0  +++ Current Network Parameter +++ Window Update Gap = 0 Reverse Packet    = ENABLE Mode              = CLIENT FPGA MAC address  = 0x000102030405 FPGA IP           = 192.168.7.42 FPGA port number  = 60000 Target IP         = 192.168.7.25 Target port number = 60001 Press 'x' to skip parameter setting:           </pre>	<pre> +++ UDP10GIP with CPU Demo [IPVer = 1.5] Input mode : [0] Client [1] Server =&gt; 0  +++ Current Network Parameter +++ Mode              = CLIENT FPGA MAC address  = 0x000102030405 FPGA IP           = 192.168.7.42 FPGA port number  = 4000 Target IP         = 192.168.7.25 Target port number (Target-&gt;FPGA) = 61000 Target port number (FPGA-&gt;Target) = 60000 Press 'x' to skip parameter setting:           </pre>

◆ : User Input  
 ◆ : User Output

Figure 2-16 Message after system boot-up

However, if there is an Ethernet connection problem and the status is linked down, an error message will be displayed instead of the welcome message, as shown in Figure 2-17.

```

+++ UDP10GIP with CPU Demo [IPVer = 1.5] ++
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
          
```

Figure 2-17 Error message when ethernet connection is down



- iii) If the user wishes to skip parameter setting and use default parameters to start the system initialization, input 'x' as shown in Figure 2-18. If any other keys are entered, the menu for changing parameter will appear, similar to the “Reset TCPIP/UDPIP parameters” menu. The examples of running the main menu of TOE10G-IP and UDP10G-IP are described in “dg\_toe10gip\_cpu\_instruction” and “dg\_udp10gip\_cpu\_instruction” document, respectively.

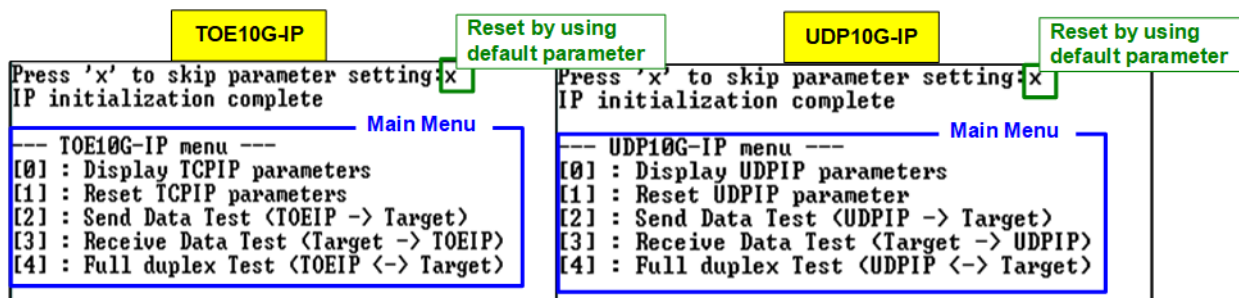


Figure 2-18 Initialization complete

*Note: The transfer performance in the demo is reliant on the PC resource in Test platform.*

### 3 Test environment setup using two FPGAs

Before running the demo using two FPGAs, please prepare the following.

- Two FPGA development boards, which can either be the same or different boards, such as ZC706/ZCU102/ZCU106/KCU105/VCU118/KCU116/ZCU111
- 10G Ethernet cable:
  - a) 10 Gb SFP+ Active Optical Cable (AOC)
  - b) 2x10 Gb SFP+ transceiver (10G BASE-R) with optical cable (LC to LC, Multimode)
  - c) For VCU118, use QSFP+ to 4 SFP+ cable
- Micro USB cables for programming the FPGA and connecting between FPGA board and PC
- Mini USB cable (ZC706 board) or micro USB cable (ZCU102/KCU105/VCU118/KCU116 board) for Serial console, connecting between FPGA board and PC
- Serial console software such as TeraTerm, installed on PC. The console setting is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming the FPGA installed on the PC

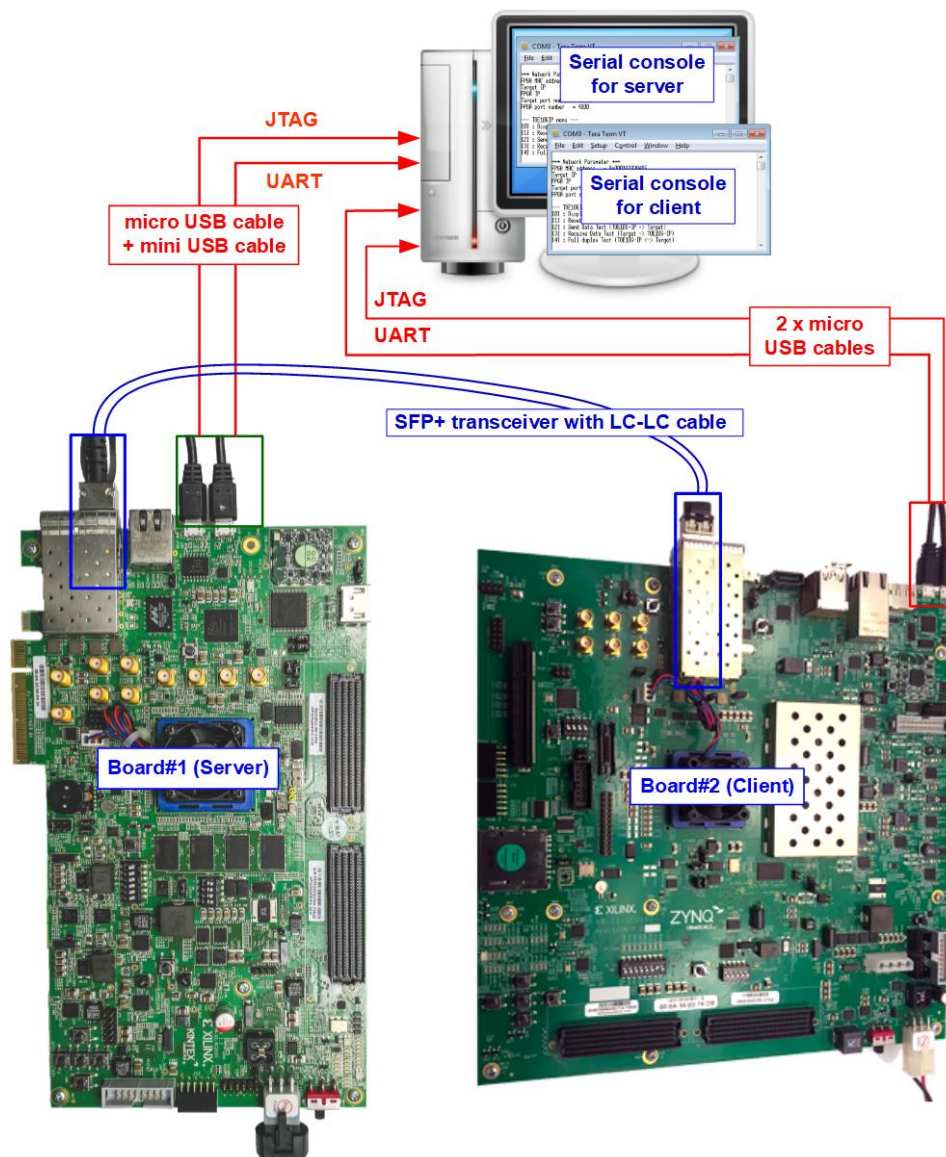


Figure 3-1 TOE10G-IP/UDP10G-IP with CPU demo (FPGA<->FPGA)

The steps for setting up a test environment using two FPGAs are described below.

To begin, follow steps 1) – 8) of Topic 2 (Test environment setup using an FPGA and PC) to prepare the FPGA board and SFP+ connection for running the demo. Once the two FPGA boards have been completely configured, the Serial console will display a menu to select Client or Server mode. Below shows the next steps in details.

- 1) Open the Serial console for FPGA board#1 and FPGA board#2, which are set to initialize in Server mode and Client mode, respectively.
  - i) Set '1' on the Serial console of FPGA board#1 for running in Server mode.
  - ii) Set '0' on the Serial console of FPGA board#2 for running in Client mode.
  - iii) The default parameters for the selected mode will be displayed on the console, as shown in Figure 3-2.

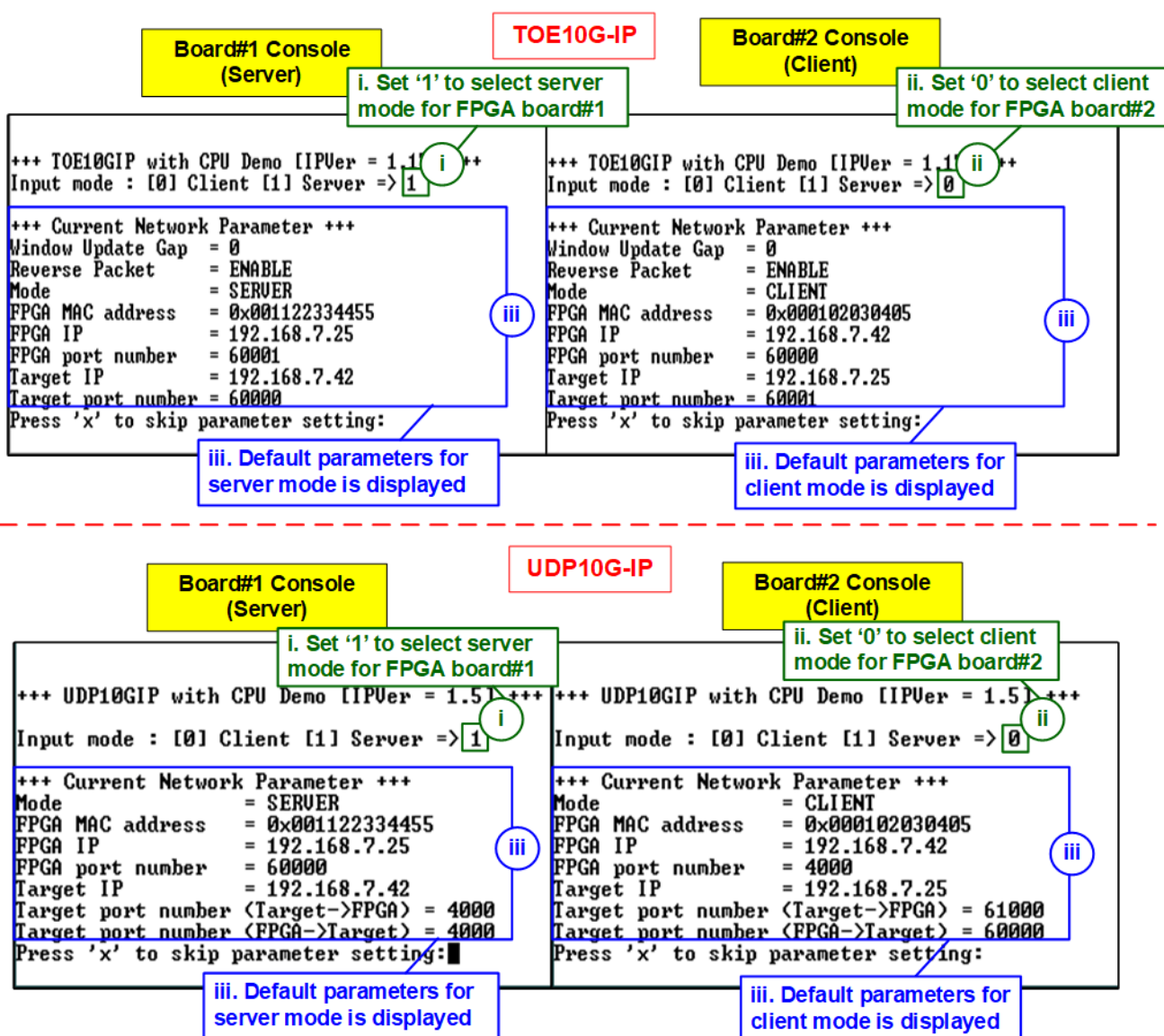


Figure 3-2 Input mode

- 2) Input 'x' to use default parameters, or use other keys to change parameters. The parameters of Server mode must be set before Client mode.

When running TOE10G-IP,

- i) Set parameters on the Server Serial console (board#1 console).
- ii) Set parameters on the Client Serial console (board#2 console) to start IP initialization by transferring ARP packet.
- iii) After finishing the initialization process, "IP initialization complete" and the main menu will be displayed on the Server and Client consoles.

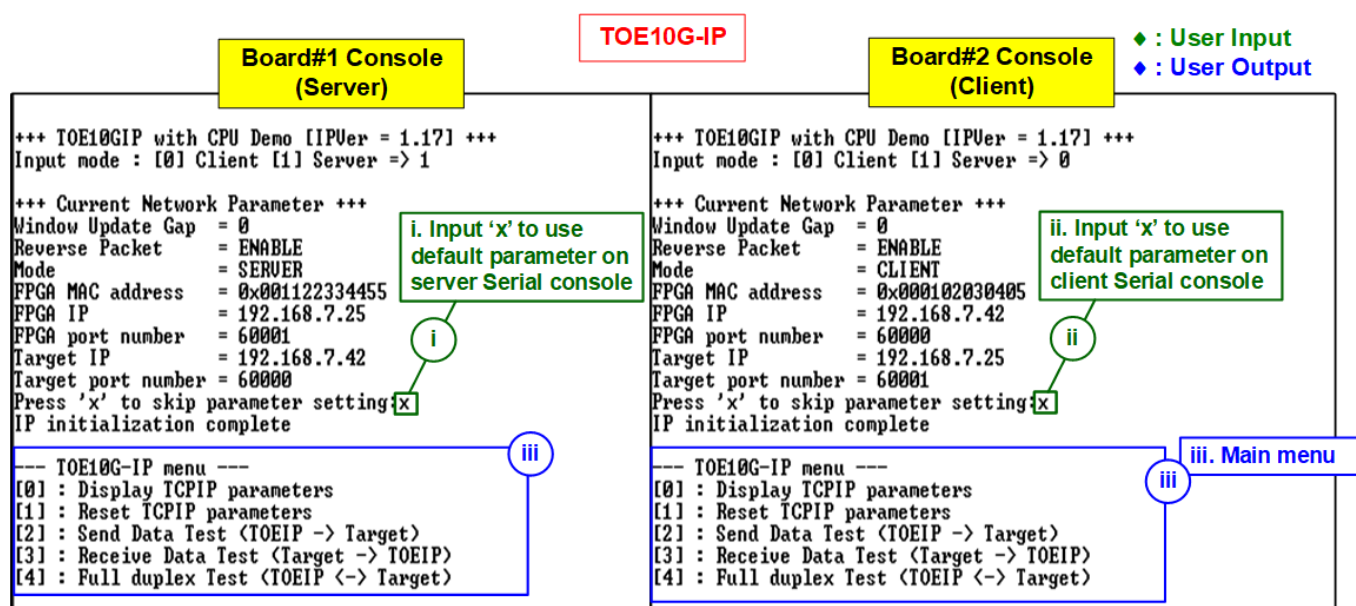


Figure 3-3 Main menu of TOE10G-IP

When running UDP10G-IP,

- i) For Server mode (board#1 console), if user does not change the default parameters, input 'x' to skip parameter setting.
- ii) For Client mode, the user must change Target port number (Target->FPGA) to use same value as Target port number (FPGA->Target).
- iii) After finishing initialization process, "IP initialization complete" and the main menu will be displayed on the Server and Client consoles.

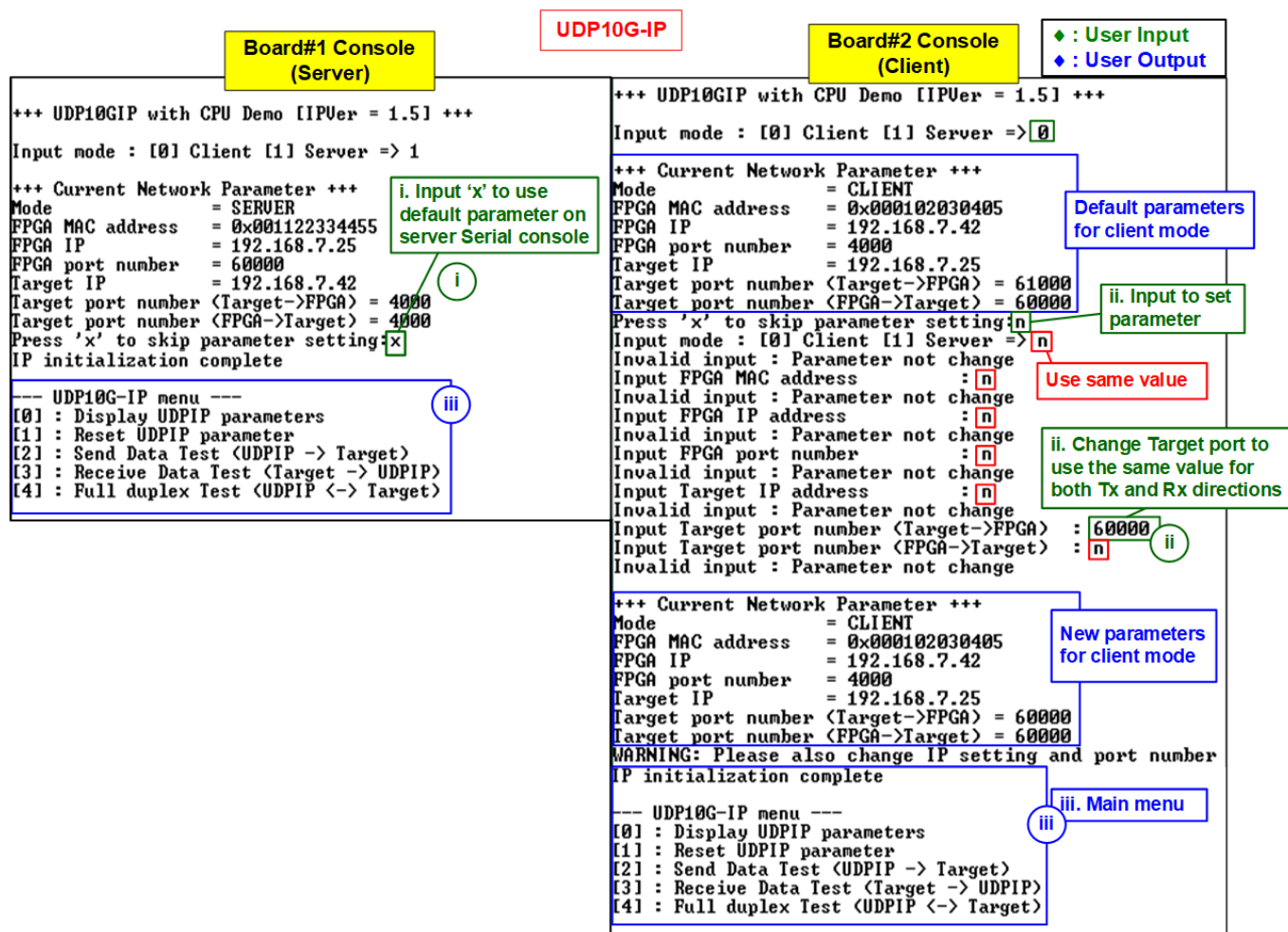


Figure 3-4 Main menu of UDP10G-IP

## 4 Revision History

Revision	Date	Description
3.3	13-Mar-23	Update Figure 2-9
3.2	9-Mar-23	Add KCU116 and ZCU111 boards
3.1	15-Mar-22	Update Figure 2-16, Figure 3-2, and Figure 3-3
3.0	21-Aug-20	TOE10G-IP and UDP10G-IP
2.0	21-Jul-20	Remove test result on the console
1.1	8-Mar-19	Support FPGA <-> FPGA test and ZCU102
1.0	15-Sep-17	Initial version release