TOE1G-IP Two-Port Demo Instruction

Rev1.2 2-Sep-16

1 Environment Setup

As shown in Figure 1 – Figure 2, to run TOE1G-IP FTP demo, please prepare

1) FPGA Development board (AC701/KC705/ZC706)
2) ISE ver 14.4 or later, or Vivado tool
3) For ZC706 board, use SFP-RJ45 adapter

Note: The demo uses FCLF-8520-3/FCLF-8521-3 to be SFP-RJ45 adapter
https://www.finisar.com/sites/default/files/downloads/finisar_fclf-8520-3_fclf-8521-3_1000base-t_copper_sfp_optical_transceiver_productspecreve1.pdf

4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
5) PC with Gigabit Ethernet support
6) micro USB cable for programming FPGA between FPGA Development board and PC
7) “send_tcp_client.exe” and “recv_tcp_client_single.exe”, provided by Design Gateway to be test application on PC
8) USB mini cable for Serial interface between FPGA Development board and PC

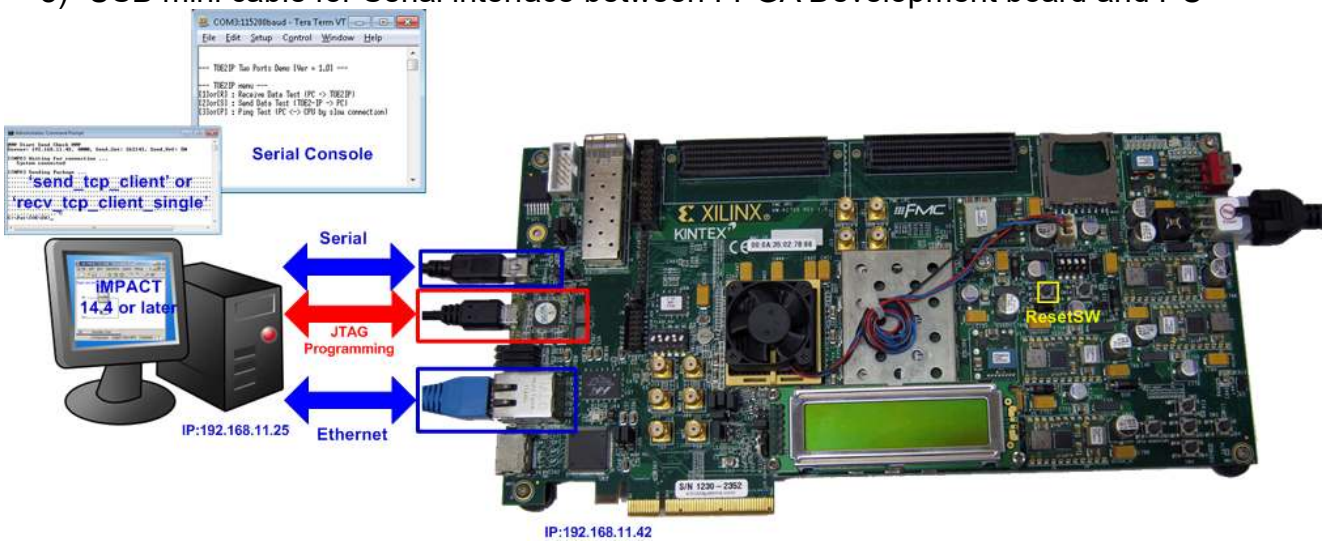

Figure 1 TOE1G-IP Two-Port Demo Environment Setup on KC705

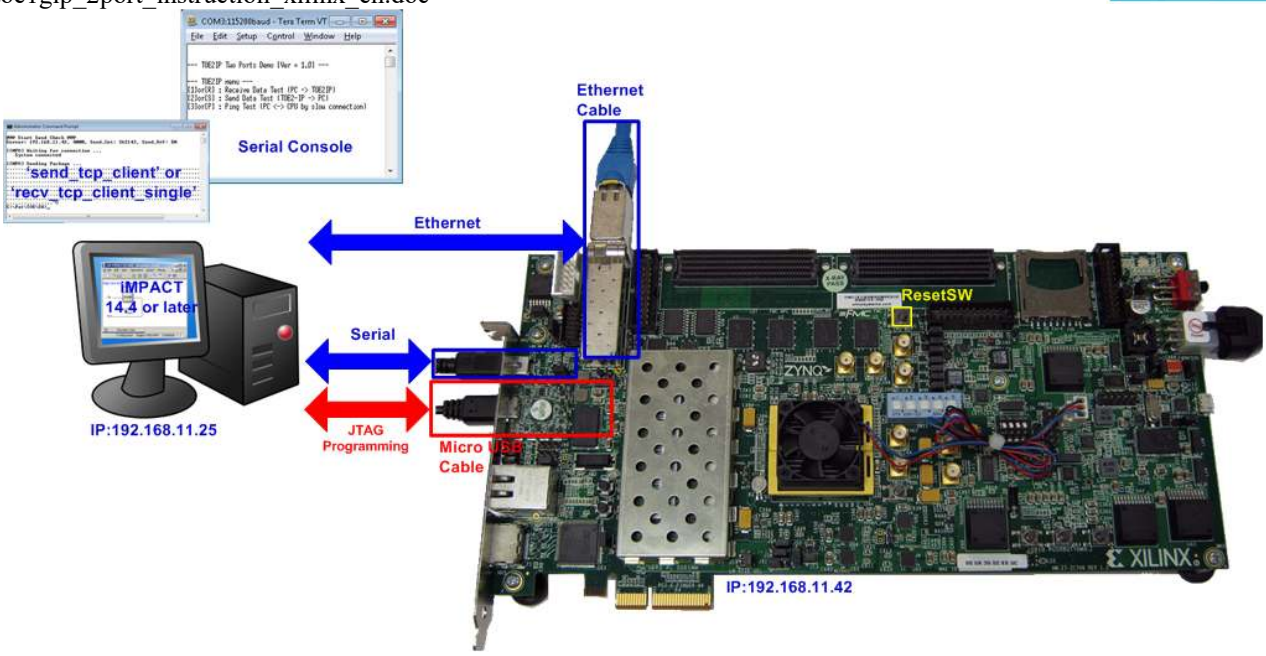

Figure 2 TOE1G-IP Two-Port Demo Environment Setup on ZC706

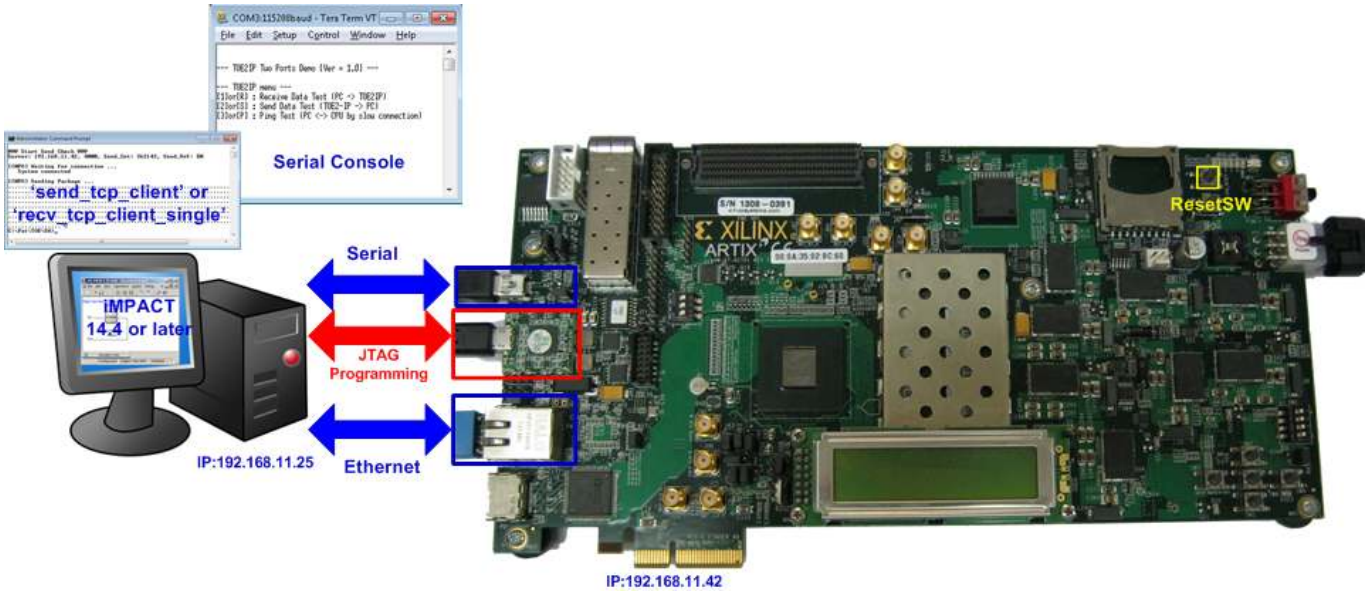

Figure 3 TOE1G-IP Two-Port Demo Environment Setup on AC701

2 Demo description

The demo designs three test operations in the main menu, i.e. fast data reception by "send_tcp_client.exe", fast data transmission by "recv_tcp_client_single.exe", and slow data connection by Ping command. Each test operation on FPGA board uses different test application on PC. LEDs on FPGA are mapped to show the status of fast data connection only, as shown in Table 1.

Table 1 LED Definition

GPIO LED	ON	OFF
0	Data transferring	No data connection
1/R	TOE1G-IP receives data from PC	No received data from PC
2/C	Data transferring from TOE1G-IP to PC	No data transferring
3/L	Data transferring from PC to TOE1G-IP	No data transferring

3 PC Setup

Please follow the same setting as described in "dg_toe1gip_instruction_xilinx_en" document (standard demo).

4 How to run demo

4.1 FPGA Programming

To run the demo, please follow these steps.

- For ZC706 board only, set SW11=”00000” to configure PS from JTAG and set SW4=”01” to connect JTAG with USB-to-JTAG interface, as shown in Figure 4 – Figure 5.

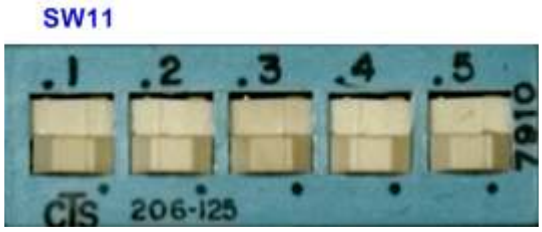

Figure 4 SW11 setting to configure PS from JTAG on ZC706 board

Figure 5 SW4 setting to use USB-to-JTAG on ZC706 board

- Connect micro USB cable from FPGA development board to PC and connect power supply to FPGA board.
- Connect USB mini cable from FPGA development board to PC and open serial monitoring software on PC such as HyperTerminal. Terminal setting is BuadRate=115200, Data=8 bit, Non-Parity, Stop=1.
- Connect Ethernet cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- For KC705/AC701, open iMPACT and download “download_twoport.bit” to FPGA development board. After download completely, 1000 link status LED at DS11 (near RJ45) on KC705 will be ON while DS11 on AC701 will be OFF to show that the Ethernet link is ready, as shown in Figure 6.

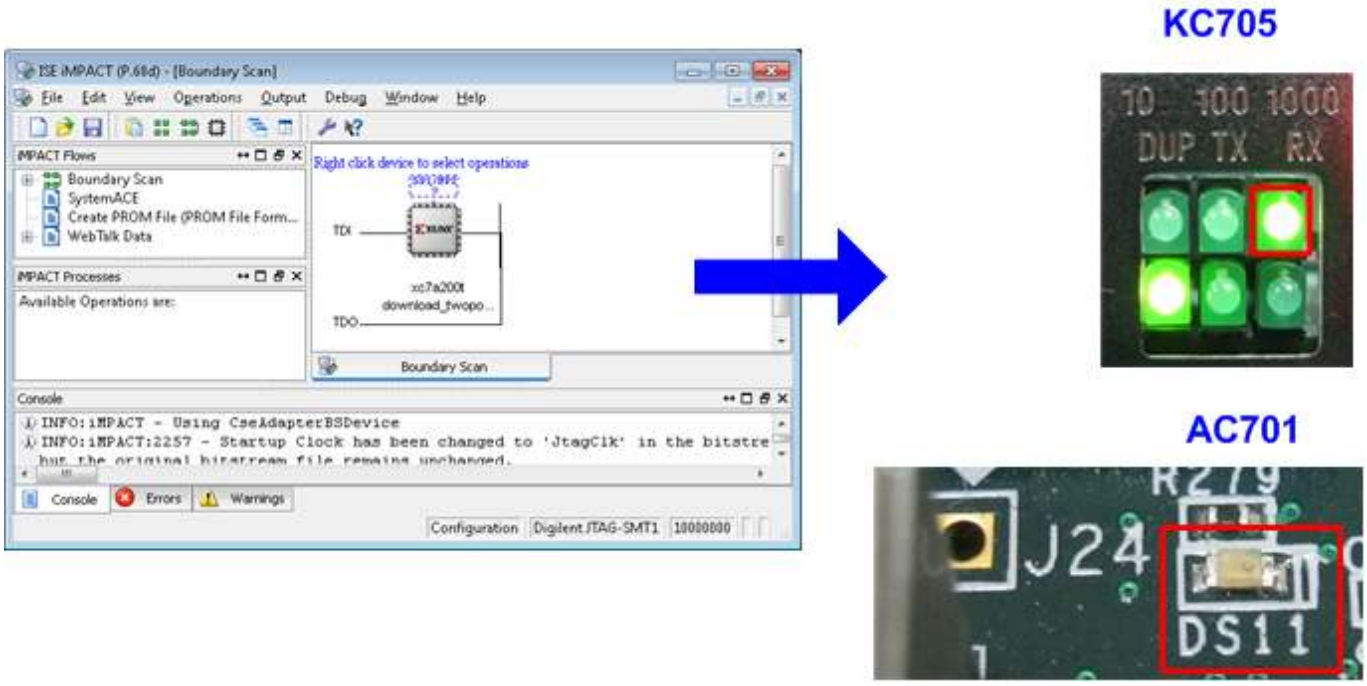

Figure 6 Programmer Environment

- For ZC706, open ISE command prompt or Vivado TCL Shell, change current directory to ready_for_download, and run batch file as shown in Figure 7 – Figure 8. There is no Ethernet LED status on ZC706, so user can check from message on Serial console instead.

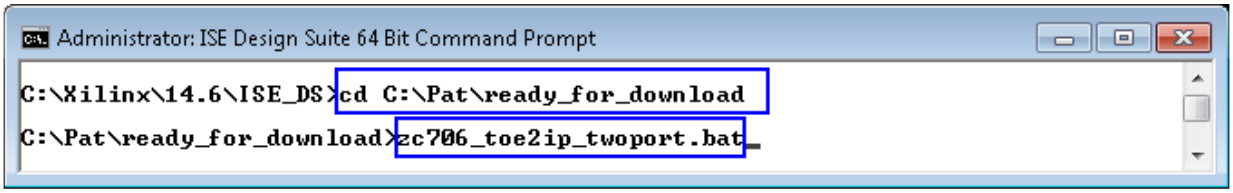

Figure 7 Example command script for download to ZC706 by ISE tool

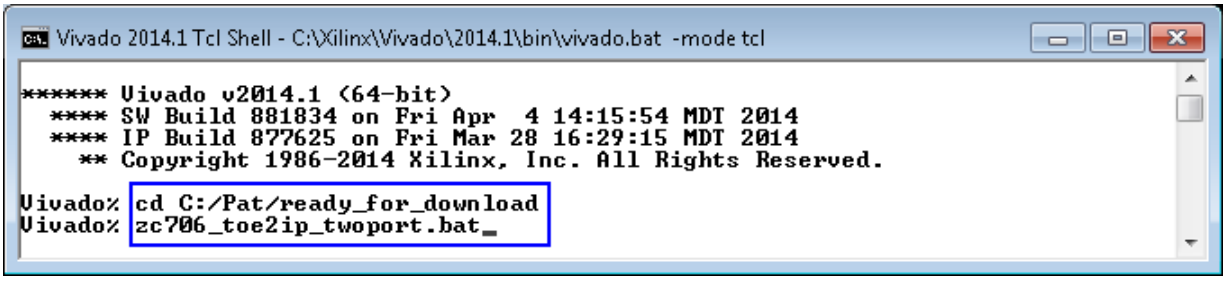

Figure 8 Example command script for download to ZC706 by Vivado tool

- On serial console, Main menu will be displayed when FPGA can detect PC in the network. If last message is “Wait network connection”, please check LAN cable and Ethernet connection setting on PC.

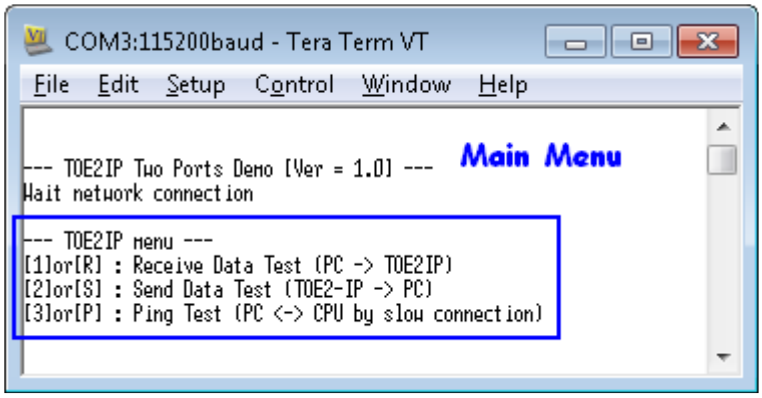

Figure 9 Main Menu

4.2 Run Test operation

Though hardware can support to transfer data in both TX/RX directions and both fast/slow connections at the same time, the demo designs to test only one mode for easily test. There are three test operations following the main menu, i.e.

(1) Receive Data Test: This test transfers data from PC to FPGA through fast connection. "send_tcp_client" application is used to run on PC during the test.

(2) Send Data Test: This test transfers data from FPGA to PC through fast connection. "recv_tcp_client_single" application is used to run on PC during the test.

(3) Ping Test: This test transfers data in both directions between FPGA and PC through slow connection. "ping" command is used to run on PC during the test.

More details about each test operation are described as follows.

4.2.1 Receive Data Test

The step to test on this mode is follows.

(1) On Serial console, user inputs [1] or [R] key. After that, message as shown in Figure 10 is displayed.

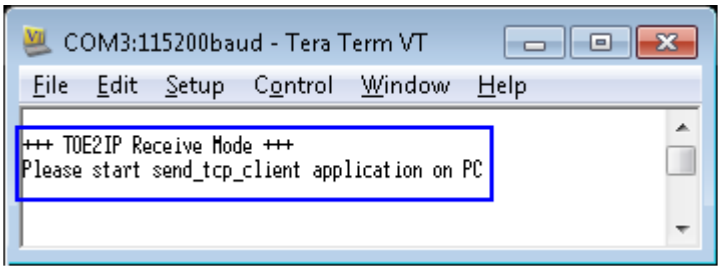

Figure 10 Message when run Receive Data Test

(2) Open command prompt, and run "send_tcp_client" application on PC, as shown in Figure 11. There are four input parameters for this application, i.e.

a) Destination IP address: IP address for TOE1G-IP in the demo is 192.168.11.42

b) Destination port: Fast connection port in the demo is 4000

c) Packet Count: Total number of 16kByte packets to send to FPGA. Valid from 1-262143. So, maximum transfer length is 4,294,950,912 bytes.

d) Test pattern: [0]-Dummy data, [1]-32 bit increment data. Mode0 uses less CPU resource than mode 1, so some PCs will show the better performance when run by mode 0. For high-performance PC, both modes can achieve same transfer performance.

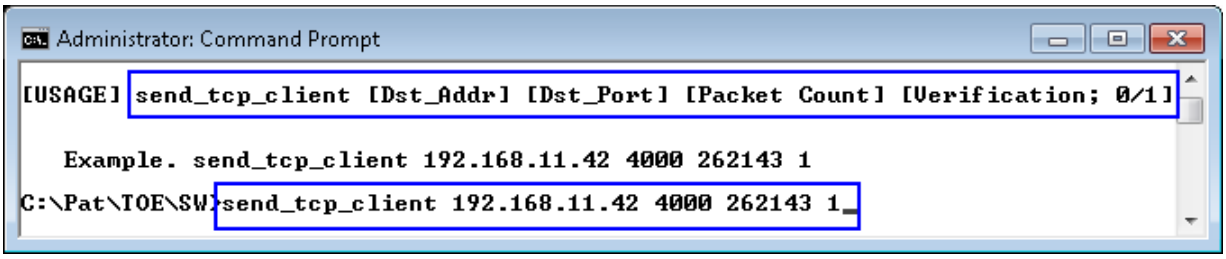

Figure 11 Run "send_tcp_client" application

Note: If user input any key to Serial console before running test application, the test will be cancelled and main menu will be displayed instead, as shown in Figure 12.

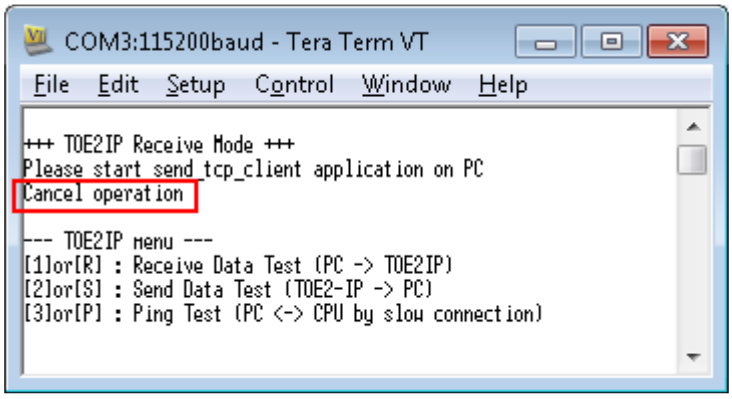

Figure 12 Cancel operation from user input during waiting send_tcp_client

(3) If total transfer size is more than 512 MB (Packet Count > 32768) which is buffer size in the demo, the menu to select data verification will not be displayed on Serial console. Transfer performance will be displayed on the PC while Serial console shows total transfer size, as shown in Figure 13.

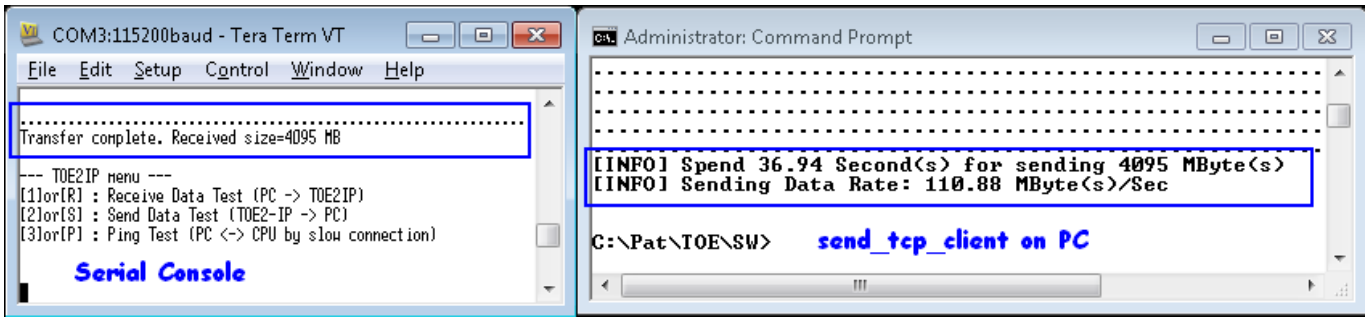

Figure 13 Test Result when transfer size is more than 512 MB

(4) If total transfer size is less than or equal 512 MB and transfer is completed, “Press Y/N to verify data” message will be displayed on Serial console, as shown in Figure 14. User can input ‘Y’/’N’ to run or skip data verification on FPGA. Data verification can be selected only when user inputs test pattern mode in “send_tcp_client”=1. If “send_tcp_client” runs in mode 0 (dummy data), it needs to input ‘N’ to disable data verification on FPGA, as shown in Figure 15.

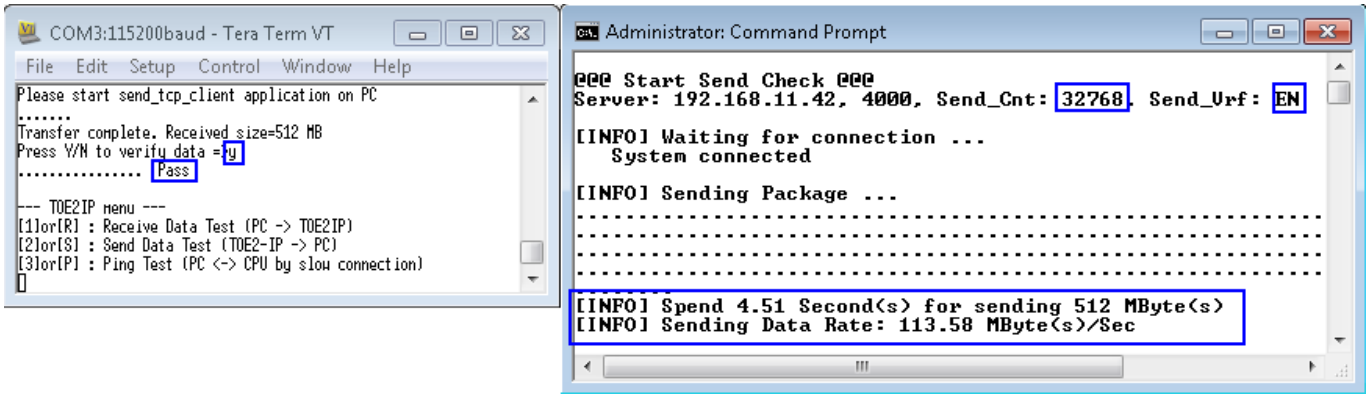

Figure 14 Test Result when enable data verification

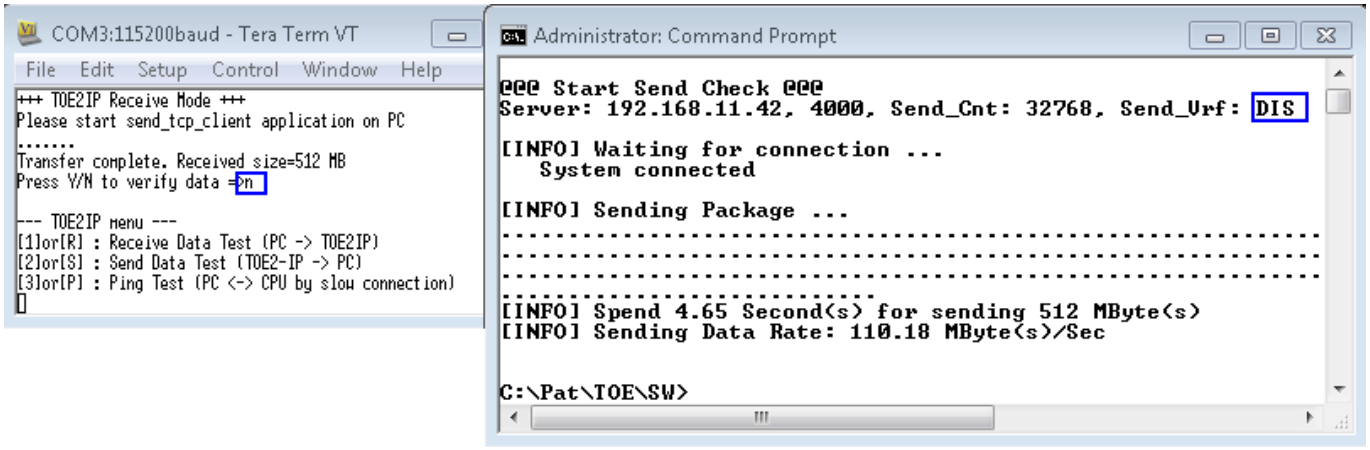

Figure 15 Test Result when disable data verification

If user enables data verification but dummy data is filled by test application, error message with error data will be displayed as shown in Figure 16.

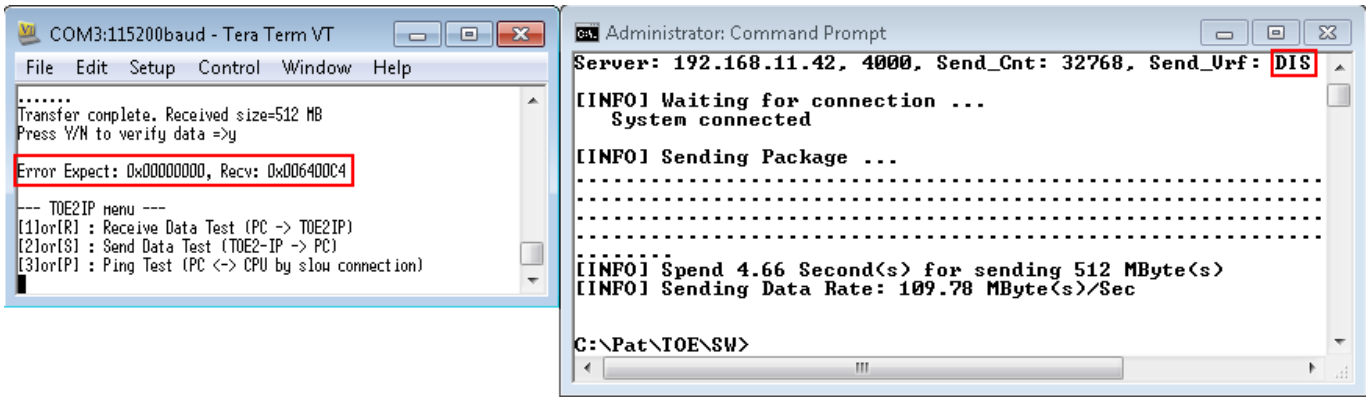

Figure 16 Error message on Serial console when data verification fail

4.2.2 Send Data Test

The step to test in this mode is follows.

(1) On Serial console, user inputs [2] or [S] key. After that, two or three input parameters are required, i.e.

a) Packet size: [0]-1460 byte (normal frame), [1]-8960 byte (jumbo frame)
b) Total transfer length: Valid from 1 – 0xFFFFFFFF.
c) Prepare test data: This input is displayed only when total transfer length is not more than 512 MB. Select 'Y' to fill increment test pattern, or 'N' to fill dummy data.

After that the console will show message with the recommended command to run "recv_tcp_client_single" test application on the console. Please copy this command from Serial console to command prompt for start test application.

Similar to Receive Data Test, if user input any key to Serial console before running test application, the test will be cancelled and main menu will be displayed instead

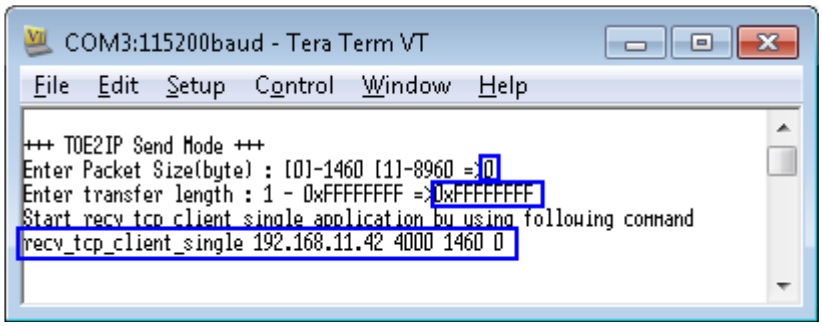

Figure 17 Input menu without test pattern selection (transfer length > 512 Mbyte)

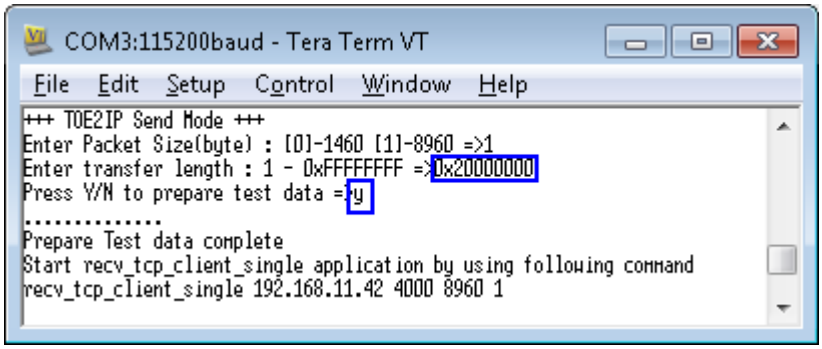

Figure 18 Input menu with test pattern selection (transfer length <= 512 Mbyte)

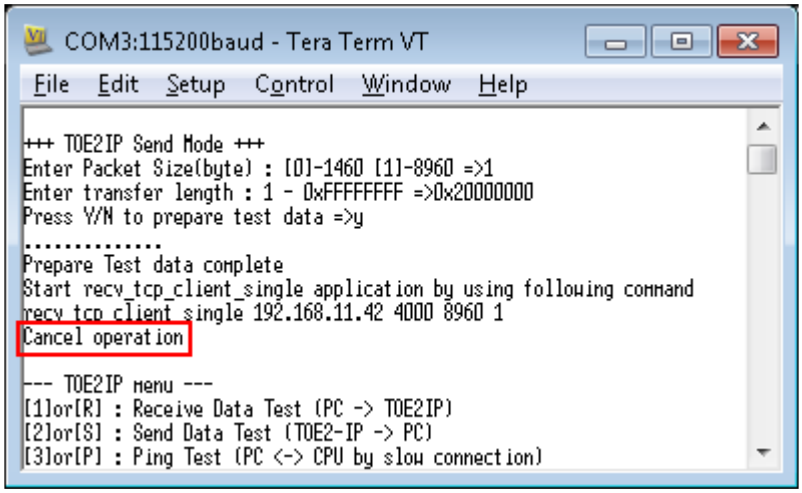

Figure 19 Cancel operation from user input during waiting recv_tcp_client_single

(2) Open command prompt, and run "recv_tcp_client_single" application on PC, as shown in Figure 20. There are four input parameters for this application, i.e.
   a) Destination IP address: IP address for TOE1G-IP in the demo is 192.168.11.42
   b) Destination port: Fast connection port in the demo is 4000
   c) Receive Length: Threshold value of the received data size in the application to start dump data out. Generally, this value is equal to packet size in the serial console. But if total transfer length is too less, it will be equal to total transfer length instead.
   d) Verification: [0]-No verification, [1]-Enable data verification. If enable data verification, some PC will get the less performance than no verification mode. But for high-performance PC, this parameter is not effect.
      User can select to enable data verification when total data transfer length is not more than 512 MB and increment test data is prepared by FPGA, not dummy data.

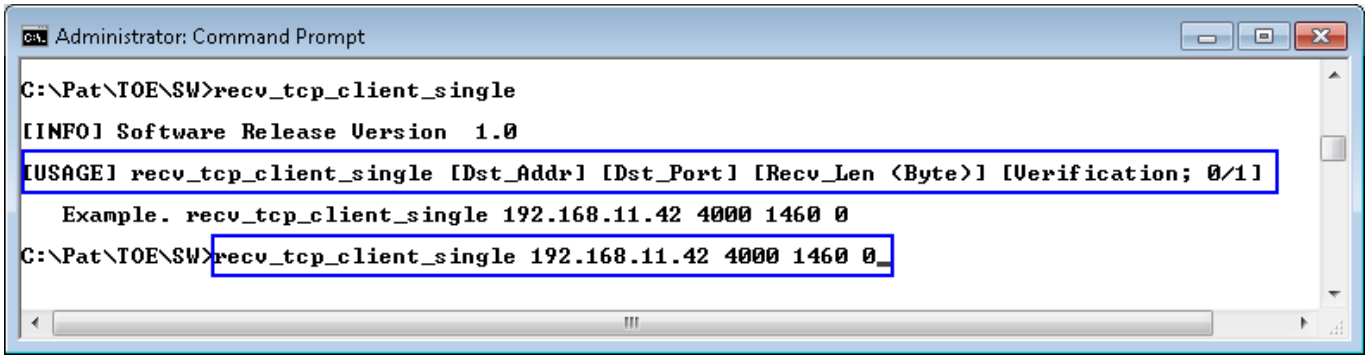

Figure 20 Run "recv_tcp_client_single" application

- Figure 21 and Figure 22 show the example test result when running dummy mode by 4 GB data size by using normal frame and jumbo frame, so test application must be run in mode 0 (no data verification).The performance is little better than normal frame when running by using jumbo frame.

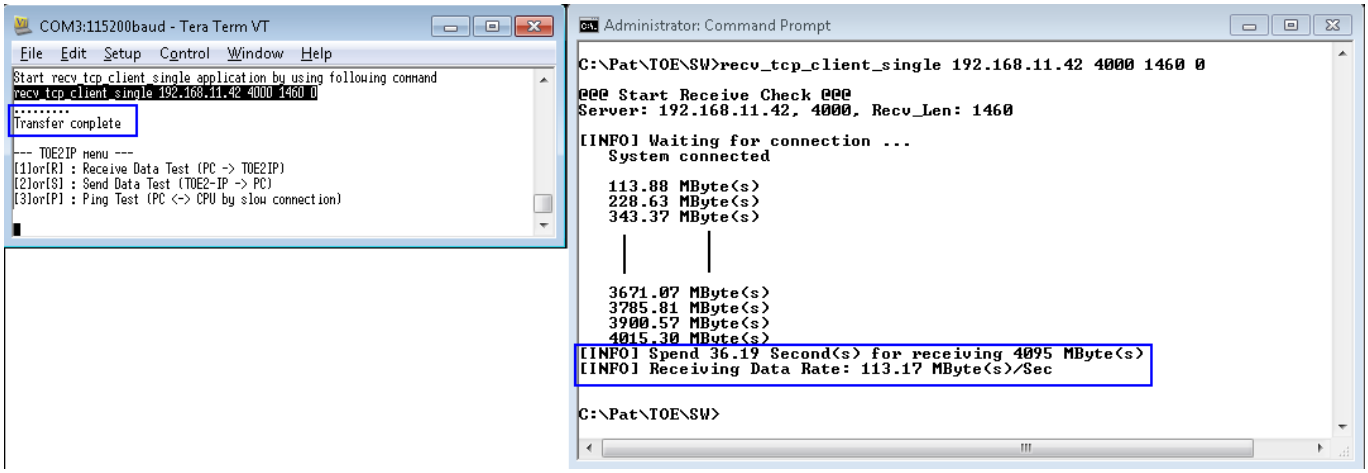

Figure 21 Test Result when no data verification (Packet size = 1460)

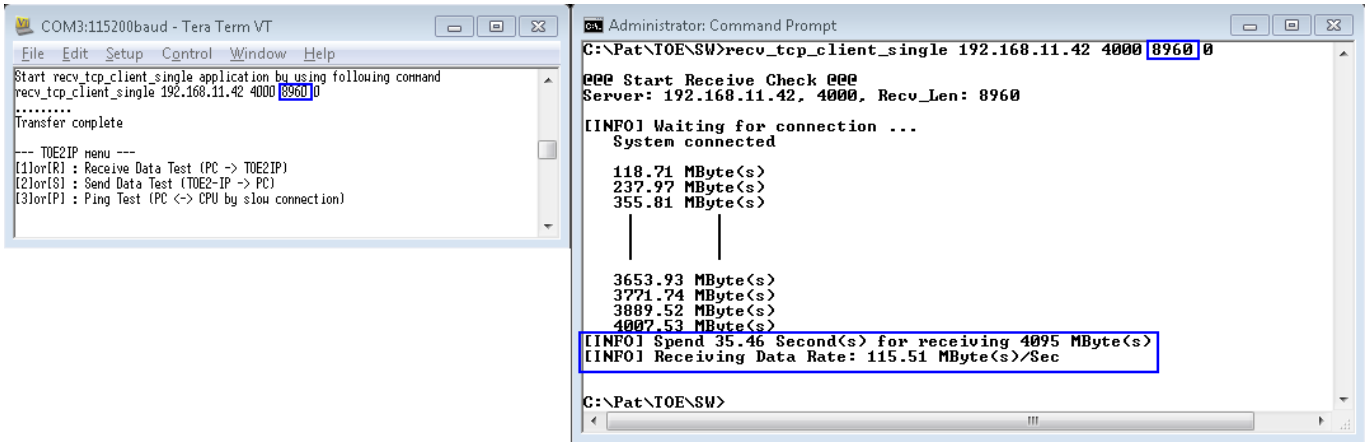

Figure 22 Test Result when no data verification (Packet size = 8960)

- Figure 23 and Figure 24 show the example test result when transfers 512 MB data with enable and disable data verification sequentially.
- Figure 25 shows the example error condition when run "recv_tcp_client_single" application to verify dummy data from FPGA which is not recommended command from Serial console.

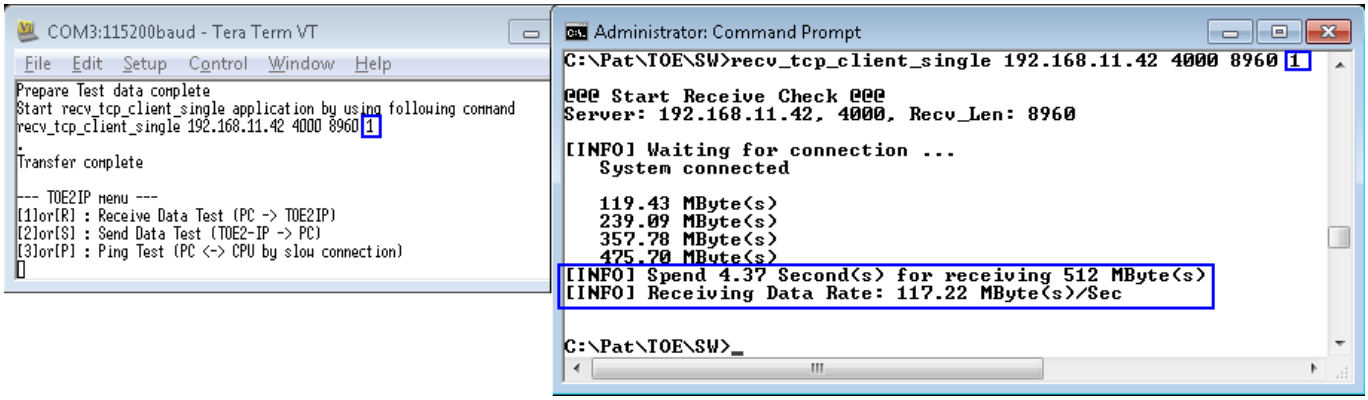

Figure 23 Test Result when enable data verification

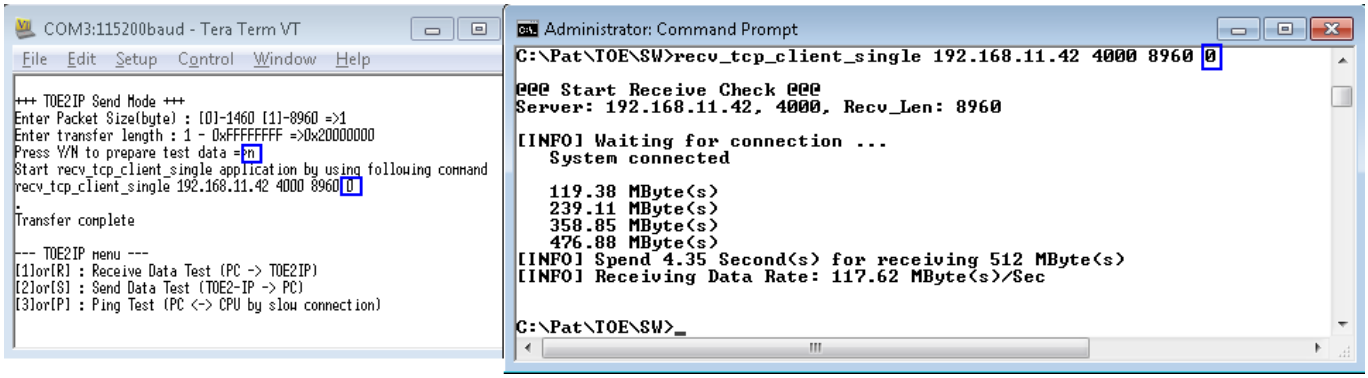

Figure 24 Test Result when disable data verification

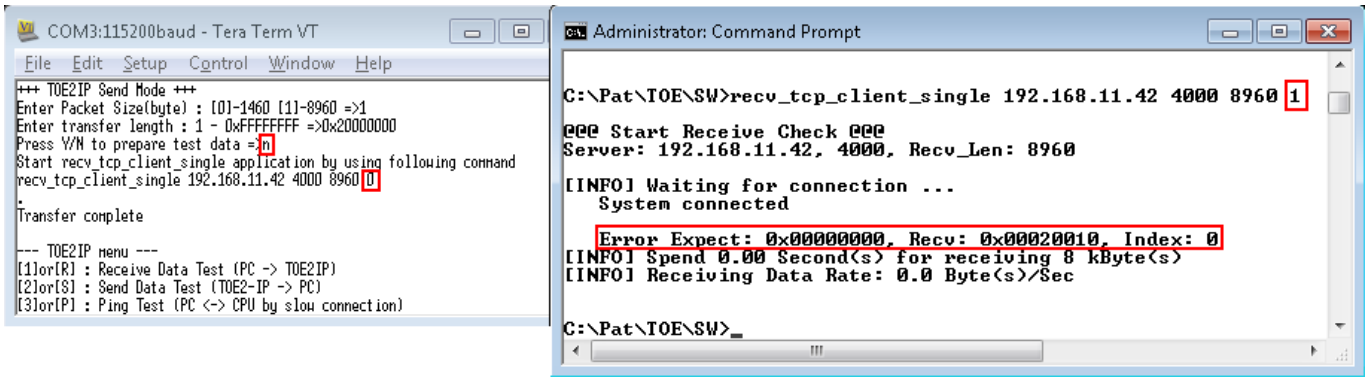

Figure 25 Error message on test application when data verification fail

4.2.3 Ping Test

The step to test on this mode is follows.

(1) On Serial console, user inputs [3] or [P] key. After that, “Please start run Ping command on PC” message will be displayed.

(2) Open command prompt and run ping command by using
>> ping 192.168.11.42
Note: In the demo, FPGA IP address is equal to 192.168.11.42.

(3) After ping test is completed, user can exit the test and go back to main menu by input any keyboard to Serial console.

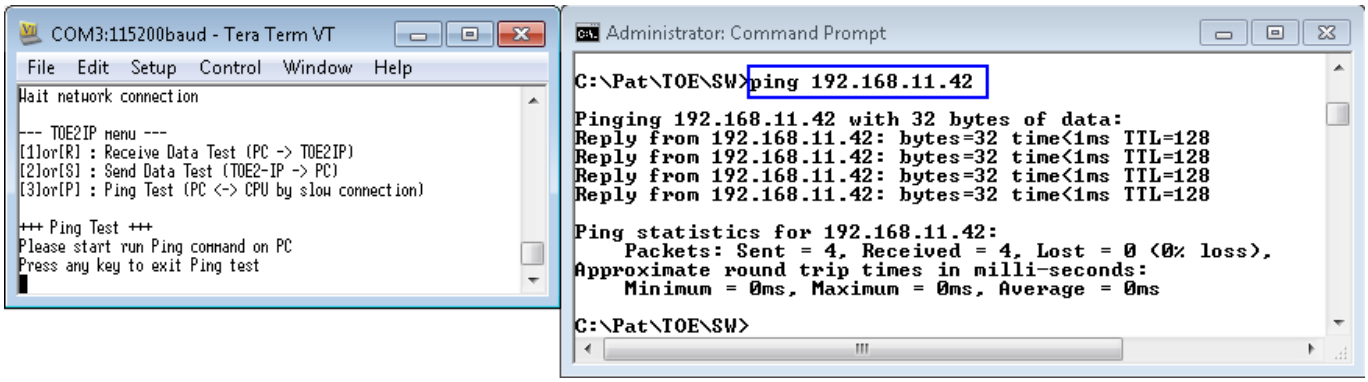

Figure 26 Ping command Test

5 Revision History

Revision	Date	Description
1.0	16-Jan-15	Initial version release
1.1	29-Dec-15	Add AC701 support
1.2	2-Sep-16	IP core product renamed from TOE2-IP to TOE1G-IP