TOE1G-IP Full Duplex Demo Instruction

Rev1.4 15-Nov-16

This document describes the instruction to run TOE1G-IP for transferring data between FPGA development board and PC in both directions at the same time through Gigabit Ethernet.

1 Environment Setup

As shown in Figure 1-1 – Figure 1-5, to run TOE1G-IP full duplex demo, please prepare

1) FPGA Development board: AC701/KC705/VC707/ZC706/Zynq Mini-ITX (Z100 model)
2) Xilinx programmer software (iMPACT/Vivado)
3) For ZC706/Zynq Mini-ITX board: SFP-RJ45 adapter
4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
5) PC with Gigabit Ethernet support
6) micro USB cable for programming FPGA between FPGA Development board and PC
7) Test Application “tcp_client_txrx.exe” running on PC, provided by Design Gateway

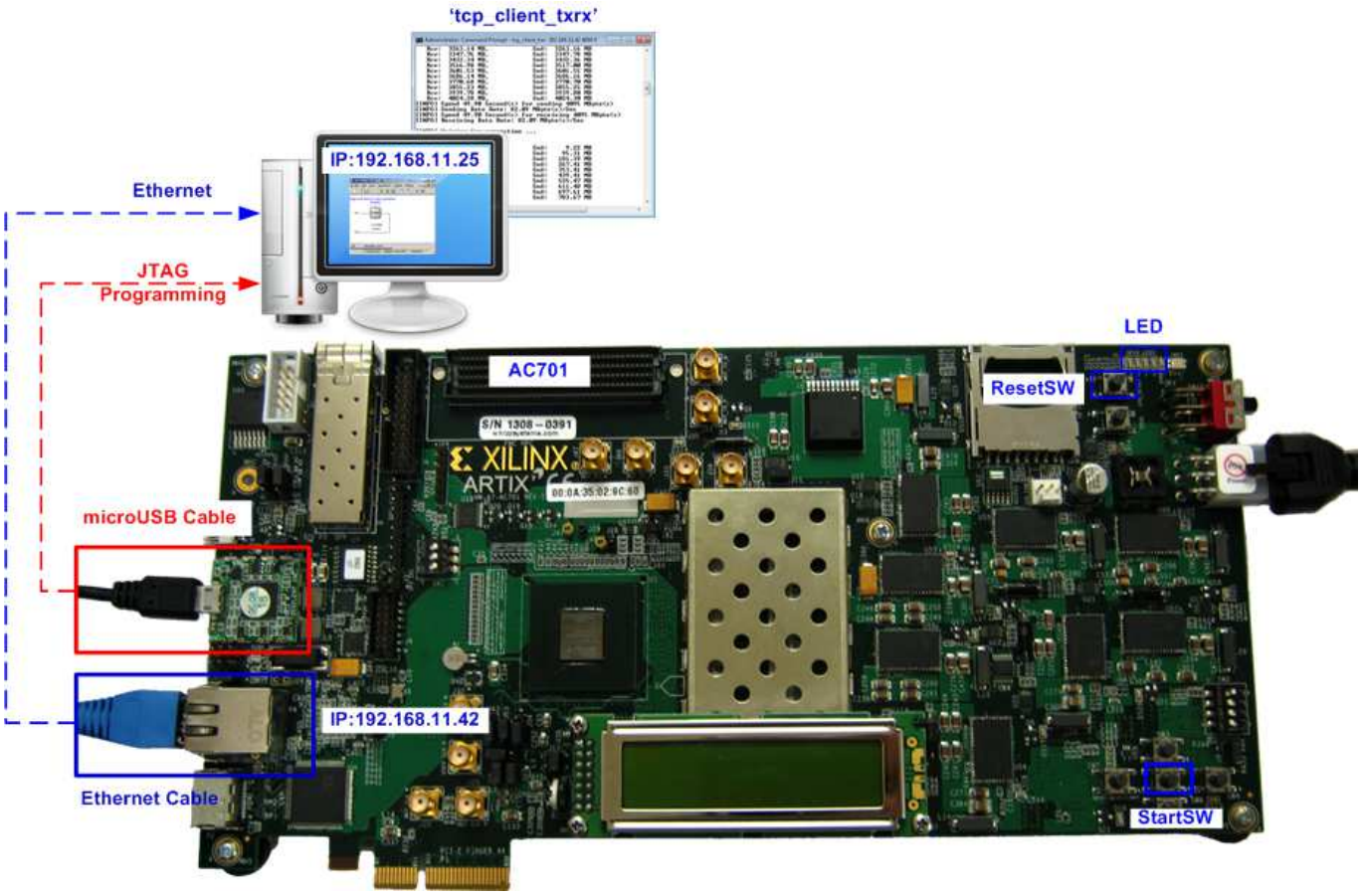

Figure 1-1 TOE1G-IP Full Duplex Demo Environment Setup on AC701

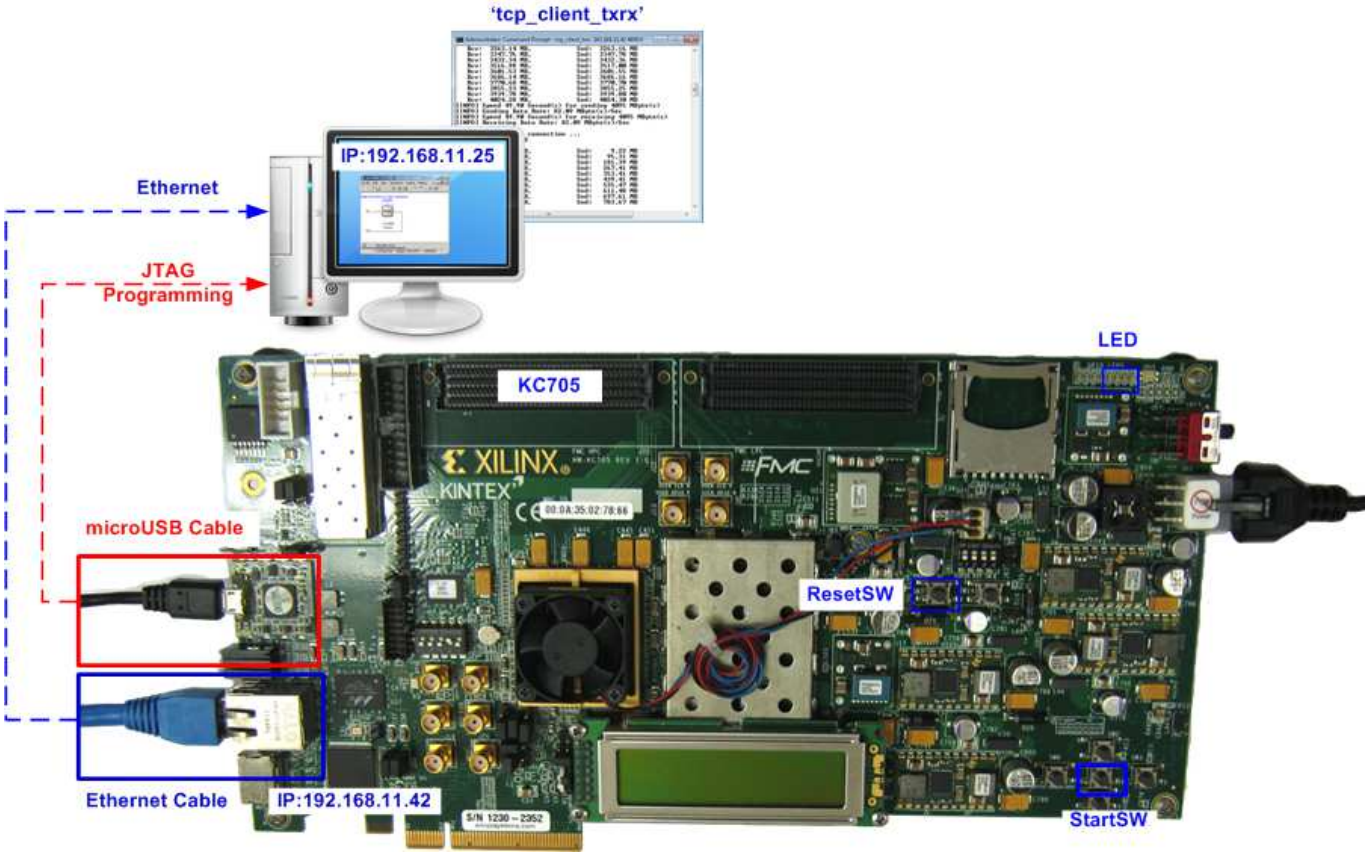

Figure 1-2 TOE1G-IP Full Duplex Demo Environment Setup on KC705

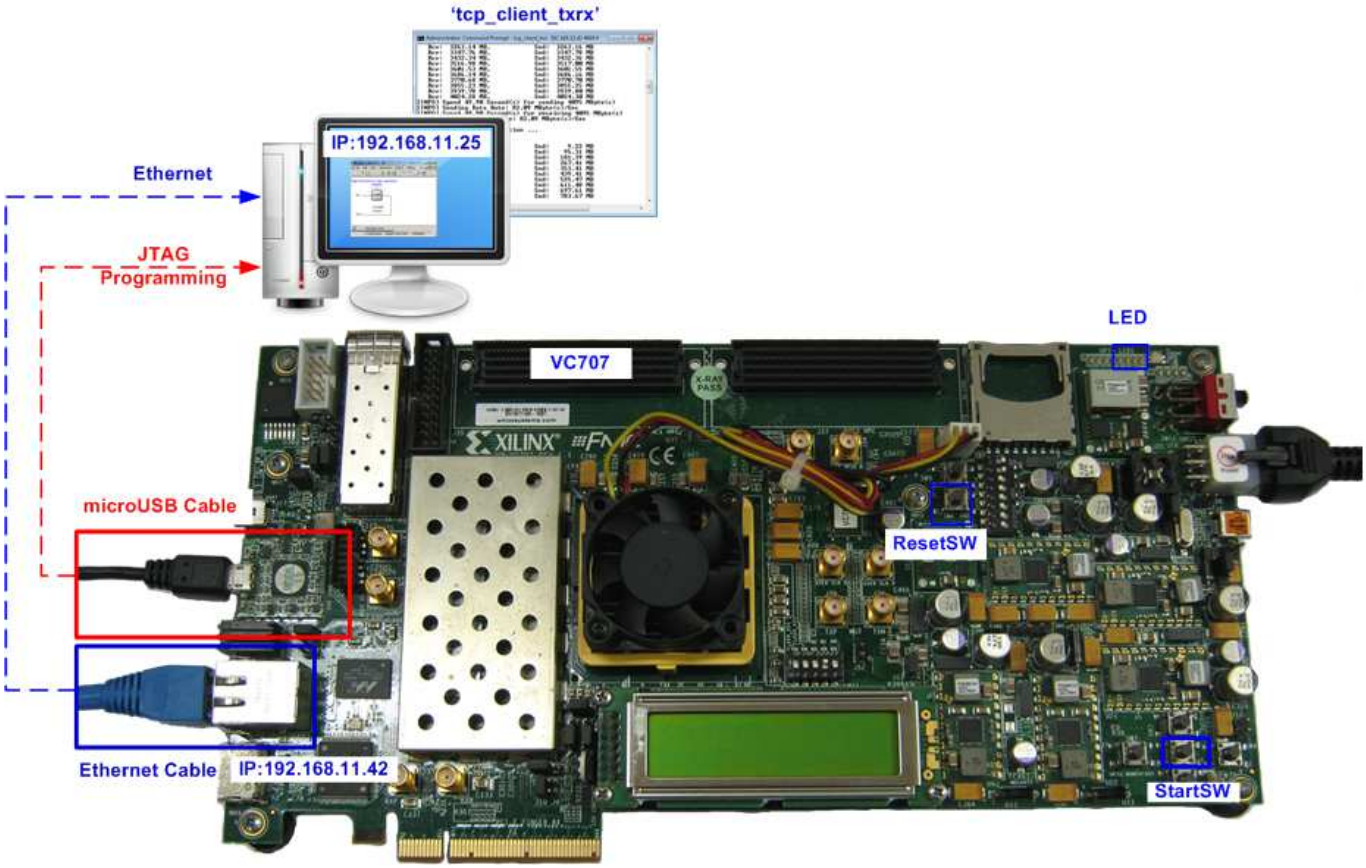

Figure 1-3 TOE1G-IP Full Duplex Demo Environment Setup on VC707

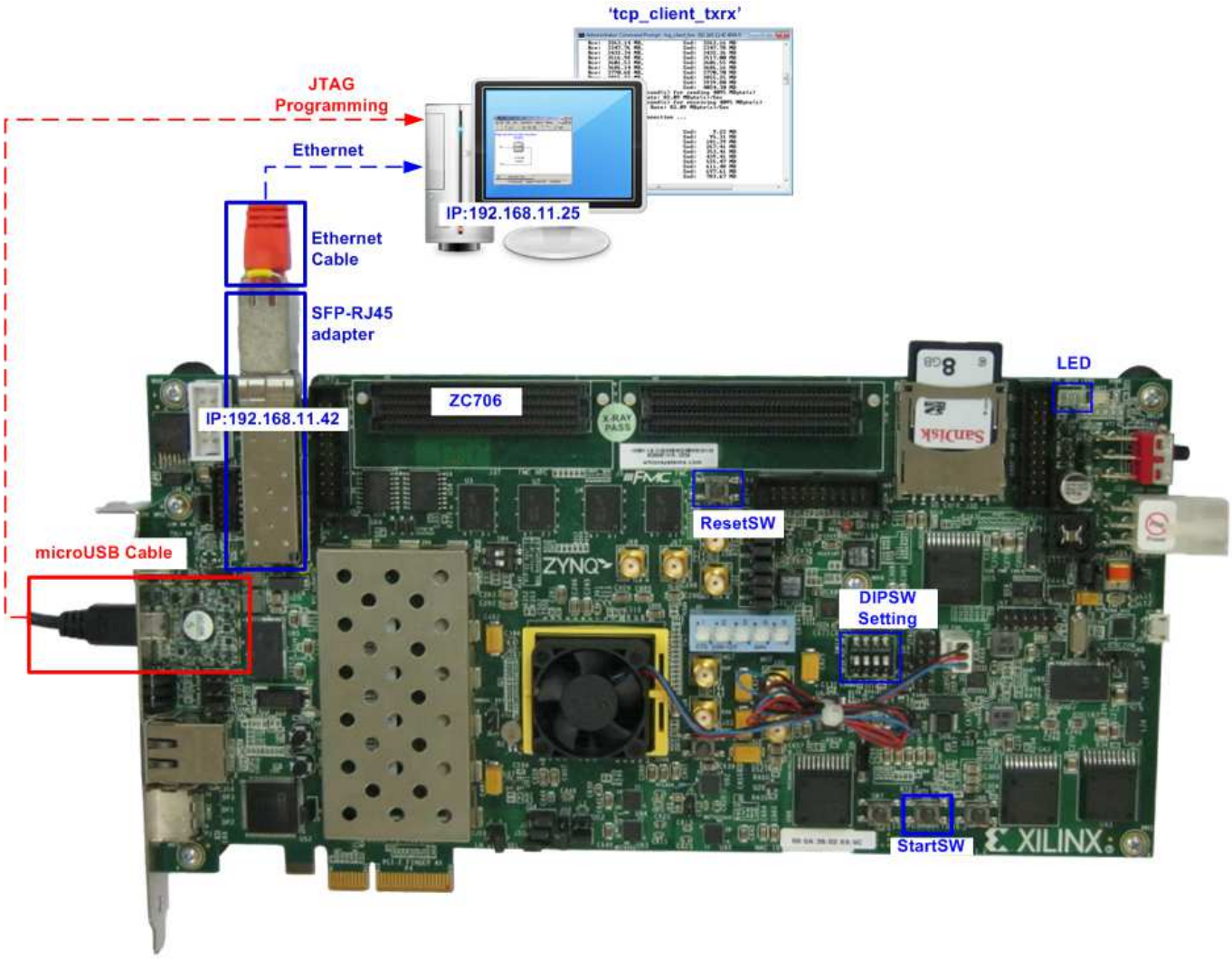

Figure 1-4 TOE1G-IP Full Duplex Demo Environment Setup on ZC706

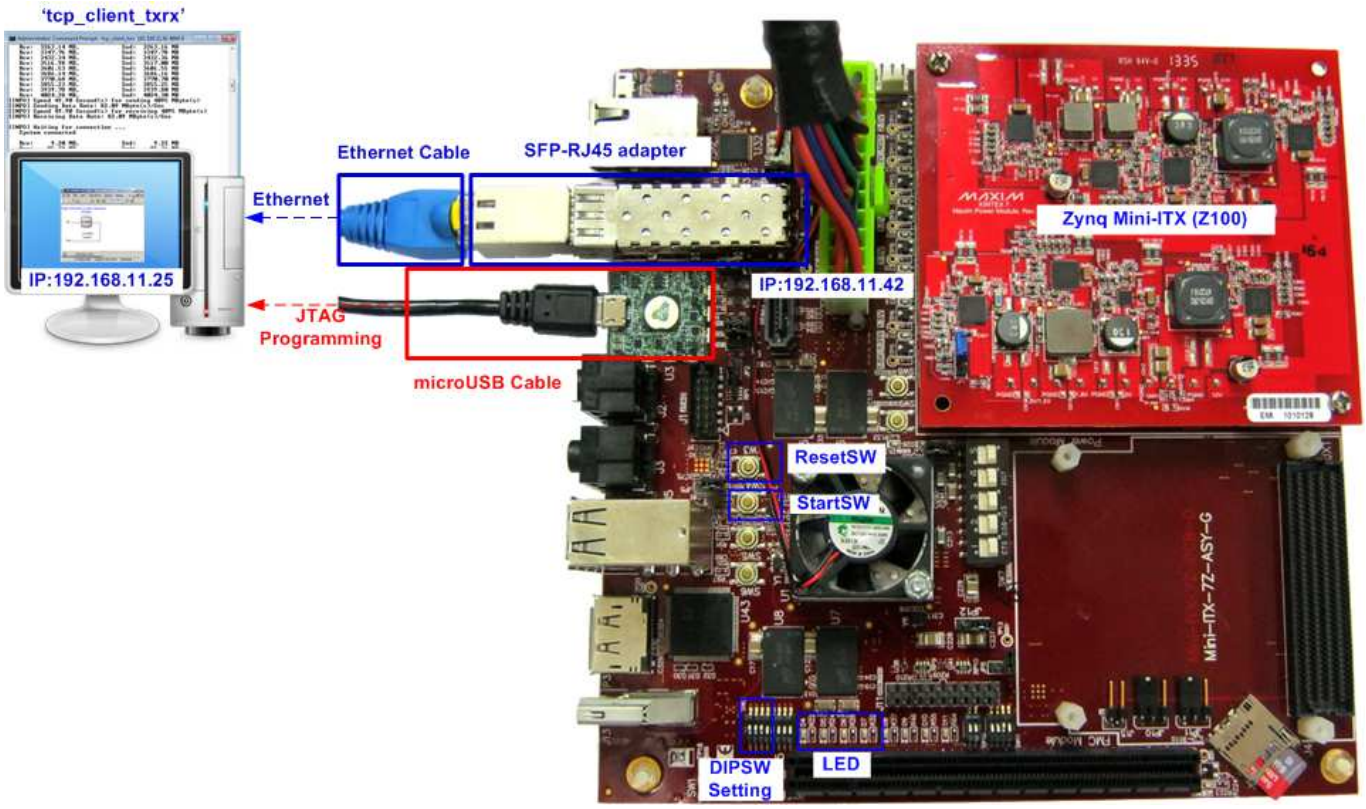

Figure 1-5 TOE1G-IP Full Duplex Demo Environment Setup on Zynq Mini-ITX (Z100)

Note: SFP-RJ45 adapter in the demo uses FCLF-8520-3/FCLF-8521-3.
https://www.finisar.com/sites/default/files/downloads/finisar_fclf-8520-3_fclf-8521-3_1000base-t_copper_sfp_optical_transceiver_productspecreve1.pdf

2 Demo description

The logic on FPGA is designed to connect data input and output of TOE1G-IP as loopback connection. So, total transmit data from test application on PC will be returned to PC for checking the data by test application. TCP connection is opened by PC, so PC runs on TCP Client mode while FPGA runs on TCP Server mode. The definition of LED on FPGA Development board is described in Table 2-1.

LED	ON/BLINK	OFF
0/D4	ON: IP initialize complete	Not complete. Please check that StartSW (Center-SW) has already been pressed and confirm IP address setting on PC that is correct.
1/R/D5	BLINK: Operation timeout or cable lost	Normal operation
2/C/D6	N/A	N/A
3/L/D7	ON: Port is established	No operation

Table 2-1 LED Definition

3 PC Setup

Please follow the same setting as described in “dg_toe1gip_instruction_xilinx_en” document http://www.dgway.com/products/IP/TOE1G-IP/dg_toe1gip_instruction_xilinx_en.pdf

4 How to run demo

4.1 FPGA Programming

To run the demo, please follow the step described in “dg_toe1gip_instruction_xilinx_en” document.
http://www.dgway.com/products/IP/TOE1G-IP/dg_toe1gip_instruction_xilinx_en.pdf

But, bit file of this module is “toefulltest.bit” to FPGA Development board, as shown in Figure 4-1. LED status after configuration complete is shown in Figure 4-2.

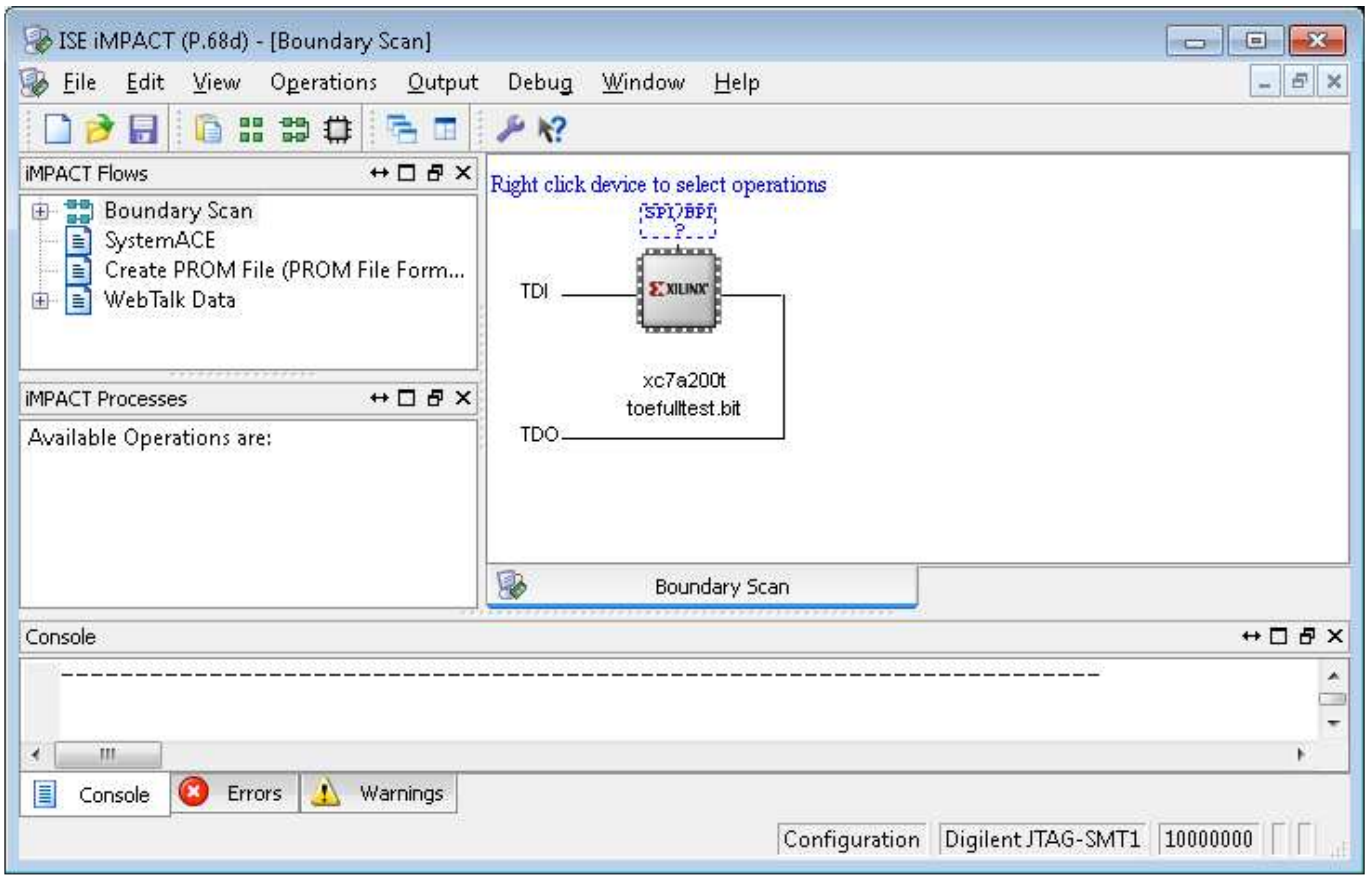

Figure 4-1 Programmer Environment

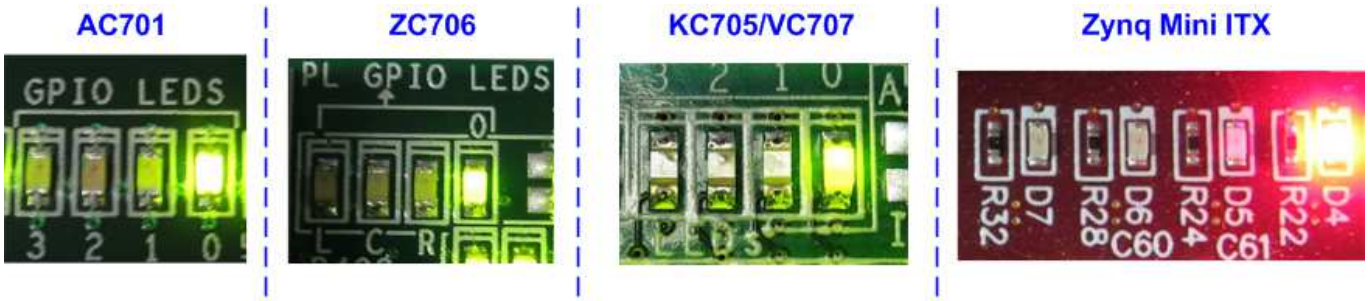

Figure 4-2 LED Status after press StartSW

Note: Transfer performance on the demo depends on Test PC performance to send and receive data through Gigabit Ethernet

4.2 Run Test Application

Test application will operate to send and receive 4 GB data at the same time. When all 4 GB are transferred for both directions, port connection will be closed by FPGA. Test application is designed to operate in loop, so new connection will be created by Test application to rerun the test. User needs to cancel the application to stop the test.

There are two operation modes for running the demo, i.e. Performance test mode, and Verification mode. The details of each mode are follows.

4.2.1 Performance Test mode

- Open “command prompt” on PC, and run “tcp_client_txrx” test application by following command
  >> tcp_client_txrx <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘0’-All ‘0’ pattern are sent out and no data verification

  For example,
  >> tcp_client_txrx 192.168.11.42 4000 0

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 4-3.
- User can cancel operation by pressing “Ctrl+C”.

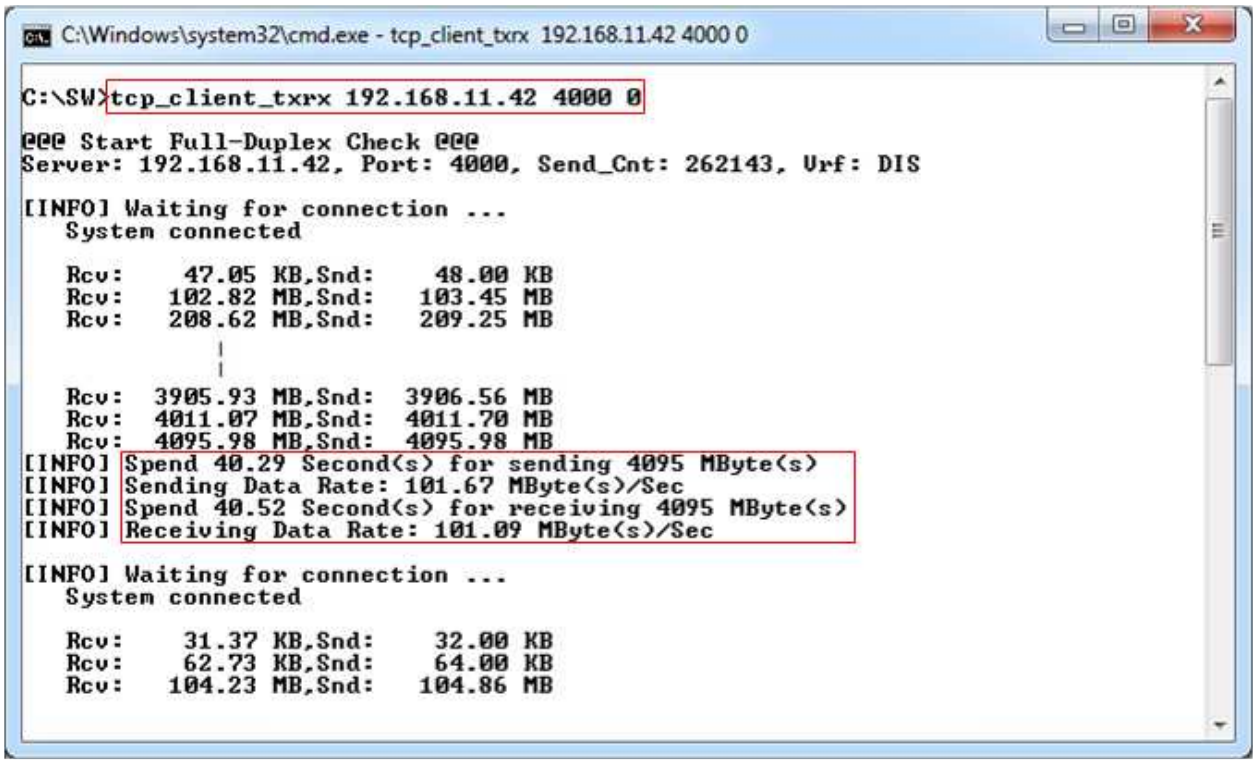

Figure 4-3 Test Result on Performance test mode

Figure 4-4 LED Status when running full duplex Demo in both modes

4.2.2 Verification mode

- Open “command prompt” on PC, and run “tcp_client_txrx” test application by following command
  >> tcp_client_txrx <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘1’-32-bit increment data are sent out and data verification is enabled.

  For example,
  >> tcp_client_txrx 192.168.11.42 4000 1

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 4-5.
- User can cancel operation by pressing “Ctrl+C”.

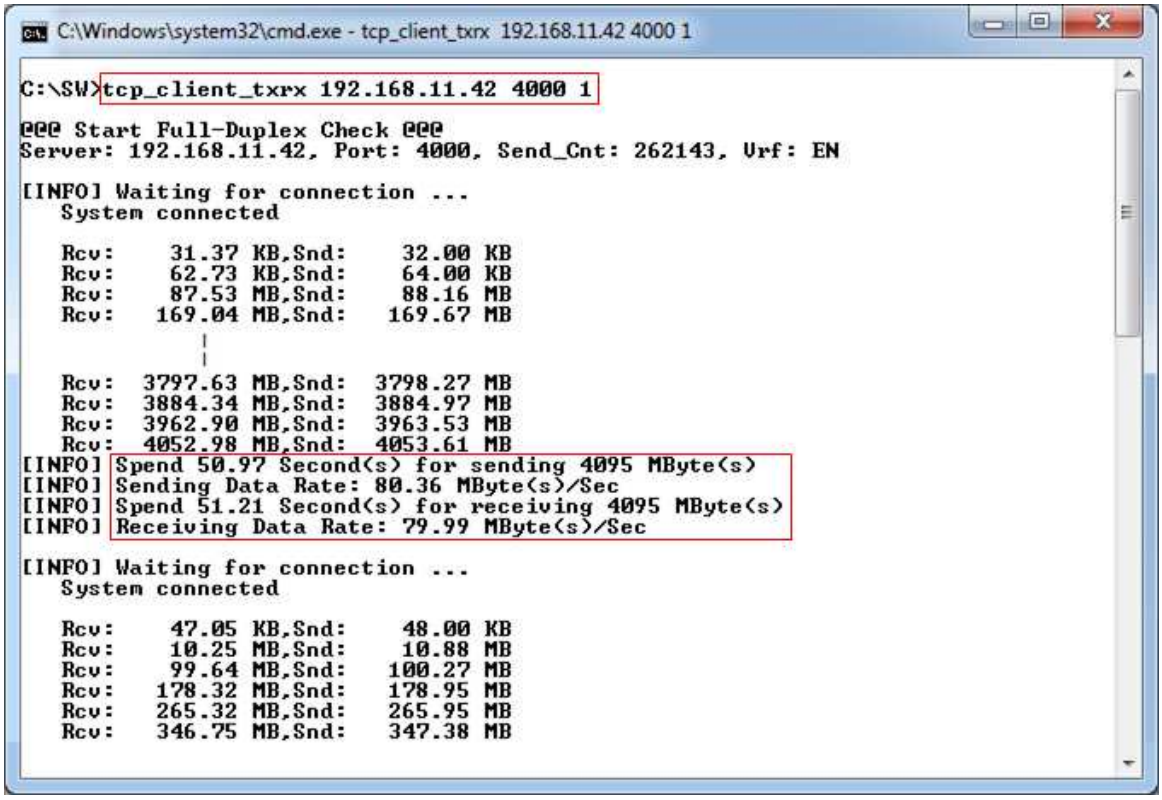

Figure 4-5 Test Result on Verification mode

5 Revision History

Revision	Date	Description
1.0	14-Aug-14	Initial version release
1.1	3-Dec-14	Update internet controller model
1.2	29-Dec-14	Add ZC706 support
1.3	2-Sep-16	IP core product renamed from TOE2-IP to TOE1G-IP
1.4	15-Nov-16	Add Zynq Mini-ITX support