TOE1G-IP Demo Instruction

Rev1.6 15-Nov-16

This document describes the instruction to run TOE1G-IP for transferring data between FPGA development board and PC through Gigabit Ethernet. This demo can select to run with supported and not supported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1-1 – Figure 1-5, to run TOE1G-IP standard demo, please prepare

1) FPGA Development board: AC701/KC705/VC707/ZC706/Zynq Mini-ITX(Z100 model)
2) Xilinx programmer software (iMPACT/Vivado)
3) For ZC706/Zynq Mini-ITX board: SFP-RJ45 adapter
4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
5) PC with Gigabit Ethernet support
6) micro USB cable for programming FPGA between FPGA Development board and PC
7) “send_tcp_client.exe” and “recv_tcp_client.exe”, provided by Design Gateway, which are test application available on PC

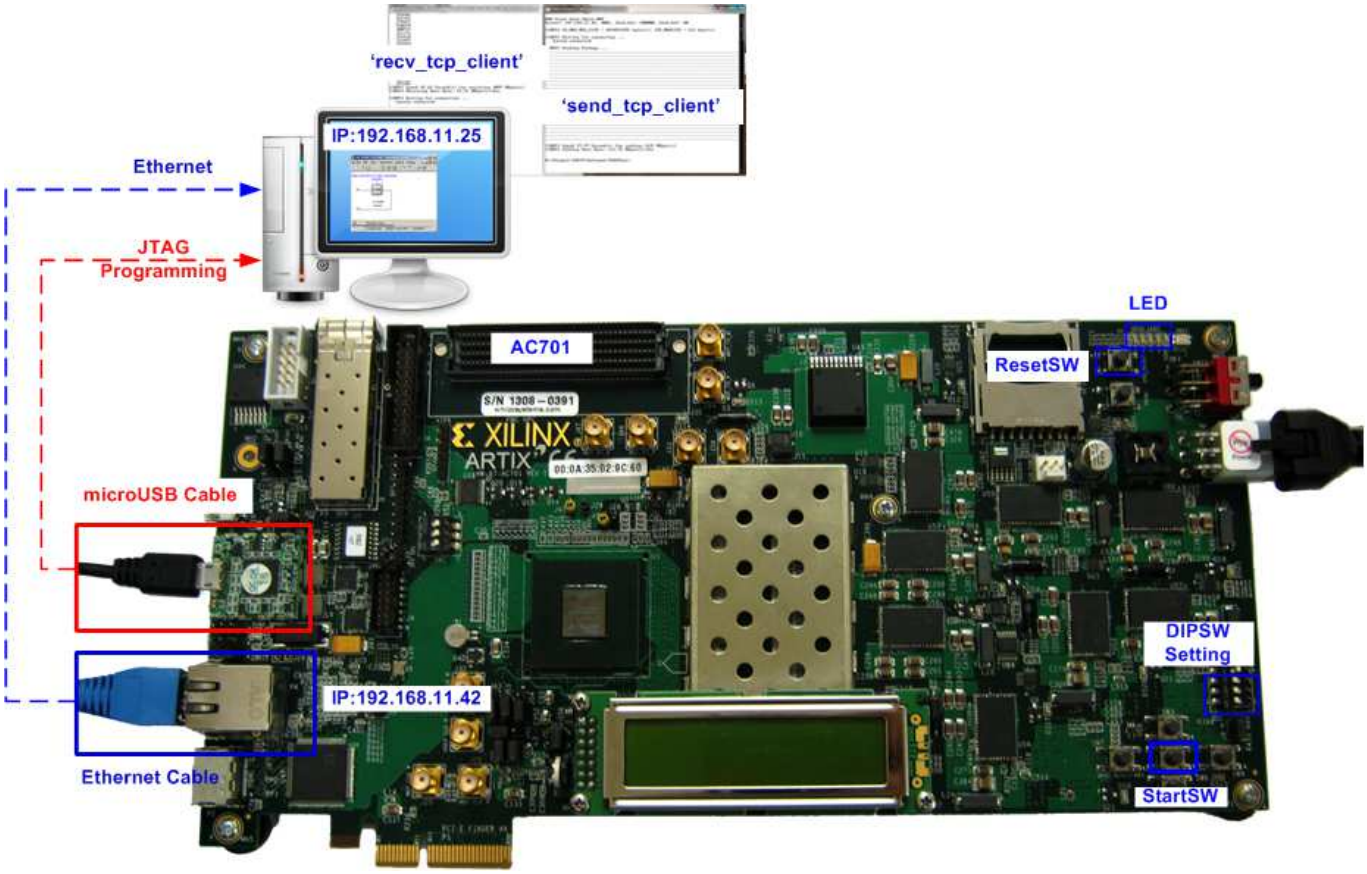

Figure 1-1 TOE1G-IP Demo Environment Setup on AC701

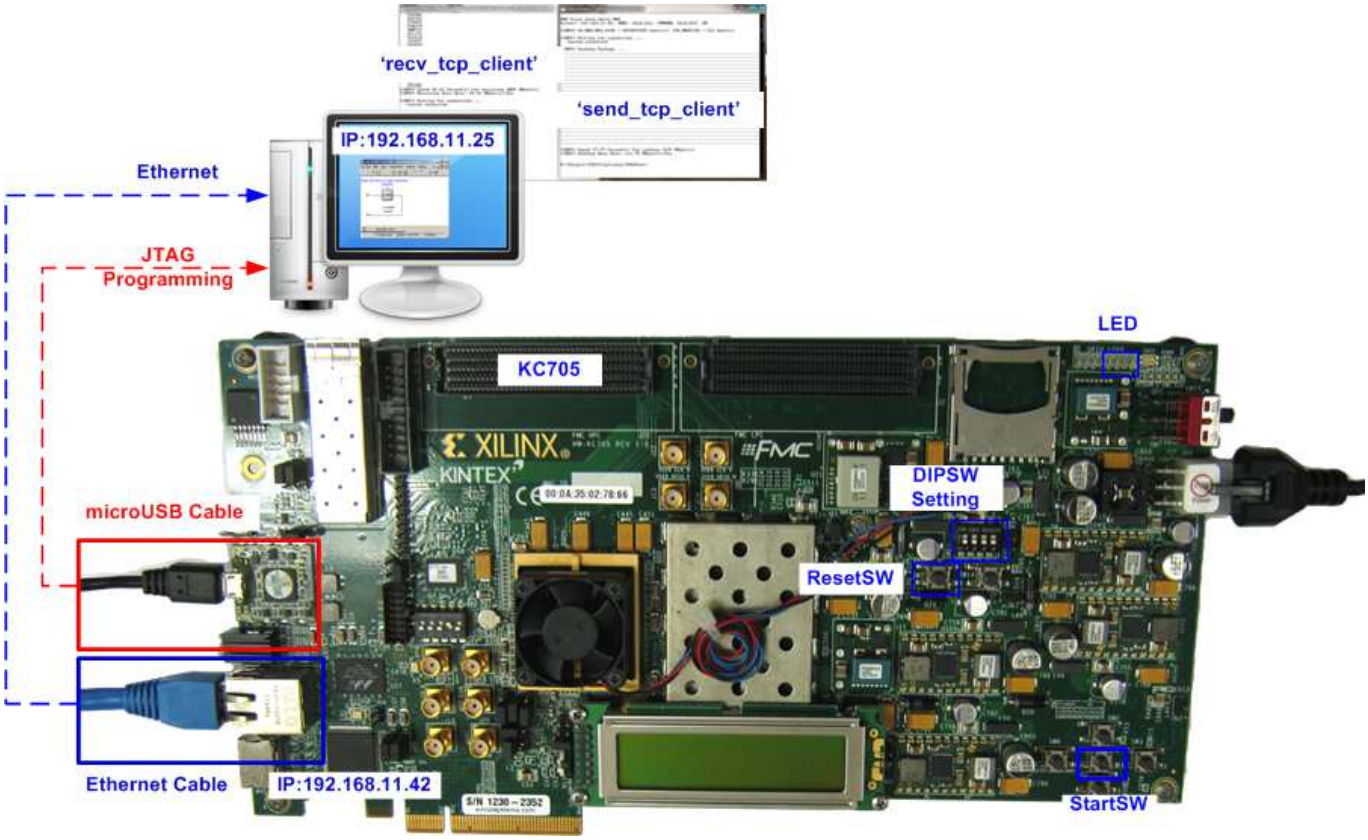

Figure 1-2 TOE1G-IP Demo Environment Setup on KC705

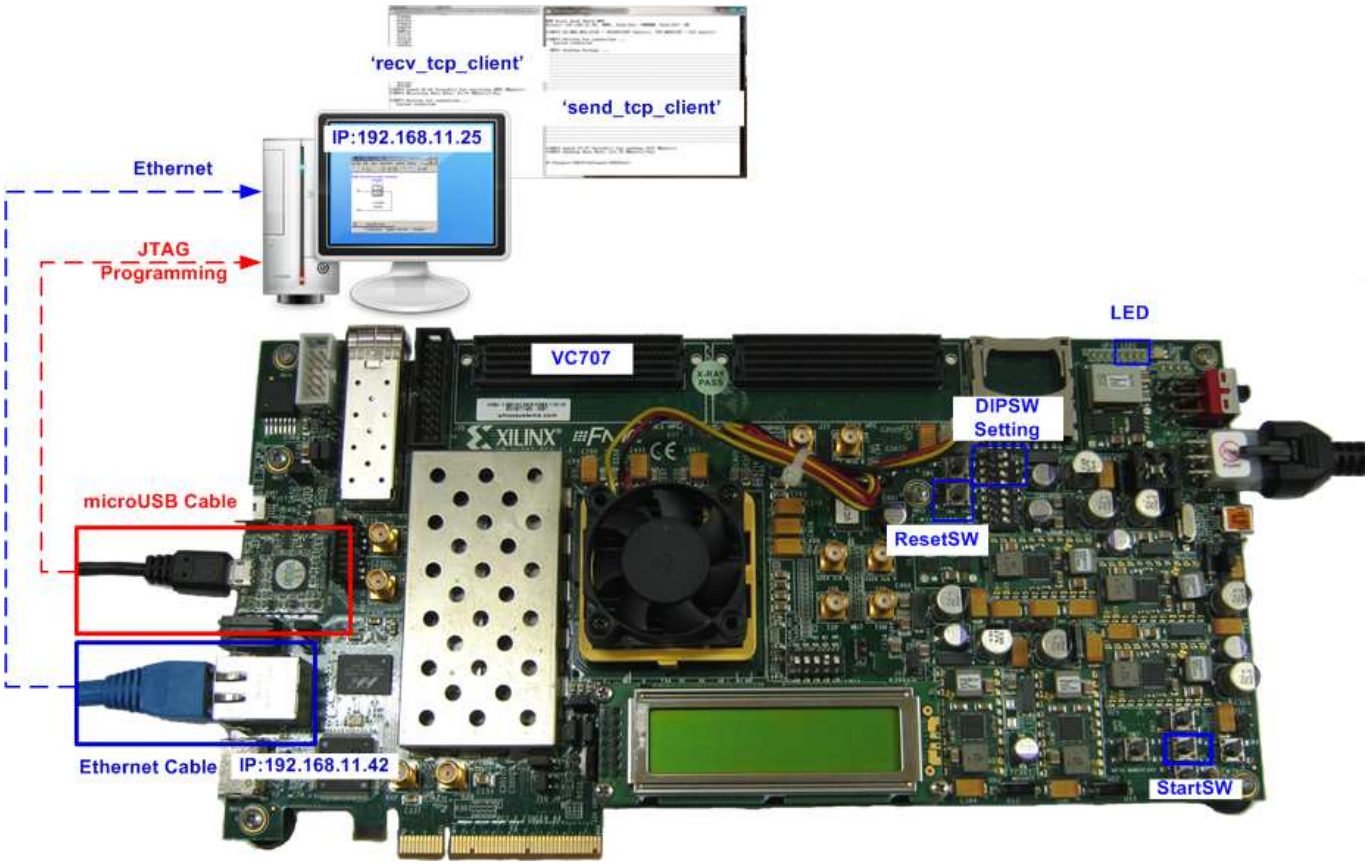

Figure 1-3 TOE1G-IP Demo Environment Setup on VC707

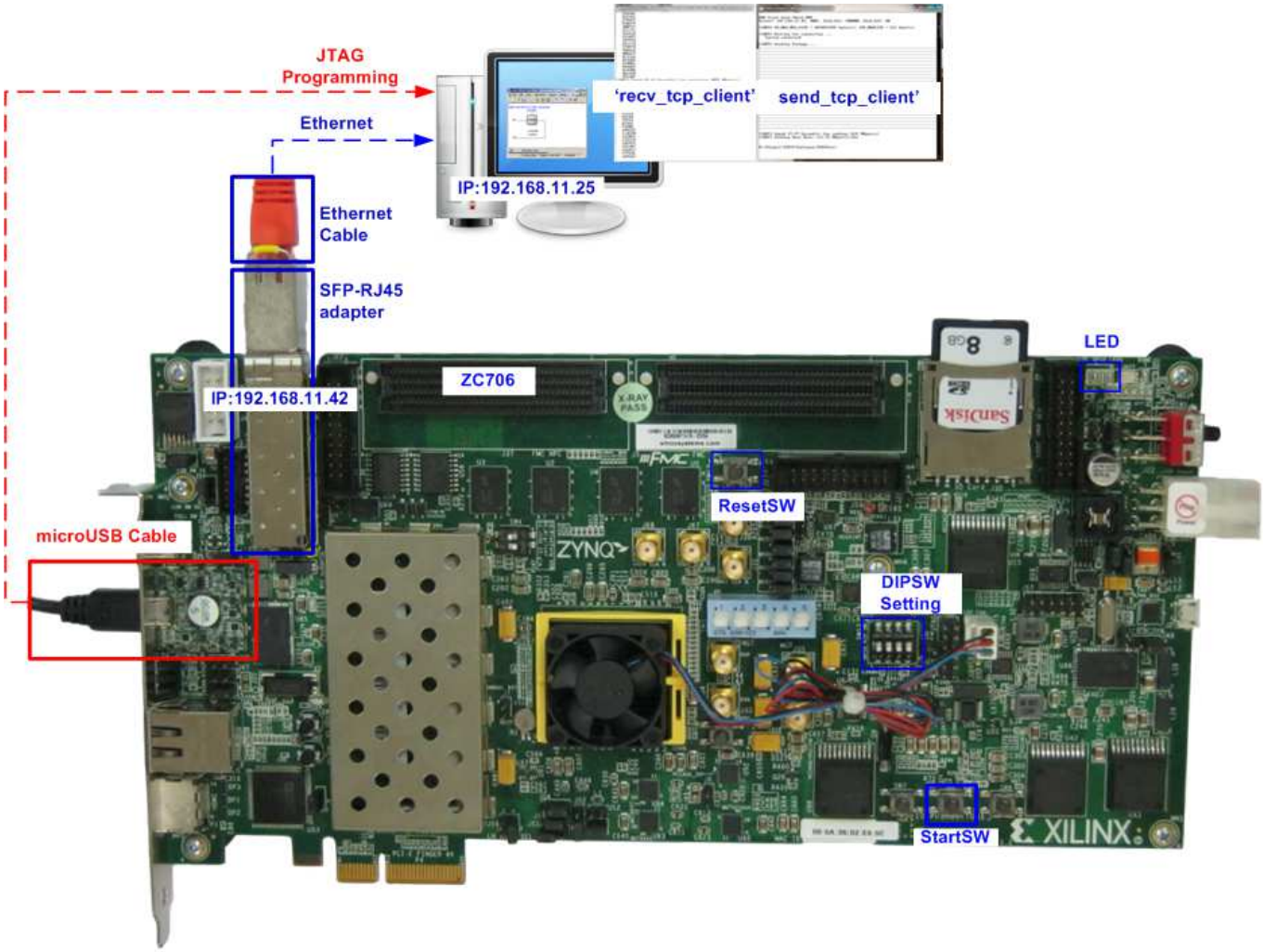

Figure 1-4 TOE1G-IP Demo Environment Setup on ZC706

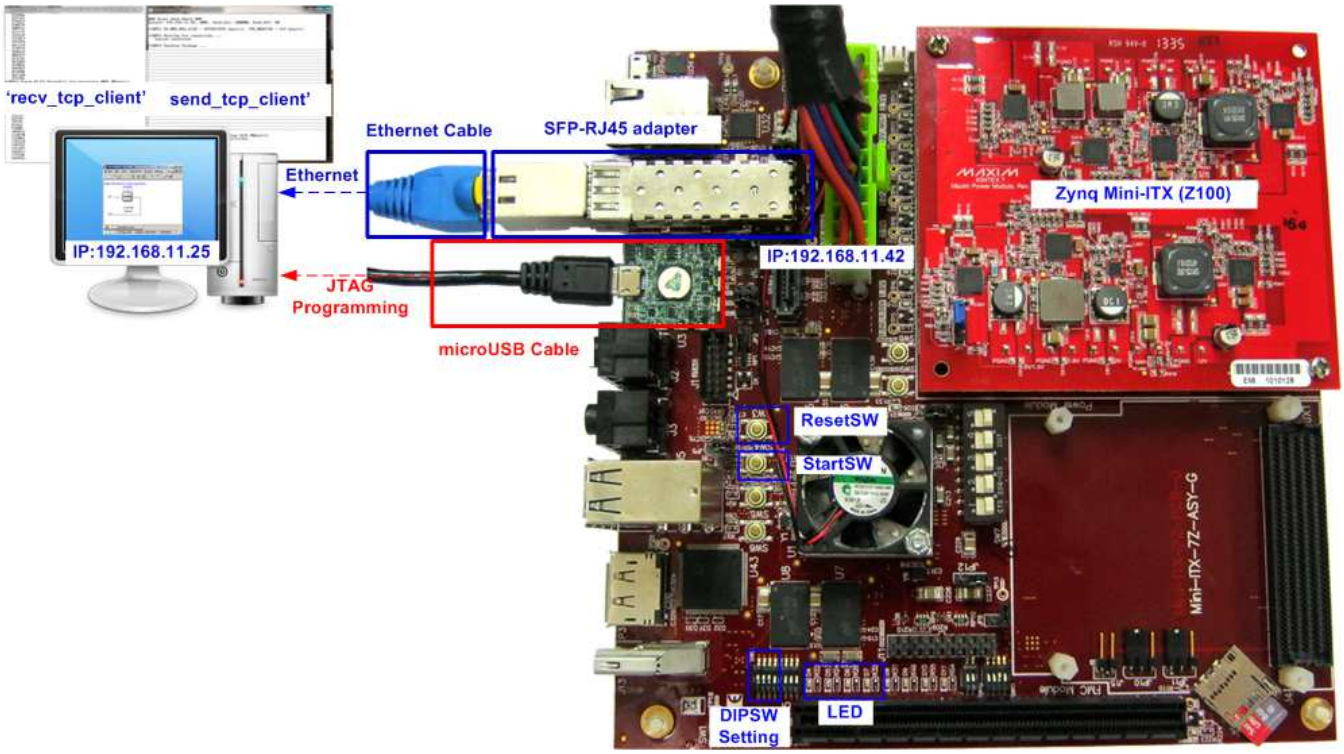

Figure 1-5 TOE1G-IP Demo Environment Setup on Zynq Mini-ITX (Z100 model)

Note: SFP-RJ45 adapter in the demo uses FCLF-8520-3/FCLF-8521-3.
https://www.finisar.com/sites/default/files/downloads/finisar_fclf-8520-3_fclf-8521-3_1000base-t_copper_sfp_optical_transceiver_productspecreve1.pdf

2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board (Server mode) and PC (Client mode). Each test mode requires different test application on PC and different DIPSW setting on FPGA development board. The definition of DIPSW and LED on FPGA development board are described in Table 2-1 and Table 2-2.

Note: DIPSW setting must not change during operation.

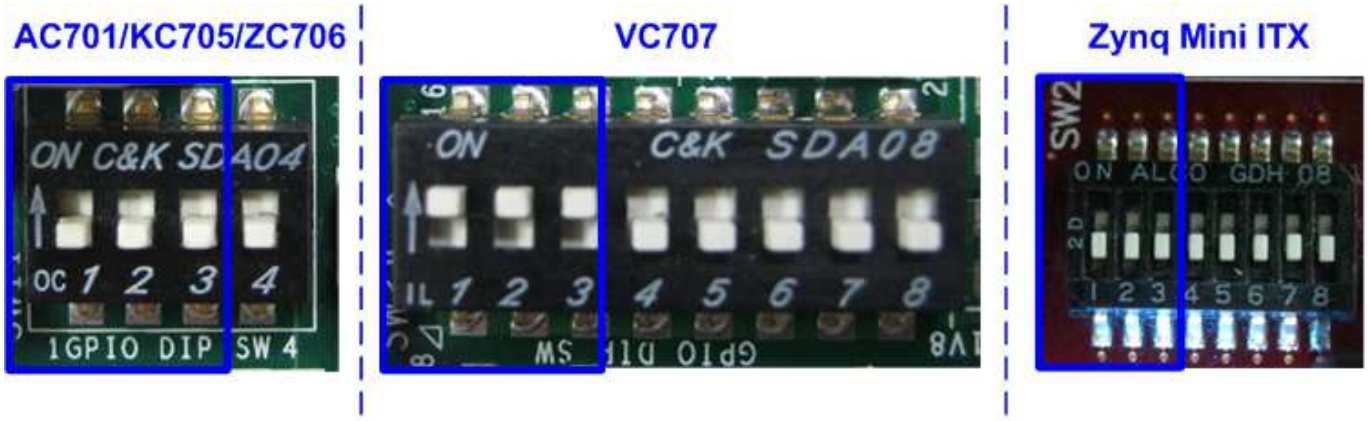

Figure 2-1 DIPSW Bit1-3 for user input

DIPSW	OFF	ON
Bit 1	Sending mode by using non-Jumbo frame (1460 bytes)	Sending mode by using Jumbo frame (8960 bytes)
Bit 2	Sending mode	Receiving mode
Bit 3	Receiving mode without data verification	Receiving mode with data verification

Table 2-1 DIPSW Setting Definition

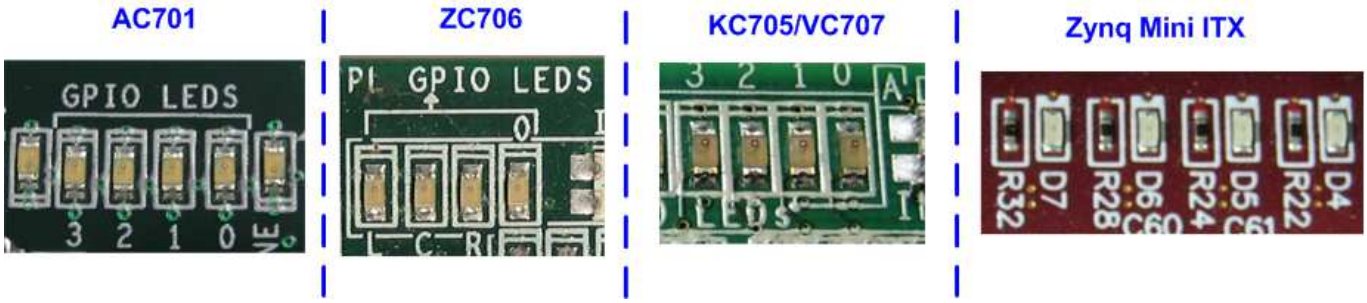

Figure 2-2 LED bit0-3 for user output

LED	ON/BLINK	OFF
0/D4	ON: IP initialize complete	Not complete. Please check that StartSW (Center-SW) has already been pressed and confirm IP address setting on PC that is correct.
1/R/D5	BLINK: Operation timeout or cable lost	Normal operation
2/C/D6	Sending mode in Jumbo frame.	Sending mode in non-jumbo frame
3/L/D7	BLINK: data verification is fail in receiving mode ON: Port is established.	No operation

Table 2-2 LED Definition

The step to run sending and receiving test are described as follows.

2.1 Sending mode

In this mode, 4 GB data will be transferred from FPGA development board to PC, and "recv_tcp_client.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select two transfer packet sizes by DIPSW[1] setting, i.e. 1460 data byte for running with not supported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting from LED2/C/D6 status.

The operation sequence for sending mode is follows.

1) TOE1G-IP within FPGA development board initializes system parameters such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
2) Test application on PC opens connection to connect with FPGA development board, and waits data sending from FPGA.
3) TOE1G-IP starts to send 4 GB data to PC while PC verifies receiving data that is correct.
4) After all data are transferred, TOE1G-IP sends packet to close connection.
5) PC sends acknowledge to close connection. Then, operation will run as loop from Step2) to Step5) until operation cancelled.

2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By using "send_tcp_client.exe" operating on PC, data will be sent out until total number of transferred data equal to setting value. This test can run as two modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC and verification module within FPGA development board will be OFF for achieving best performance transfer. In data verification mode, 32-bit increment data will be generated from PC and verification module will be ON for data verification. LED3/L/D7 will blink if error data is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can be set as option value in command line.

The operation sequence for receiving mode is follows.

1) Similar to Step 1) in Sending mode.
2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
3) TOE1G-IP receives data and verifies data if enable.
4) After all data are transferred, Test application sends packet to close connection.
5) TOE1G-IP sends acknowledgment to close connection. This mode will run only one time, not in repeat loop like Sending mode.

3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

3.1 IP Setting

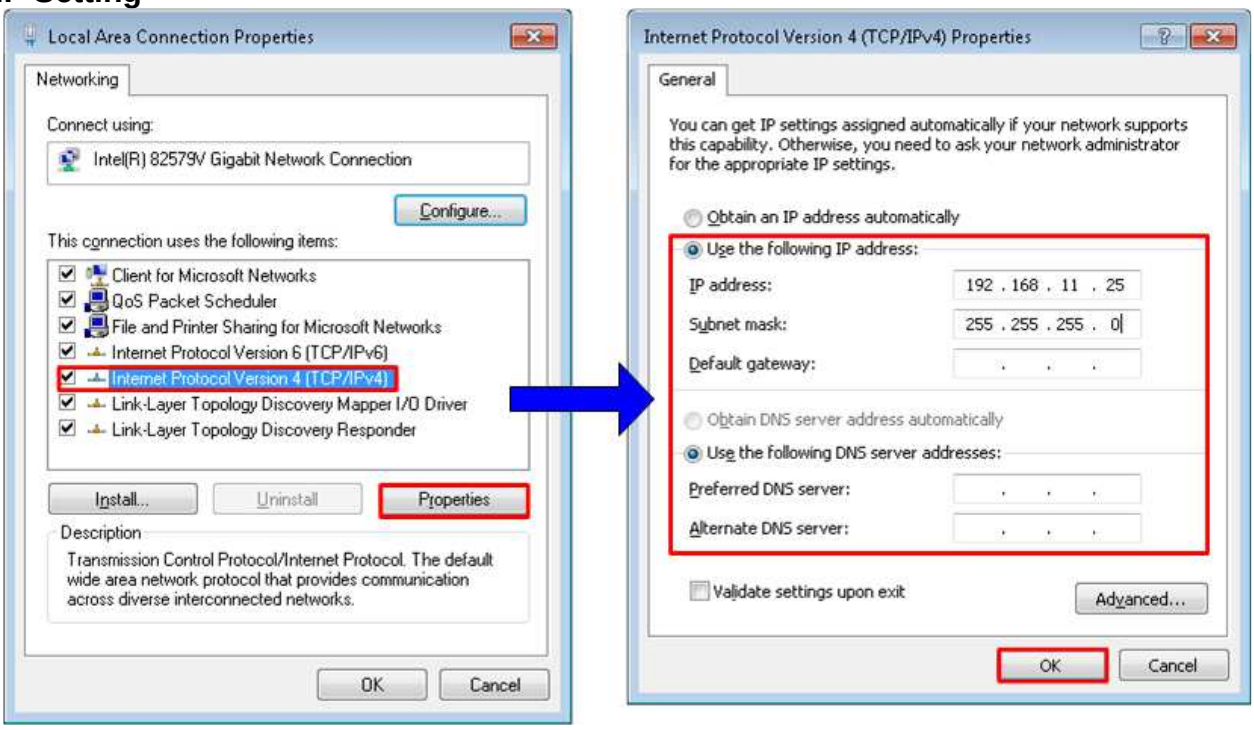

Figure 3-1 IPv4 Setting

- Open Local Area Connection Properties of test connection, as shown in left window of Figure 3-1.
- Select “TCP/Ipv4” and then click Properties.
- Set IP address = 192.168.11.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 3-1.

3.2 Speed and Frame Setting

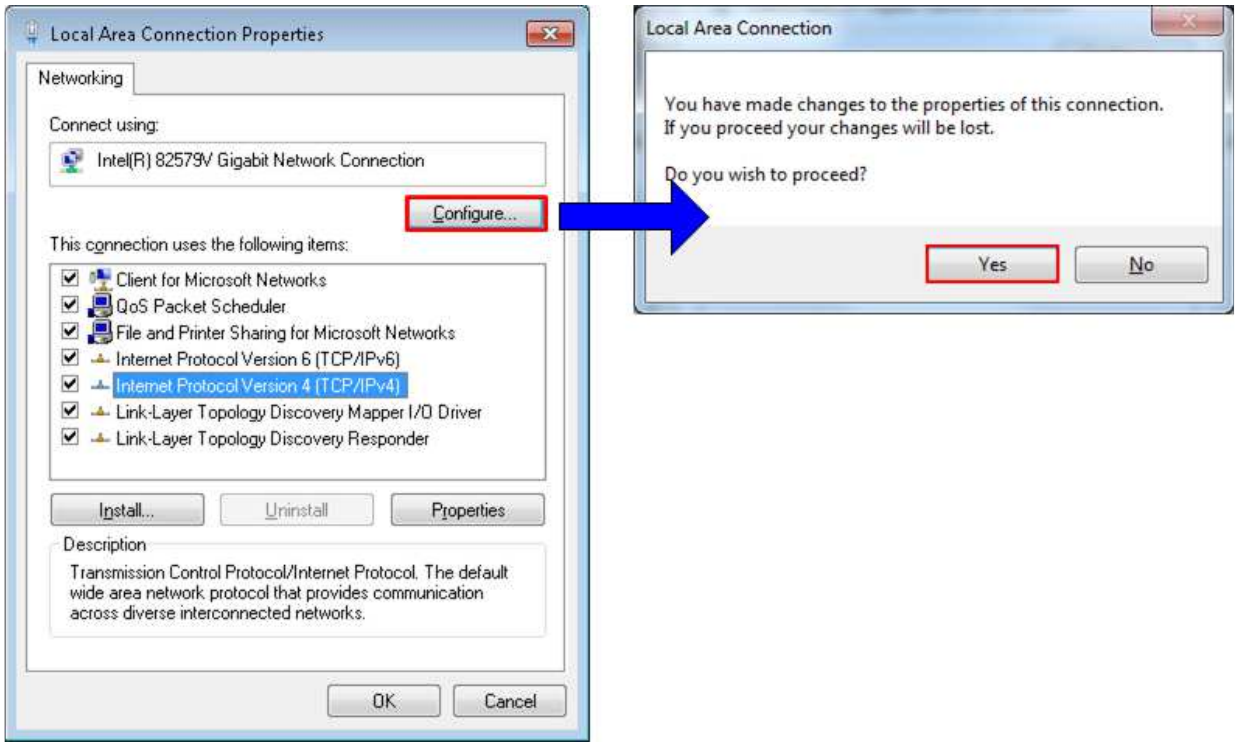

Figure 3-2 Network Configure

- On Local Area Connection Properties window, click “Configure”, as shown in Figure 3-2.
- On Advance tab, Jumbo Packet = 9014 Bytes to enable jumbo frame, as shown in Figure 3-3.

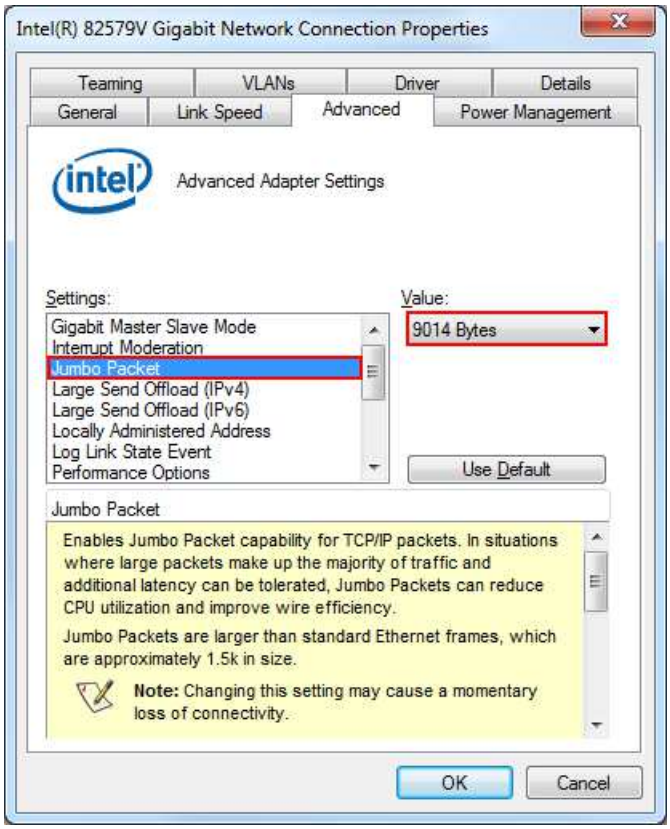

Figure 3-3 Jumbo Frame Setting

- On Link Speed tab, select “1.0 Gbps Full Duplex” for running Gigabit transfer test, as shown in left window of Figure 3-4.
- On Advance tab, Settings=Interrupt Moderation and Value= “Enabled”, as shown in right window of Figure 3-4.

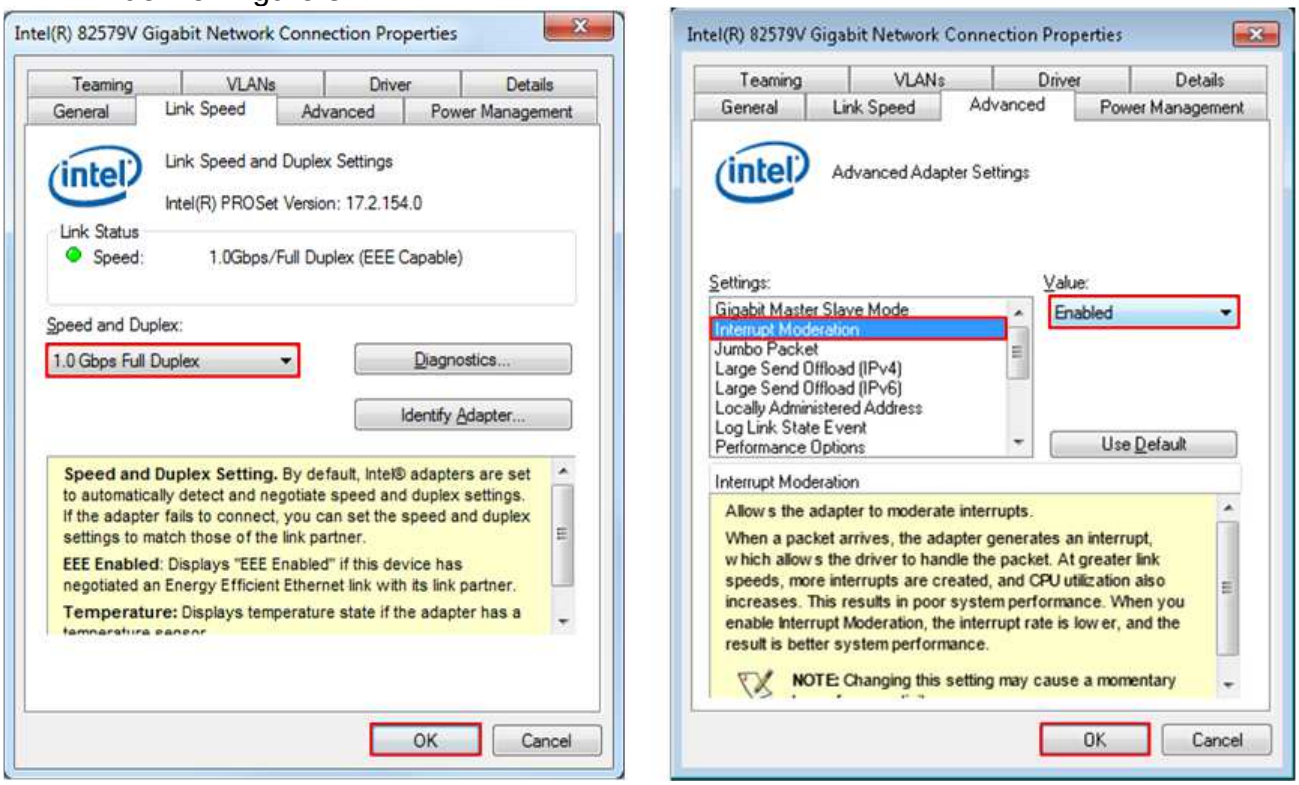

Figure 3-4 Link speed and Jumbo frame setup

- For Intel LAN controller, Performance Options in “Advanced” tab should be set for better performance as shown in Figure 3-5. “Interrupt Moderation Rate” in “Performance Options” windows must be set to “Off”.

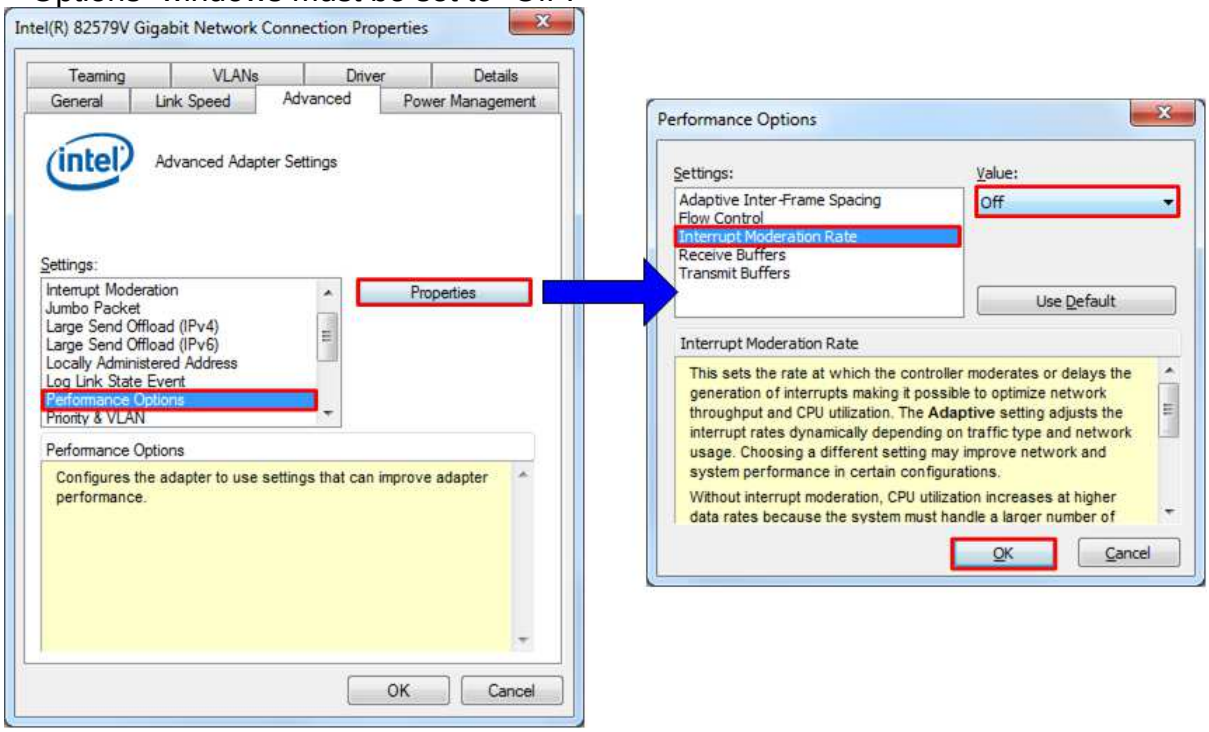

Figure 3-5 Enable Interrupt Moderation

4 How to run demo

Both Sending and Receiving demo requires same initial steps to set up hardware as follows.

1) Power off system
2) Set up board option
   a) For ZC706 board only,
      i. Set SW11=”00000” to configure PS from JTAG, as shown in Figure 4-1.
      ii. Set SW4=”01” to connect JTAG with USB-to-JTAG interface, as shown in Figure 4-2.

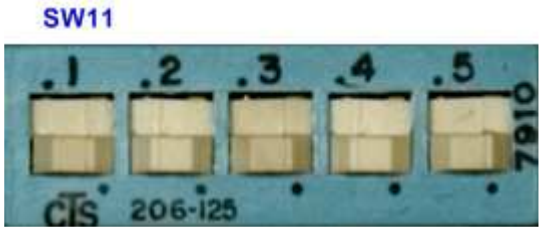

Figure 4-1 SW11 setting to configure PS from JTAG on ZC706 board

Figure 4-2 SW4 setting to use USB-to-JTAG on ZC706 board

   b) For Zynq Mini-ITX board only,
      i. Set SW7="00000" to configure PS from JTAG, as shown in Figure 4-3.
      ii. As shown in Figure 4-4, install a jumper on JP1 pins 1-2 to enable JTAG chain, install the power module onto the board via J8, J9, J10 connectors, and connect ATX power cable to FPGA board via P2 connector.

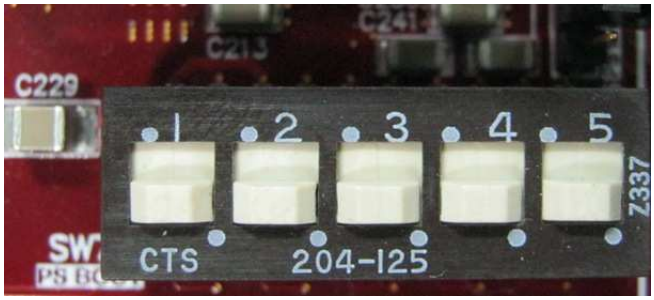

Figure 4-3 SW7 setting to configure PS from JTAG on Zynq Mini-ITX

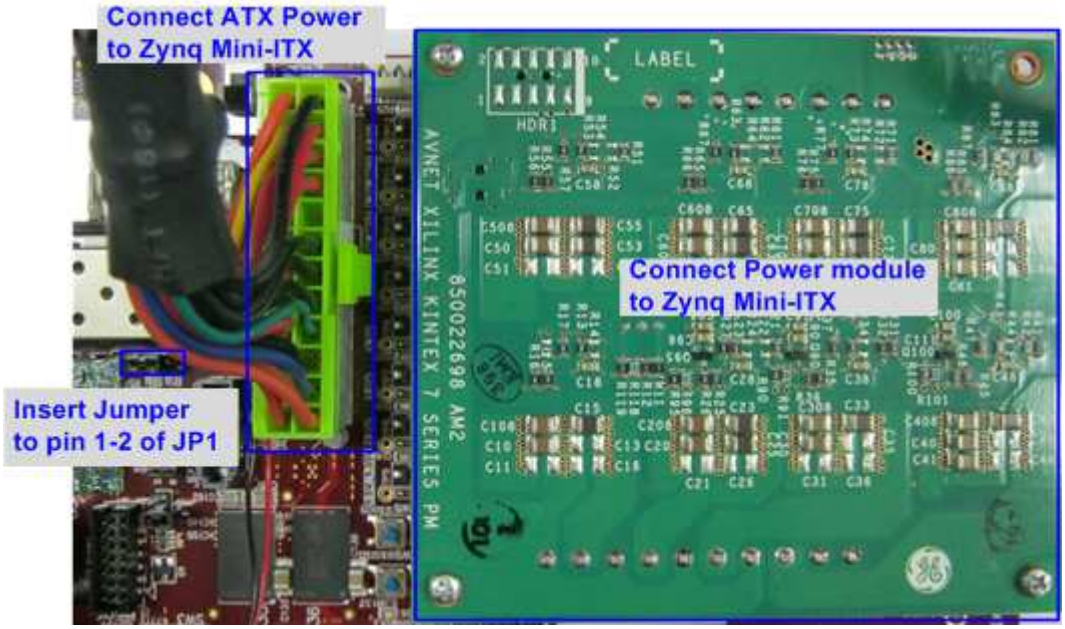

Figure 4-4 The power module installed onto the board

3) Connect micro USB cable from FPGA development board to PC and connect power supply to FPGA board.
4) Connect Ethernet cable between FPGA development board and PC.
5) Set up network setting on PC, following Topic 3.
6) Power on FPGA development board.
7) Open Xilinx programmer (iMPACT or Vivado) and download bilt file to FPGA development board, as shown in Figure 4-5.

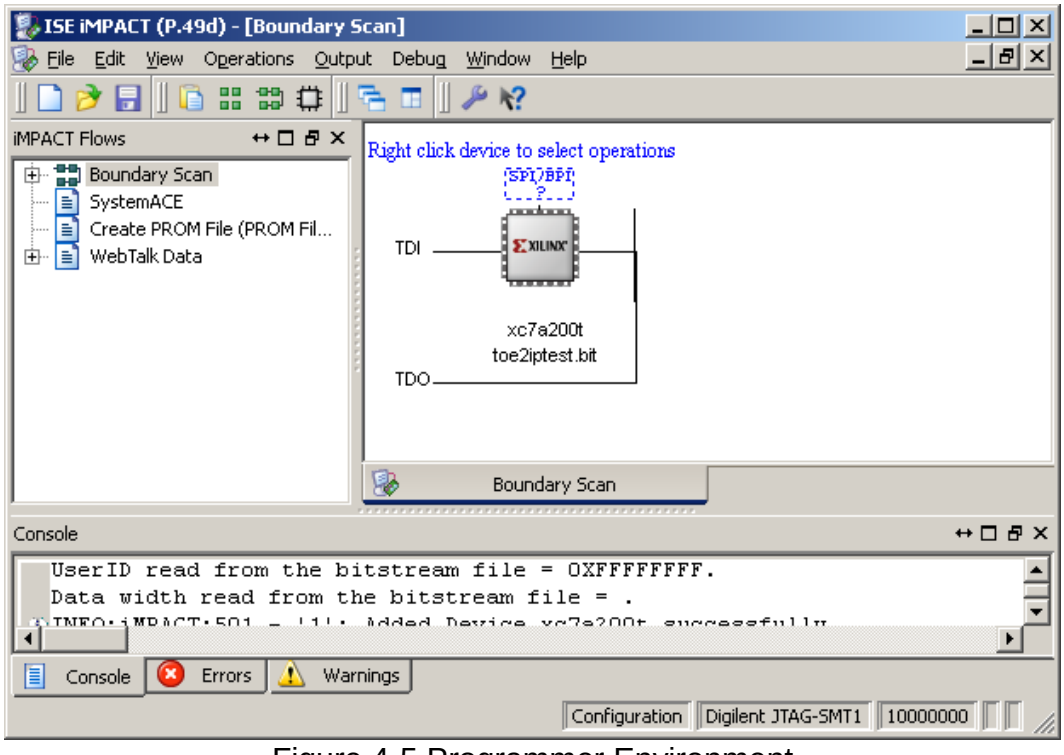

Figure 4-5 Programmer Environment

8) Check LED status on FPGA development board now and LED0/1/3 are all turn off.
9) Check link status of PHY chip for some boards.
   a) For AC701 board, check link status LED of PHY chip at DS11. LED must be OFF to show that Ethernet link is ready, as shown in Figure 4-6.
   b) For KC705/VC707 board, check 1000 link status LED at DS11 (near RJ45). LED must be ON to show that Ethernet link is ready, as shown in Figure 4-6.

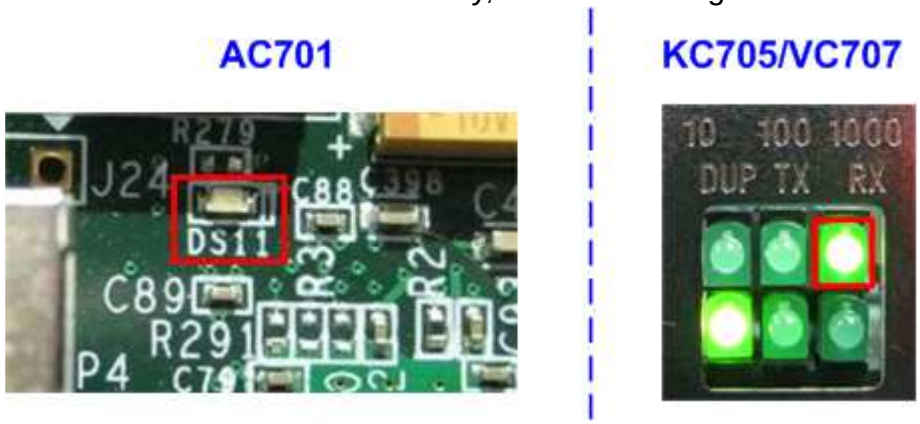

Figure 4-6 Link Status LED from PHY chip

10) Press StartSW at Center-SW for Xilinx board or SW4 for Zynq Mini-ITX to initialize system parameter

Figure 4-7 StartSW position on each board

11) LED0/D4 will turn on while LED2/C/D6 status will depend on DIPSW[1] setting.

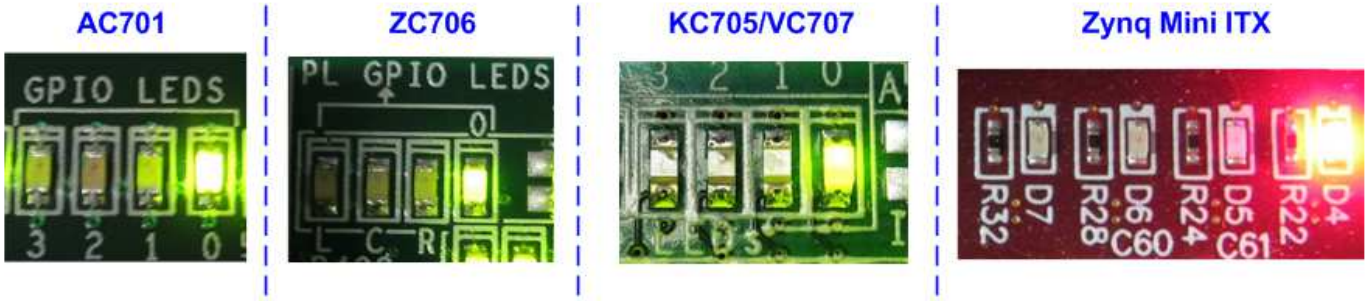

Figure 4-8 LED Status after press StartSW when DIPSW[1]=OFF

Figure 4-9 LED Status after press StartSW when DIPSW[1]=ON

Now system is ready to transfer data. The step to test Sending and Receiving data is described in next topic.

Note: Transfer performance on the demo depends on Test PC performance to send and receive data through Gigabit Ethernet

4.1 Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test.

4.1.1 Non-Jumbo frame mode

- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = OFF and confirm that LED2/C/D6 status is OFF.
- Open “command prompt” on PC, and run “recv_tcp_client” test application by following command
  >> recv_tcp_client <FPGA IP address> <FPGA port number> <number of data in packet>
  For example,
  >> recv_tcp_client 192.168.11.42 4000 1460
  Note: This demo fixes IP address, port number, and the number of data. So, please do not change any value without vhdl code modification.
- Test application displays received data size during transferring. After end each transfer loop, time usage and performance will be displayed, as shown in Figure 4-10.
- User can cancel operation by pressing “Ctrl+C”.

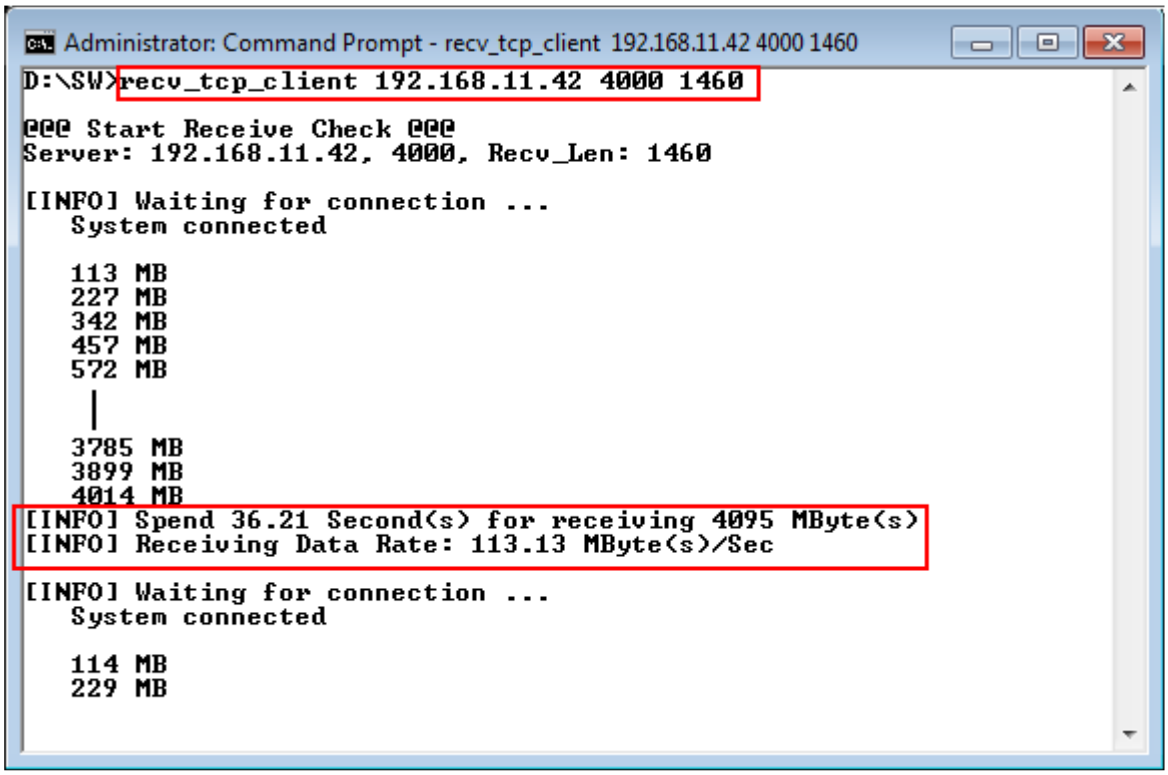

Figure 4-10 Non-Jumbo frame Sending Demo

Figure 4-11 LED Status when running Sending Demo with Non-Jumbo frame

4.1.2 Jumbo frame mode

- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = ON and confirm that LED2/C/D6 status is ON.
- Open “command prompt” on PC, and run “recv_tcp_client” test application by following command
  >> recv_tcp_client 192.168.11.42 4000 8960
  Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without hdl code modification.
- Message during test operation and how to cancel operation are similar to Non-Jumbo frame mode.

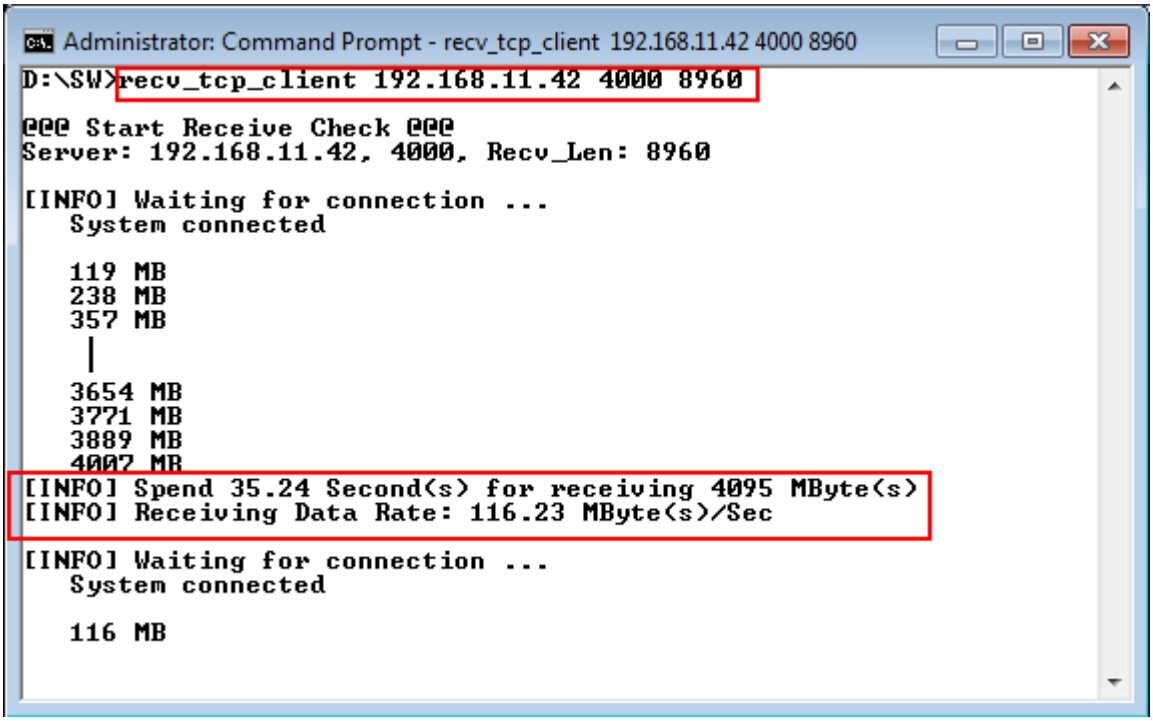

Figure 4-12 Jumbo frame Sending Demo

Figure 4-13 LED Status when running Sending Demo with Jumbo frame

4.2 Run Receiving Demo

4.2.1 Performance test mode

- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = OFF.
- Open “command prompt” on PC, and run “send_tcp_client” test application by following command
  >> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
  - User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 Mbyte data is transferred. Valid range of transfer size is 1 – 262143.
  - Mode: ‘0’- All ‘0’ pattern are sent for performance test.

  For example,
  >> send_tcp_client 192.168.11.42 4000 100000 0

- Test application displays “…” during transferring packet. Time usage with performance will be displayed when complete data transfer, as shown in Figure 4-15.

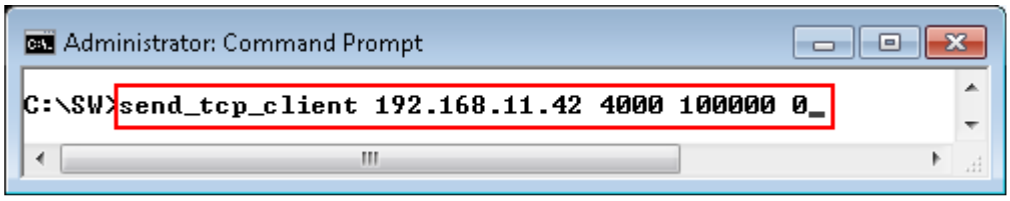

Figure 4-14 Command line for receiving demo on Performance test mode

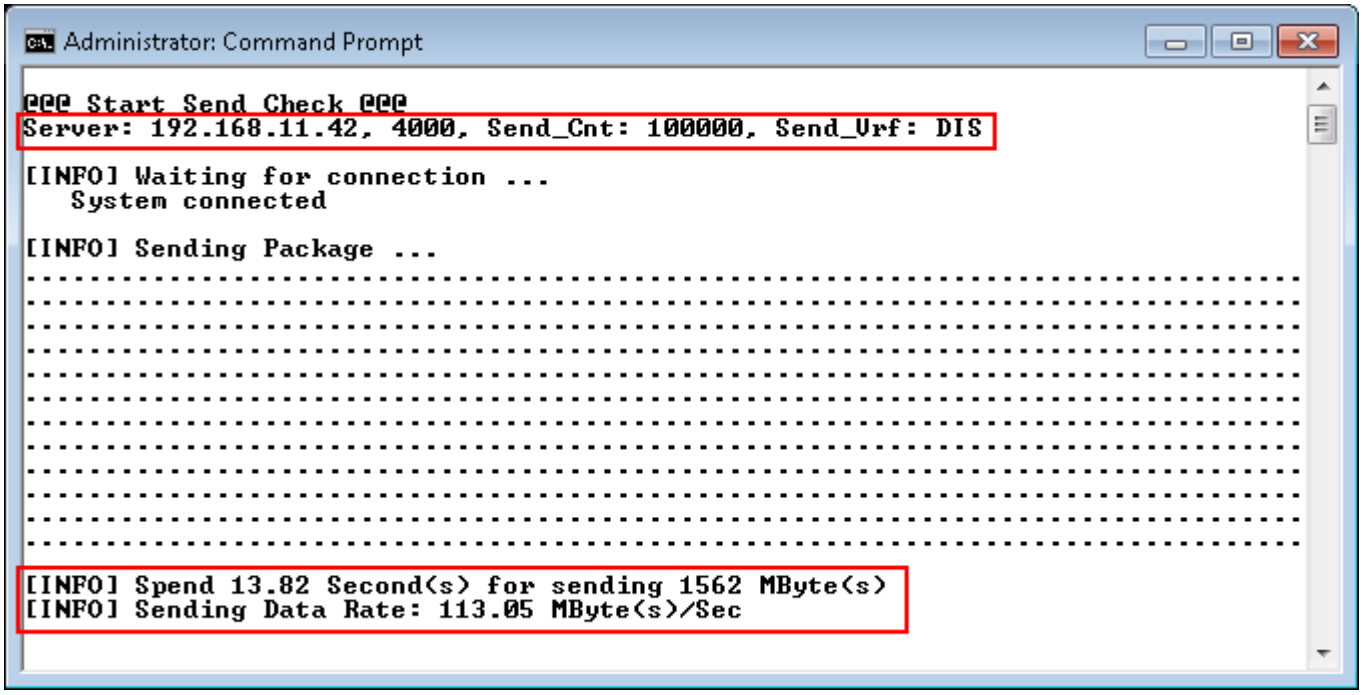

Figure 4-15 Receiving Demo on Performance test mode

4.2.2 Verification mode

- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = ON to enable verification module.
- Open “command prompt” on PC, and run “send_tcp_client” test application by following command
  >> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
  - User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 Mbyte data is transferred. Valid range of transfer size is 1 – 262143.
  - Mode: ‘1’- 32-bit increment data are sent for data verification.

  For example,
  >> send_tcp_client 192.168.11.42 4000 100000 1
- Test application displays “…” during transferring packet and time usage with performance will be displayed when complete data transfer, as shown in Figure 4-17.

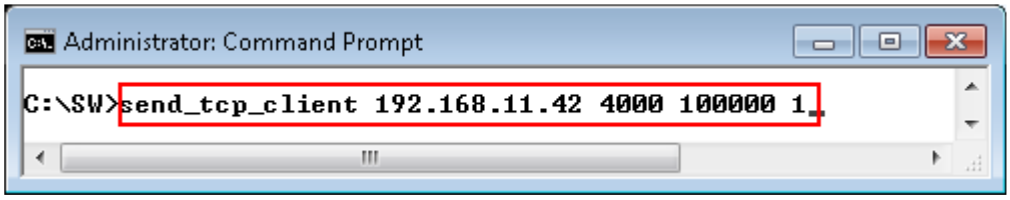

Figure 4-16 Command line for receiving demo on Verification mode

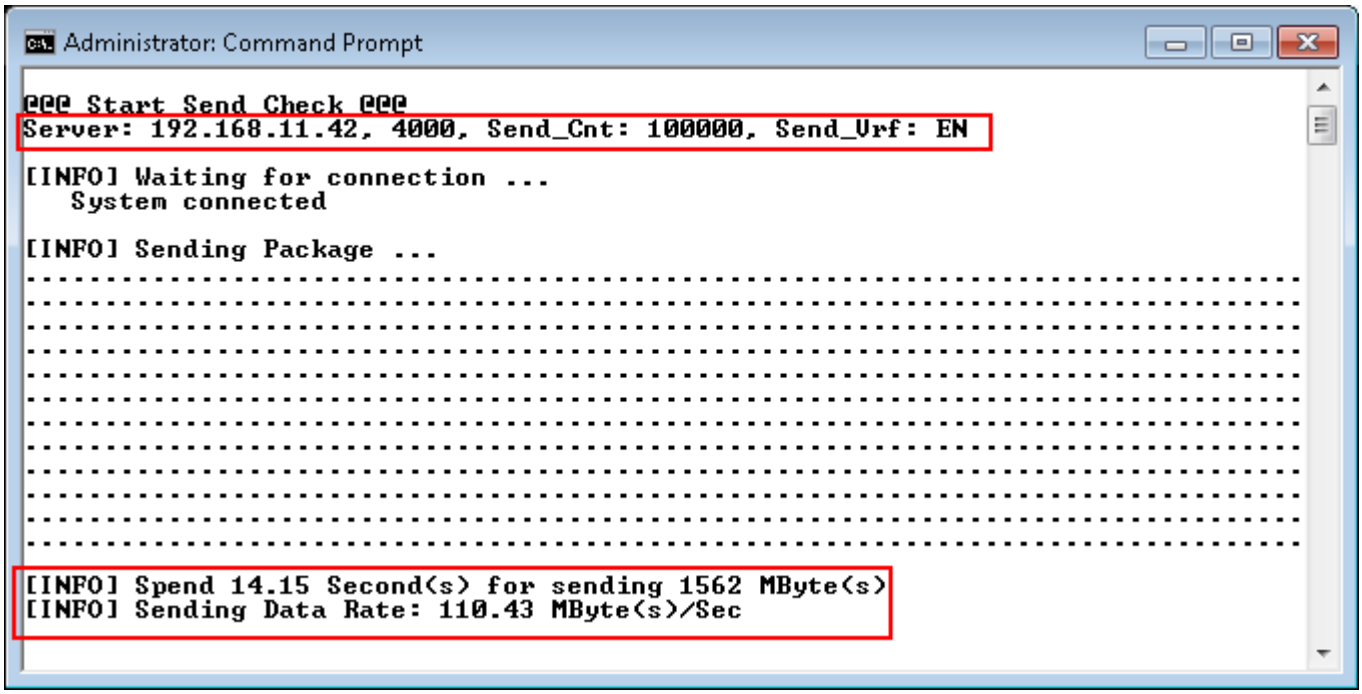

Figure 4-17 Receiving Demo on Verification mode

- LED3 will blink if any error data is detected from Verification module.

5 Revision History

Revision	Date	Description
1.0	13-Aug-14	Initial version release
1.1	3-Dec-14	Change Internet controller model
1.2	29-Dec-14	Add ZC706 support
1.3	12-Jan-15	Add DIPSW setting for JTAG programming on ZC706
1.4	29-Dec-15	Update Figure 16 and 18
1.5	2-Sep-16	IP core product renamed from TOE2-IP to TOE1G-IP
1.6	15-Nov-16	Add Zynq Mini-ITX support