



## FPGA setup for TOE200GADV-IP Demo

Rev1.00 13-Jun-24

1	Overview .....	2
2	Test environment setup when using FPGA and PC.....	3
3	Test environment setup when using two FPGAs .....	10
4	Revision History .....	14

# 1 Overview

This document provides a guide on setting up an FPGA board and preparing the necessary test environment to run the TOE200GADV-IP demo. The user has the option to create two test environments for transferring TCP payload data via a 200G Ethernet connection using TOE200GADV-IP. Figure 1-1 illustrates these two options.

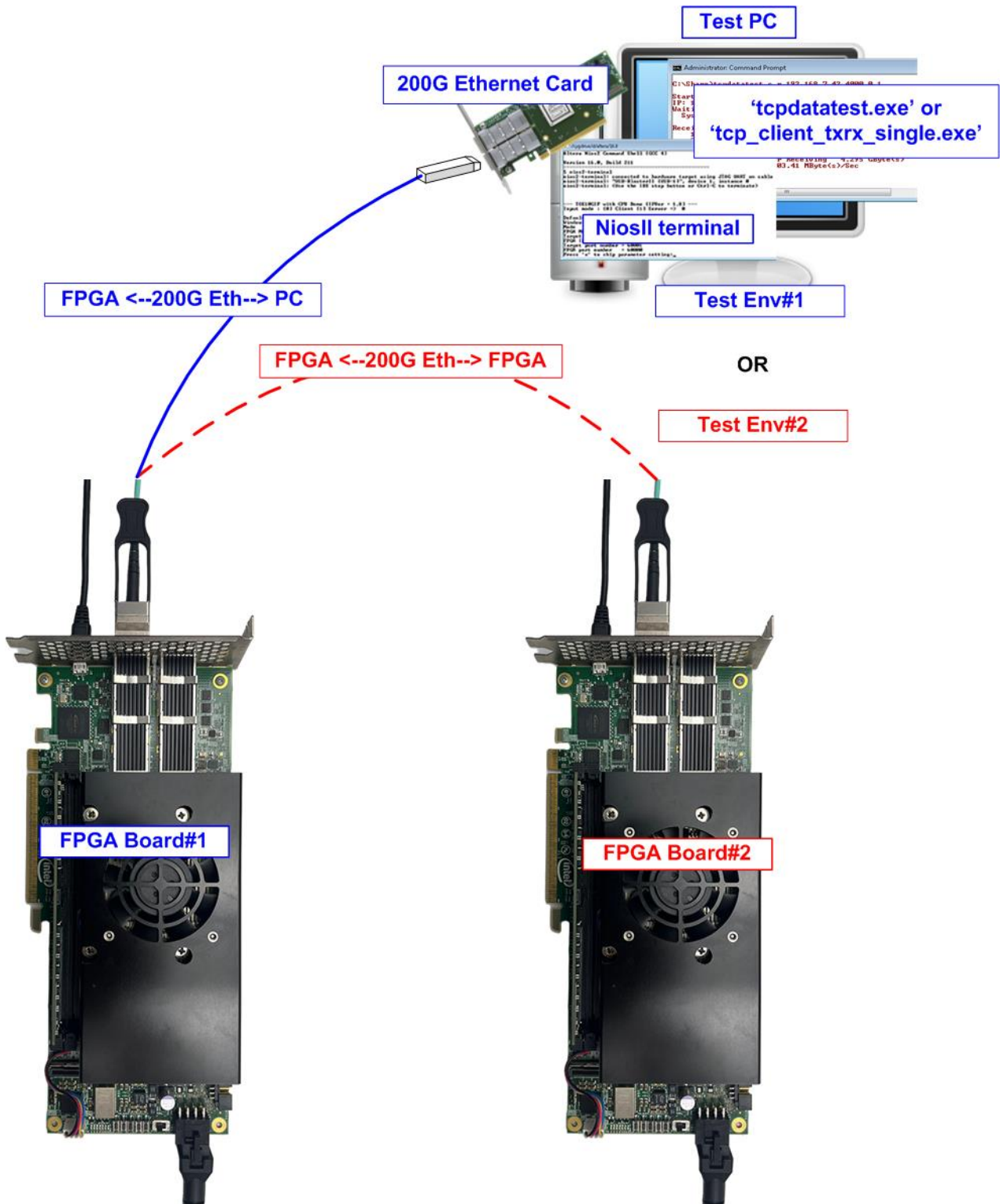


Figure 1-1 Two test environments for running the demo

The first test environment requires one FPGA board and a PC with a 200G Ethernet card for data transfer. The PC runs a test application, such as 'tcpdatatest' (half-duplex test) or 'tcp\_client\_txrx\_single' (full-duplex test). The NiosII Terminal is also run on the PC to act as the user interface console.

The second test environment involves two FPGA boards. Both boards run the TOE200GADV-IP with different initialization mode assigned (Client, Server, or Fixed-MAC).

## 2 Test environment setup when using FPGA and PC

Before running the demo using an FPGA and PC, please prepare the following.

- FPGA development boards: Agilinx 7 I-series development kit
- PC with a 200 Gigabit Ethernet card installed
- 200G Ethernet cable: QSFP56 AOC cable
- Micro USB cable connecting between FPGA and PC for JTAG connection
- Test application provided by Design Gateway for running on PC: "tcpdatatest.exe" and "tcp\_client\_txrx\_single.exe"
- Quartus Programmer and NiosII command shell, installed on PC

*Note: The hardware listed below is an example for running the demo.*

[1] 200G Network Adapter: NVIDIA MCX623105AC-VDAT ConnectX-6 Ethernet Adapter Card

<https://store.nvidia.com/en-us/networking/store/product/mcx623105ac-vdat/nvidia-connectx-6-dx-en-adapter-card-200gbe-crypto-enabled/>

[2] QSFP56 AOC cable

<https://www.sfpables.com/200g-qsfp56-to-qsfp56-aoc-850nm-3-20-meter-mel-3m-mel-3m>

[3] Test PC:

Motherboard:	ASUS Z690M-PLUS D4
CPU:	Intel i5-12600K CPU 3.6 GHz
RAM:	64 GB DDR4
OS:	64-bit Windows10 OS

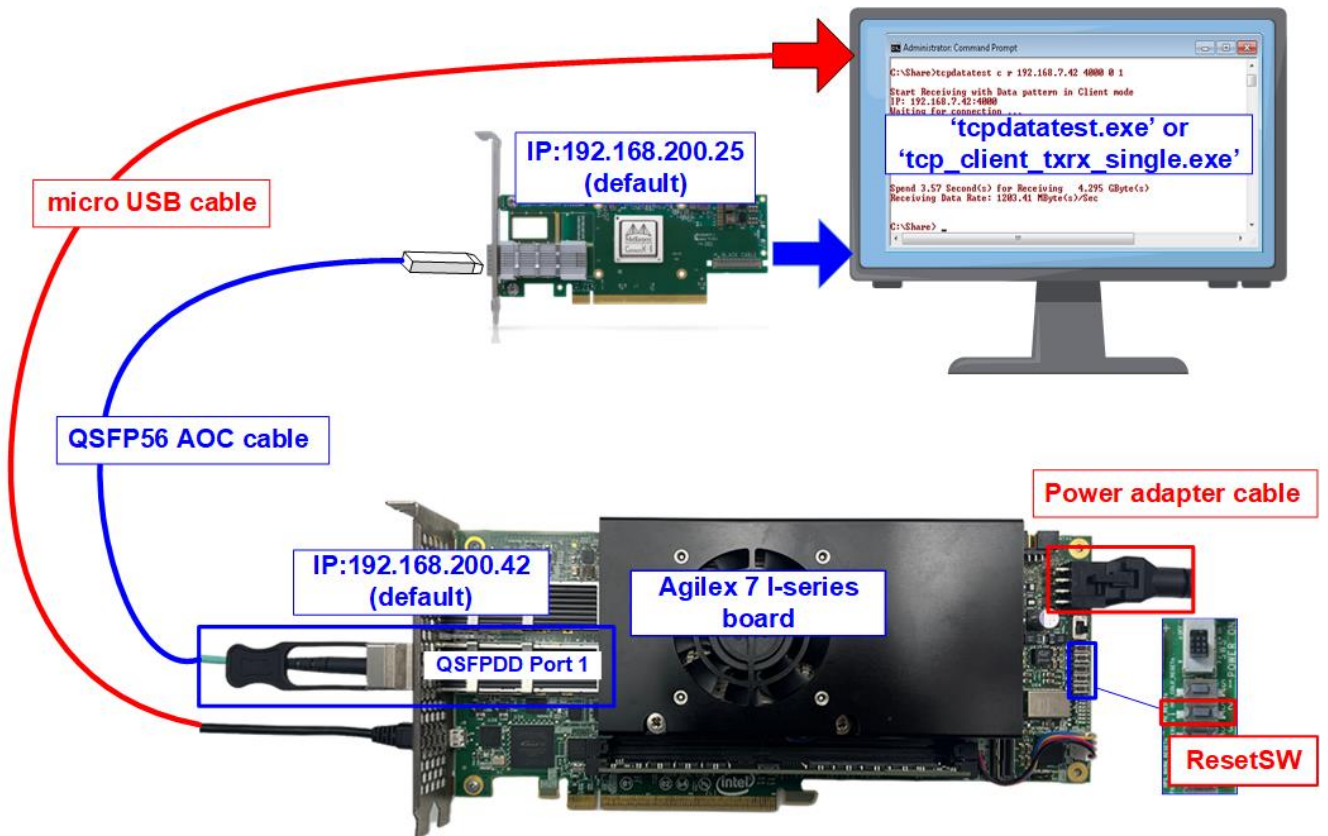


Figure 2-1 TOE200GADV-IP demo (FPGA<->PC) on Agilex 7 I-series

The steps for setting up a test environment using an FPGA board and a PC are described below.

- 1) Turn off power switch and connect the power supply to the FPGA board.
- 2) Connect a micro USB cable from the FPGA board to the PC for JTAG programming and JTAG UART.

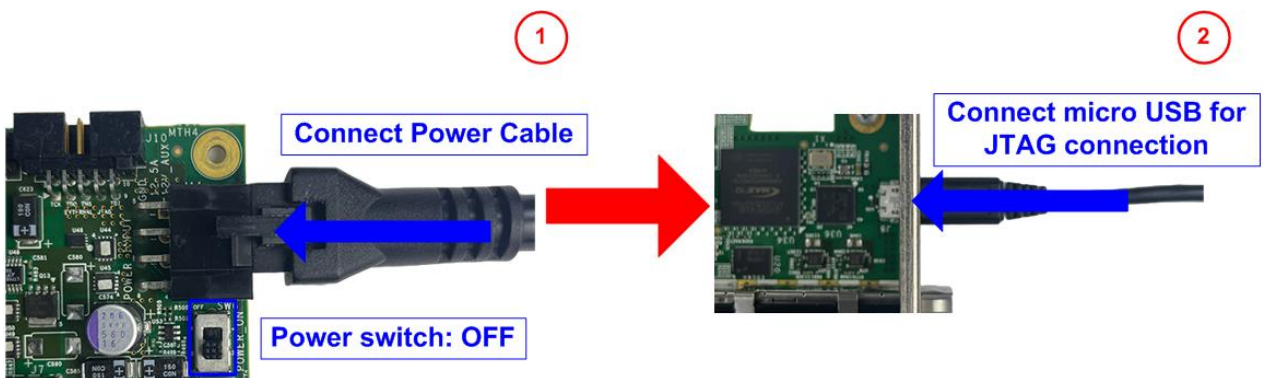


Figure 2-2 Power connection and micro USB connection

- 3) Establish a connection between the FPGA board and the PC by connecting a 200G Ethernet cable. Insert QSFP56 AOC cable between the FPGA board and the PC, as shown in Figure 2-3.

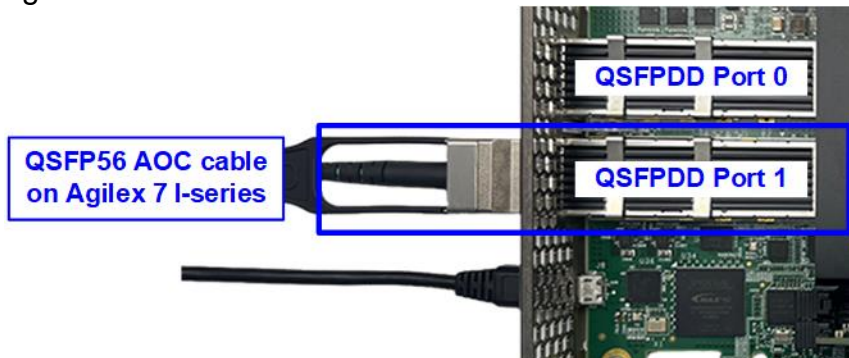


Figure 2-3 200G Ethernet connection

- 4) Please ensure the DIPSW of the FPGA boards is set to configure FPGA by JTAG only. For Agilex 7 I-series board, set bits[1:3] of SW2 to OFF OFF OFF.

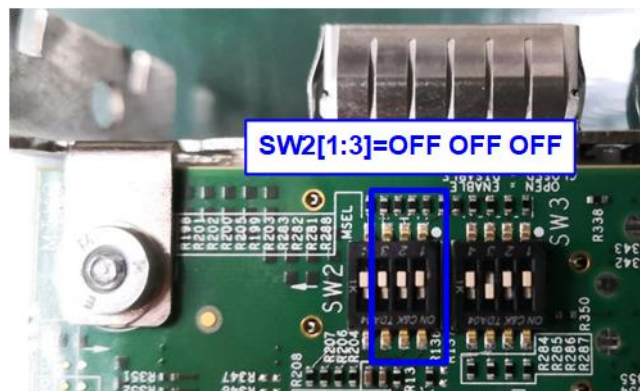


Figure 2-4 SW2 setting on Agilex 7 I-series

- 5) Turn on the power switch on the FPGA board.

- 6) Ensure that the reference clock value is configured correctly. For Agilex 7 I-series board, set clock frequency of Si5391 (OUT0) to 156.25 MHz.

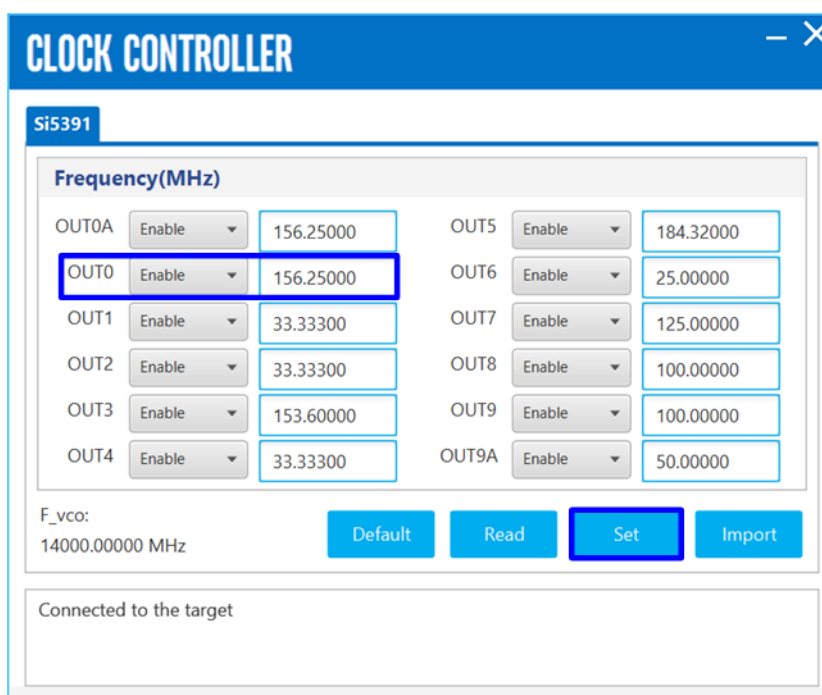


Figure 2-5 Set Clock source of Agilex 7 I-series

- 7) Open Quartus Programmer and follow these steps to program the FPGA via USB-1.
  - i) Click on “Hardware Setup...” and select AGI FPGA Development Kit [USB-1].
  - ii) Click on “Auto Detect” and select the FPGA number.
  - iii) Select the FPGA device icon.
  - iv) Click on the “Change File” button, choose the SOF file in the pop-up window, and click “open” button.
  - v) Check the “Program” option.
  - vi) Click on the “Start” button to program the FPGA.
  - vii) Wait until the Progress status reaches 100%.

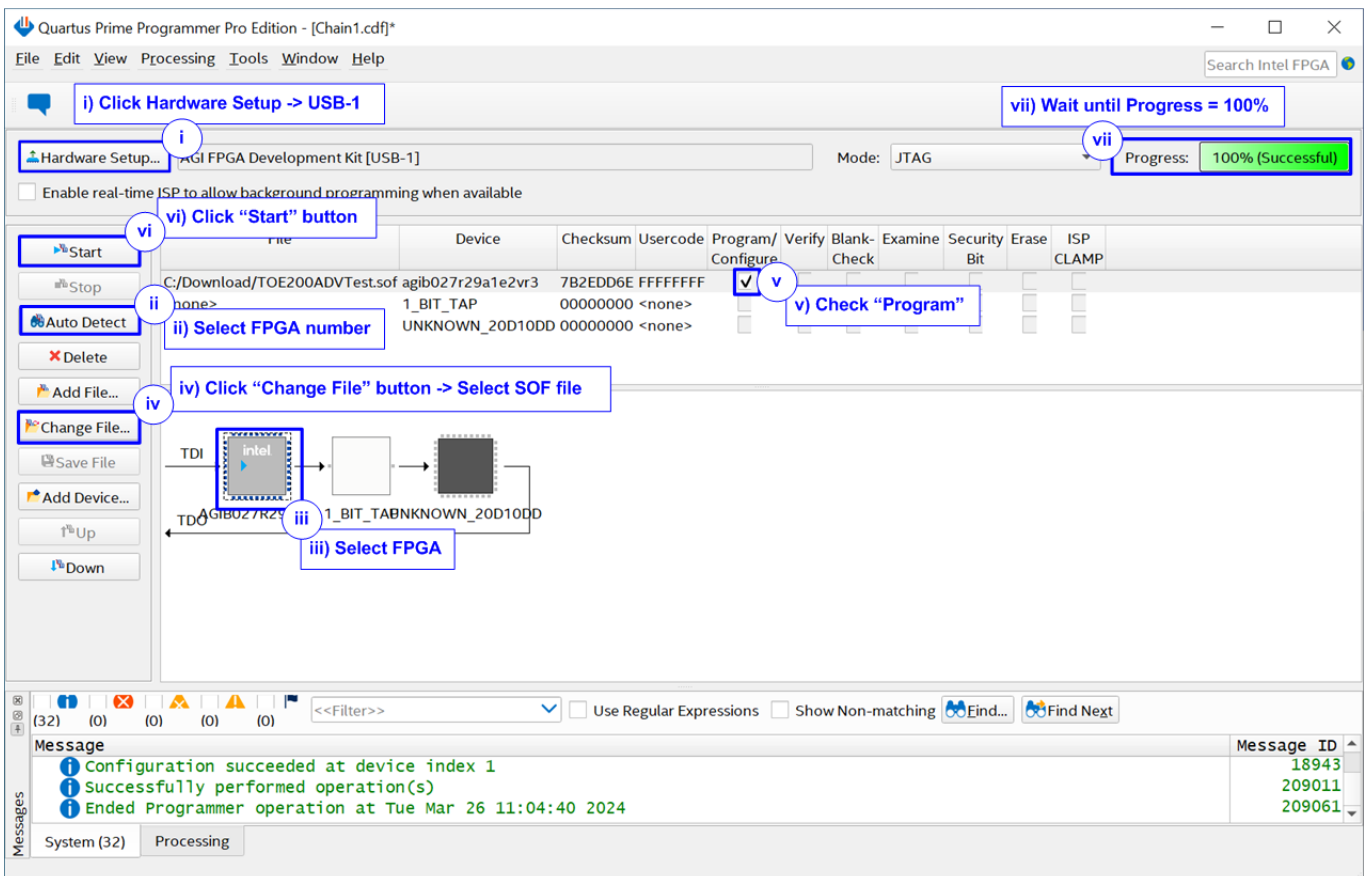
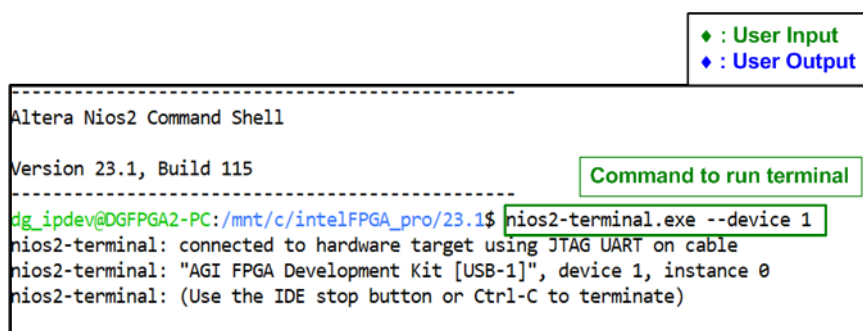


Figure 2-6 FPGA Programmer

- 8) Open the NiosII command shell.
  - i) For Agilx 7 Type “nios2-terminal.exe --device 1” to launch the console.

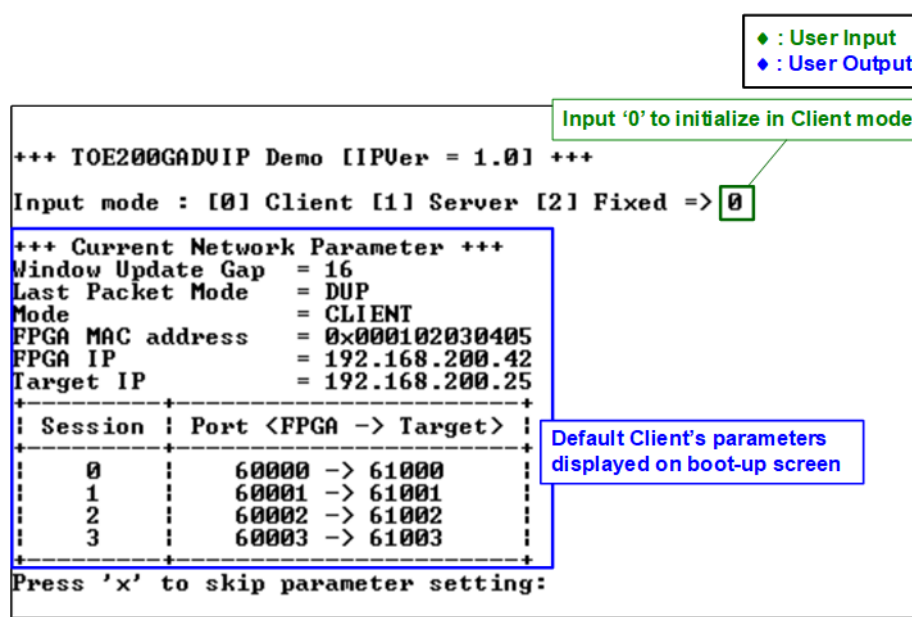


```

Altera Nios2 Command Shell
Version 23.1, Build 115
-----
dg_ipdev@DGFPGA2-PC:/mnt/c/intelFPGA_pro/23.1$ nios2-terminal.exe --device 1
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "AGI FPGA Development Kit [USB-1]", device 1, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)
  
```

Figure 2-7 Run NiosII terminal

- ii) Enter ‘0’ to initiate TOE200GADV-IP initialization in Client mode (which will send an ARP request to retrieve the PC’s MAC address).
- iii) The default parameters for the Client mode will be displayed on the console.



```

+++ TOE200GADV-IP Demo [IPVer = 1.0] +++
Input mode : [0] Client [1] Server [2] Fixed => 0
+++ Current Network Parameter +++
Window Update Gap = 16
Last Packet Mode = DUP
Mode = CLIENT
FPGA MAC address = 0x000102030405
FPGA IP = 192.168.200.42
Target IP = 192.168.200.25
-----
| Session | Port <FPGA -> Target |
-----|-----|
| 0 | 60000 -> 61000 |
| 1 | 60001 -> 61001 |
| 2 | 60002 -> 61002 |
| 3 | 60003 -> 61003 |
-----
Press 'x' to skip parameter setting:
  
```

Figure 2-8 Message after system boot-up



However, if there is an Ethernet connection problem and the status is linked down, an error message will be displayed instead of the welcome message, as shown in Figure 2-9.

```
+++ TOE200GADUIP Demo [IPVer = 1.0] +++
Link Down! Please check cable connection
Current Ethernet MAC status
TX Clock.....OK
RX Clock.....Error
RX Alignment Lock.....Error
RX Block Lock.....Error
Remote Fault.....Not Detect

Link Down! Please check cable connection
Current Ethernet MAC status
TX Clock.....OK
RX Clock.....Error
RX Alignment Lock.....Error
RX Block Lock.....Error
Remote Fault.....Not Detect
```

Error message and Ethernet status displayed when Ethernet link is down

Figure 2-9 Error message when the Ethernet link is down

- iv) If the user wishes to skip parameter setting and use default parameters to start the system initialization, input 'x' as shown in Figure 2-10. If any other keys are entered, the menu for changing parameter will appear, similar to the "Reset TCPIP parameters" menu. The examples of running the main menu of TOE200GADV-IP are described in "dg\_toe200gadvip\_instruction" document.

```
Press 'x' to skip parameter setting: x
IP initialization complete

--- TOE200GADU-IP menu ---
[0] : Display TCPIP parameters
[1] : Reset TCPIP parameters
[2] : Half duplex Test <TOEIP - Target>
[3] : Full duplex Test <TOEIP <-> Target>
[4] : Ping reply Test <FGPA <-> Target>
```

Reset by using default parameter

Main Menu

Figure 2-10 Initialization complete

*Note:* Transfer performance in the demo is limited by the PC performance. The best performance can be achieved when the test is run using FPGA-to-FPGA connection.

### 3 Test environment setup when using two FPGAs

Before running the test, please prepare following test environment.

- Two FPGA development boards: Agilex 7 I-series development kit
- 200G Ethernet cable: QSFP56 AOC cable
- Micro USB cable connecting a FPGA board to PC for JTAG connection
- Quartus Programmer for programming the FPGA and NiosII command shell, installed on PC

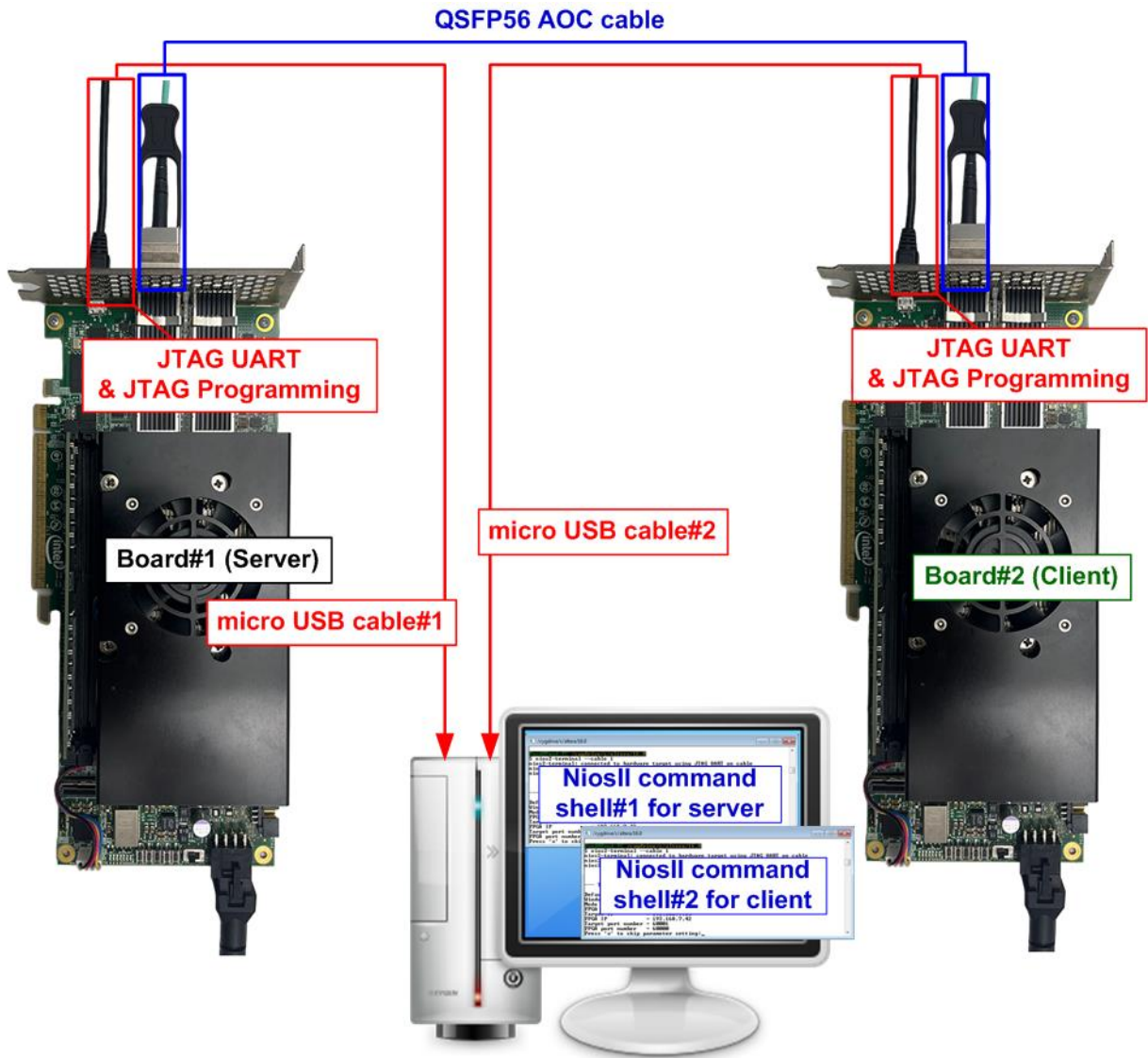


Figure 3-1 TOE200GADV-IP demo (FPGA<->FPGA)

The steps for setting up a test environment using two FPGAs are described below.

To get started with the demo, follow steps 1) – 5) of topic 2 (Test environment setup when using FPGA and PC) to set up the FPGA board and QSFP56 connection. Once you have completed the configuration for two FPGA boards, a menu will be displayed on the console for selecting Client mode, Server mode, or Fixed-MAC mode. Follow the detailed steps below to continue the demo.

*Note: When connecting two FPGA boards to the same PC via USB cable simultaneously, the Quartus programmer will detect two AGI FPGA Development Kit devices, namely USB-1 and USB-2. Choose the appropriate USB channel and start programming the configuration file to first board. Once the first board programming is completed, switch the USB channel and program the configuration file to the second board.*

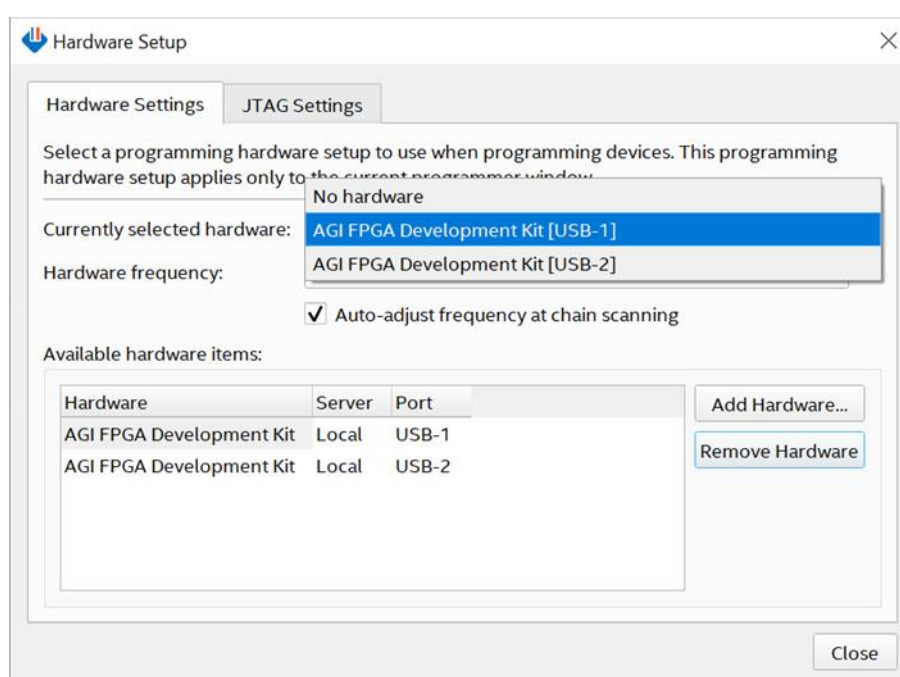


Figure 3-2 Two USB devices are detected when connecting two FPGA boards to PC

- 1) Open NiosII Command Shell.
  - i) Run “nios2-terminal.exe --device 1 --cable 1” command for FPGA#1
  - ii) Run “nios2-terminal.exe --device 1 --cable 2” command for FPGA#2

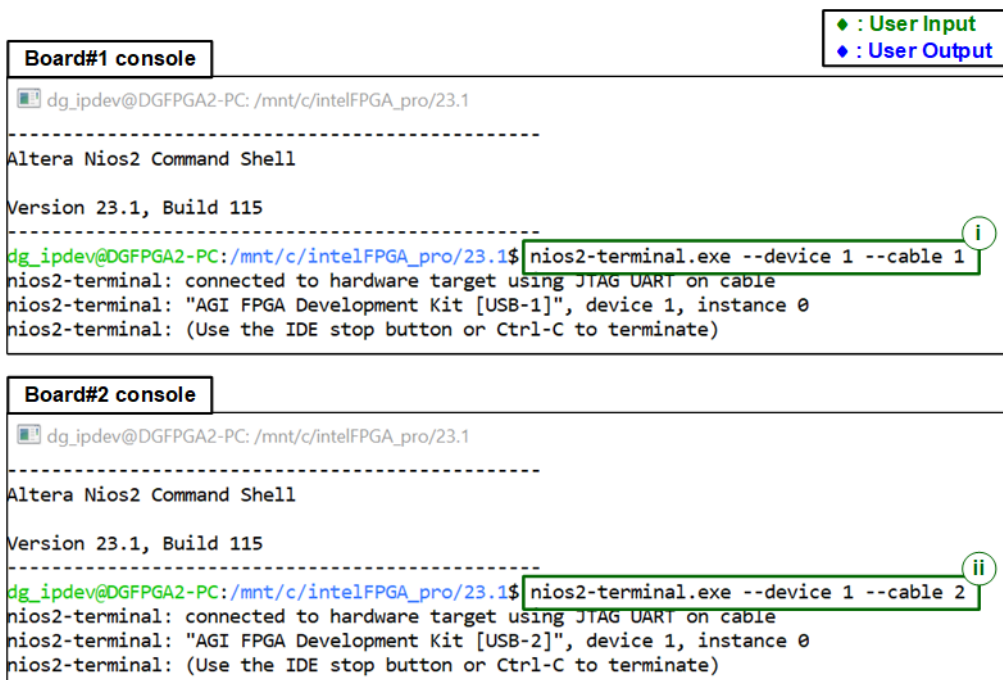


Figure 3-3 Run NiosII terminal on two consoles

- 2) Enter the input to initialize in Server/Client/Fixed-MAC mode. An example to initialize by Server-Client mode is below.
  - i) Set ‘1’ on console of FPGA board#1 for running in Server mode.
  - ii) Set ‘0’ on console of FPGA board#2 for running in Client mode.
  - iii) The default parameters for the selected mode will be displayed on the console, as shown in Figure 3-4.

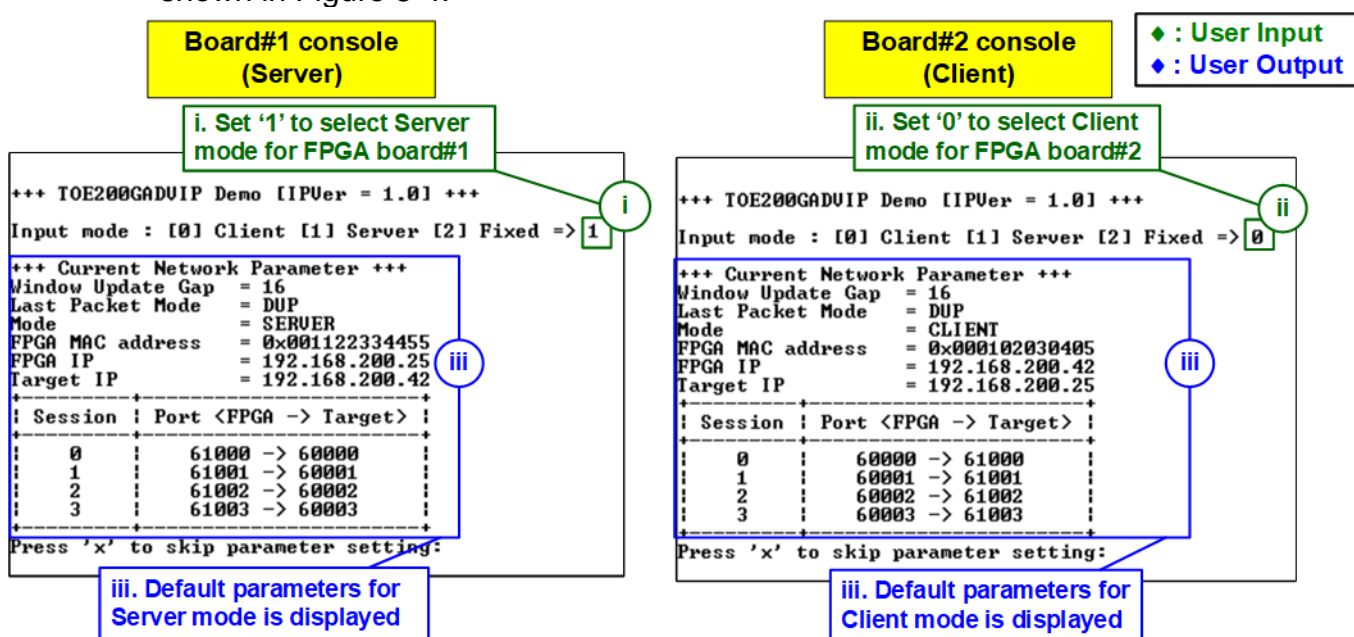


Figure 3-4 Input mode on each FPGA console

Note: The rules for setting the initialization mode are below.

- If the first board is initialized in Server mode, the other board must be initialized in Client mode.
- If the first board is initialized in Fixed-MAC mode, the other board can be run in Client mode or Fixed-MAC mode.

- 3) Input 'x' to use default parameters or use other keys to change parameters. The parameters of Server mode must be set before Client mode.
  - i) Set parameters on the Server console (board#1 console).
  - ii) Set parameters on the Client console (board#2 console) to start IP initialization by transferring ARP packet.
  - iii) After finishing the initialization process, "IP initialization complete" and the main menu are displayed on the Server and Client consoles.

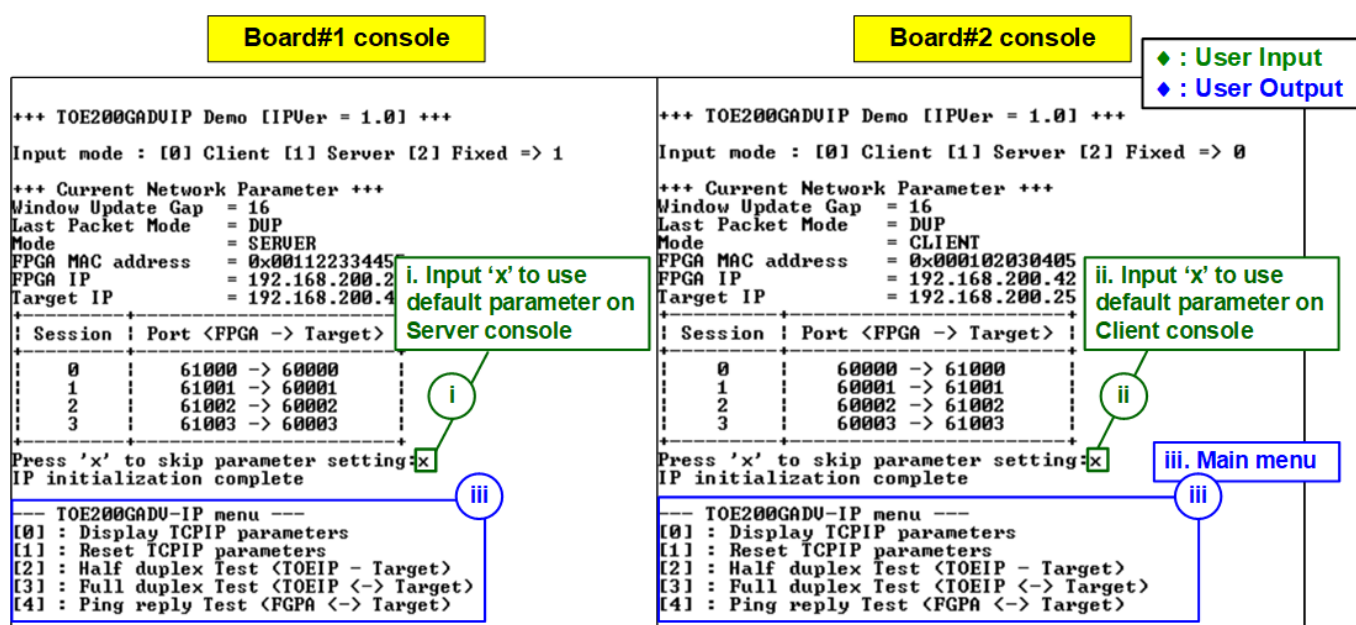


Figure 3-5 Main menu of TOE200GADV-IP

## 4 Revision History

Revision	Date	Description
1.00	13-Jun-24	Initial release