FPGA Setup for TOE200GADV-IP

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1 Introduction

This document provides a guide on setting up an FPGA board and preparing the necessary test environment to run the TOE200GADV-IP demo. The user has the option to create two test environments for transferring TCP payload data via a 200G Ethernet connection using TOE200GADV-IP. Figure 1 illustrates these two options.



Figure 1 Test Environment for the Demo

The first test environment requires one FPGA board and a PC with a 200G Ethernet card for data transfer. The PC runs a test application, such as 'tcpdatatest.exe' (half-duplex test) or 'tcp_client_txrx_single.exe' (full-duplex test). Serial console is also run on the PC to act as the user interface console.

The second test environment involves two FPGA boards. Both boards run the TOE200GADV-IP with different initialization mode assigned (Client, Server, or Fixed-MAC).



2 Test environment setup when using FPGA and PC

Before running the demo using an FPGA and PC, please prepare the following.

- FPGA development boards: VPK120 or VHK158 board.
- PC with a 200 Gigabit Ethernet card installed.
- 200G Ethernet cable: QSFP56 AOC cable.
- USB cable connecting the FPGA to the PC.
 - VPK120: a micro USB cable for programming FPGA and Serial console
 - VKH158: a USB type-C cable for programming FPGA and Serial console.
- Test application provided by Design Gateway for running on PC: "tcpdatatest.exe" and "tcp_client_txrx_ single.exe".
- Vivado tool for programming FPGA installed on PC.

<u>Note</u>: The hardware listed below is an example for running the demo.

- 200G Network Adapter: NVIDIA MCX623105AC-VDAT ConnectX-6 Ethernet Adapter Card <u>https://docs.nvidia.com/networking/display/nvidia-connectx-6-dx-ethernet-adapter-cards-user-manual.pdf</u>
 QSFP56 AOC cable
- ACC cable
 <u>https://www.sfpcables.com/200g-qsfp56-to-qsfp56-acc-850nm-3-20-meter-mel-3m-mel-3m</u>
 Target PC⁻

Targer PC.	
Motherboard:	ASUS Z690M-PLUS D4
CPU:	Intel i5-12600K CPU 3.6 GHz
RAM:	64 GB DDR4
OS:	64-bit Windows10 OS



Figure 2 TOE200GADV-IP Demo (FPGA<->PC) on VPK120





Figure 3 TOE200GADV-IP Demo (FPGA<->PC) on VHK158



The steps for setting up a test environment using an FPGA board and a PC are described below.

1) Set up the FPGA board by setting DIP switch (SW1) to be "ON ON ON ON" and (SW3) to be "OFF ON" to boot from JTAG.





Figure 4 FPGA Board Boot Setting

2) Establish a connection between the FPGA board and the PC by connecting a 200G Ethernet cable. Insert QSFP56 AOC cable between the FPGA board and the PC, as shown in Figure 5.







- Connect USB cable from the FPGA board to PC for JTAG programming and Serial console. The PC should detect and recognize three USB Serial Ports.
 - VPK120 board: Connect a micro USB cable.
 - VHK158 board: Connect a USB Type-C cable.
- 4) Open a Serial console and connect to the third USB Serial port with following settings: Baud rate=115,200, Data=8-bit, Parity=None, and Stop bits=1-bit.

Device Manager	Port:	COM8	~	Close and New open
	Sp <u>e</u> ed:	115200	~	
ile <u>A</u> ction <u>V</u> iew <u>H</u> elp	Data:	8 bit	~	Cancel
	P <u>a</u> rity:	none	~	
	<u>S</u> top bits:	1 bit	~	Help
> 📮 Portable Devices	Elow control:	none	~	
Ports (COM & LPT)	Transr	nit delay		
Communications Port (COM1)	0	msec/ <u>c</u> har	0	msec/line
USB Serial Port (COM30)	Device Friendly N	ame: USB Seri	al Port (C	OM8)
USB Serial Port (COM31)	Device Instance	urer: FTDI	040311	10_00111332143130303
	Driver Date: 7-5-2	021		

Figure 6 Serial Console for Boot-up

5) Power on the FPGA board.

VPK120 board

- i) Wait for the boot message to display on the console.
 - If the message "Connect to this XSDB server use host Xilinx-versal-system-controller-20221 and port 54321" is displayed (as shown in the right window of Figure 7), proceed to step (6).
 - If the message from the BEAM tool is displayed (as shown in the left window of Figure 7), continue to the next step to disable the BEAM tool and enable the user to run "Board User Interface" for clock configuration.

VP	<mark>'K120</mark>
Enable BEAM Tool COM32-Tera Term VT File Edit Setup Control Window Help I 15.772863] xadhI1162]: warning: cannot open library libusb-1.0.so.0, first r ^ equired symbol libusb_init, Xilinx Platform Cable USB cannot be supported I 16.179973] TGP: request_sock_ICF: Possible SYM Flooding on port 2542. Sendin g cookies. Check SNMP counters. I 6.22195] acaptum.shl11311: Connect to this XSDB server use host xilinx-ver sal-system-controller-28221 and port 54321 I 7.2984721 audit: type=1308 audit(4194303753.331:2): pid=1218 uid=0 old-audi e4294967295 aud-1000 tty= 118.0012201 audit: type=1309 audit(4194303753.331:2): con-ce00000h7 syscall=6 f sucd=0 eqid=0 sqid=0 fid=0 f	Disable BEAM Tool COM32-Tera Term VT File Edit Setup Control Window Help a9548 1 5.80802641 rpm-autoload.sh[1760]: Time taken to load BIN is 1676.0000000 Mill i Seconds BIN FILE loaded through FPGA manager successfully I 15.812577] rpm-autoload.sh[1760]: [15.859171] system_controller.sh[2060]: local3.* /var/log/local3.log [15.9 67619] xsdb[2070]: warning: cannot open library libxftdi.so, first required symbol 1 ftdi_new, Digilent FIDI based JTAG cables cannot be supported [15.968760] x sdb[2070]: warning: cannot open library libxftdi.so, first required symbol ftdi_new, Xilinx FIDI based JTAG cables cannot be supported [15.97173] xsdb[2070]: warning: cannot open library libxftdi.so, first required symbol sdb[2070]: warning: cannot open library libxftdi.so, first required symbol ftdi_ new, Xilinx FIDI based JTAG cables cannot be supported [15.971677] xsdb[2070]: wa ring: cannot open library libub-1.8.so.0, first required symbol libusb_init, X liinx Platform Cable USB cannot be supported [17.667977] TGP: request_sock_TCP: Possible SYN flooding on port 2542. Sendin g combins. Check NMP rountersy [17.6635541 acaptun.sh12238]: Connect to this XSDB server use host xilinx-ver sal-system-controller-20221 and port 54321 v

Figure 7 Boot-up Message for VPK120 Board

ii) Close the Serial console to avoid port collisions.



iii) Open the "VPK120 – Board User Interface" application and click "Enable BF on system BSP", as shown in Figure 8.

8	VPK120 - Board User Interface		_	\times		8	VPK120 - Board User Interface			-	×
<u>F</u> ile	Logging Layout <u>H</u> elp					Fil	e Logging Layout Help				
	Run All	iii. Click Enable BF on systemd BSP]	^			Run All]	iv. Enable succes	sful	
\checkmark	Enable BF on systemd BSP	READY TO RUN			_	P	Enable BF on systemd BSP		PASSED		
				 - 1		1					
\square	Sysctrir Boot Check	READY TO RUN									
\checkmark	IDCODE/SW Check	READY TO RUN									
	XCVP1202 EFUSE	READY TO RUN									
	L			_							
	Check Voltages	READY TO RUN									
_				 _							
	Check Clocks	READY TO RUN		~							
\square	Board Interface Tests System	Controller									

Figure 8 Enable Board Framework on VPK120

- iv) Wait until the message "PASSED" is displayed in the "Enable BF on system BSP" status.
- v) Power off and on the board. Re-open the Serial console and check the boot message to ensure the BEAM tool is disabled.

VHK158 board

The Board User Interface is not available for the VHK158 board. Instead, the BEAM tool is used, and its status is displayed in the boot-up message, as shown in Figure 9.

	VHK158		_
💆 COM32 - Tera Term VT		>	<
<u>File Edit Setup Control Window H</u> elp			
<pre>[15.772863] xsdb[1162]: warning equired symbol libusb_init, Xilin; [16.199893] TCP: request_sock_] g cookies. Check SNMP counters. [16.221935] acaptun.sh[131]: sal-system-controller-20221 and p [17.298183] scwebrun.sh[131]: (jupyter/runtime/*': No such file [17.988472] audit: type=1006 at =4294967295 auid=1000 tty=(none) ([18.001220] audit: type=1300 at 4 success=yes exit=4 ad=8 at=ffff =1000 uid=0 gid=0 euid=0 suid=0 fi omm="(systemd)" exe="/lib/systemd, [18.025972] audit: type=1327 at = 18.025972] at = 18.055972] at = 18.055972]</pre>	g: cannot open x Platform Cabl ICP: Possible S connect to this ort 54321 rm: can't remo or directory udit(4194303753 old-ses=4294967 udit(4194303753 svid=0 egid=0 s /systemd" key=(udit(4194303753 ********	<pre>library libusb=1.0.so.0, first : e USB cannot be supported YN flooding on port 2542. Sendin XSDB server use host xilinx-ver ve '/home/petalinux/.local/share .331:2>: pid=1218 uid=0 old-auio 295 ses=1 res=1 .331:2>: arch=c00000b7 syscall=(3=0 items=0 ppid=1 pid=1218 auio gid=0 fsgid=0 tty=(none) ses=1 on null) .331:2>: proctitle="(systemd)"</pre>	r A r e d 6 d c
* BEAM Tool Web Address	Messag	e from	
∗ No IP address is assigned ∗	BEAM t	ool	
***********	****		~

Figure 9 Boot-up Message of BEAM tools for VHK158

6) To configure the programmable clock for the FPGA board, determine whether your board requires a programmable clock setup. If the board has already used the desired clock frequency, you do not need to reconfigure it.

VPK120 board

i) Close the Serial console to avoid port collisions and open the "VPK120 – Board User Interface" application.

cks Voltages Power FM	C QSFPDD GPIO Expander EEPROM Data SYS Ctlr Bank IO About		
t Read Set Boot Frequency	Restore Device Defaults		
Set User1 FMC2 Si570 Frequency	ii) Select "VPK120_100MHz_8A34001_20210316_02 and "VPK120_100MHz_8A34001_20210316_023903	23903_156_25_ 3_156_25_Q789	Q789_corrected.txt" registe 9_corrected.tcs" config file
	txt register file from ./clockFiles folder:		
	VPK120_100MHz_8A34001_20210316_023903_156_25_Q789_corrected.txt ~		
	tcs config file from ./clockFiles folder:	iv) The	setting is successful if the
	VPK120_100MHz_8A34001_20210316_023903_156_25_Q789_corected.tcs ~	followi	ng parameters are updated
	From 8a34001 Q0 CLK0:	Q0: 0	to CLK0
	From Bank 703 CLK1:	Q1 0	to Bank 206 GTM RX2
	From Bank 206 GTM TX2 CLK2:	Q2 0	to Bank 703
Set 8A34001 FMC2 Frequency	From 8a34001 Q4 CLK3:	Q3: 0	to SMA J339
	From SMA J330-331 CLK4:	Q4: 0	to 8a34001 CLK3
	From Bank 202/204 GTM REFCLK1 CLK5:	Q5: 0	to FMC REFCLK C2M
	From Bank 206 GTM REFCLK1 CLK6:	Q6: 0	to Bank 711
	From FMC REFCLK M2C CLK7:	Q7: 156.25	to Bank 206 GTM REFCLK0
		Q8: 156.25	to Bank 204/205 GTM REFCLKP0
		Q9: 156.25	to Bank 202/203 GTM REFCLKP0
		Q10:	to SMA J328
iii) Click "Set 8A	34001 FMC2 Frequency"	Q11: 0	to N.C.

Figure 10 Reference Clock Programming for VPK120

- ii) Select the register file and config file option to the profile: "VPK120_100MHz_8A34001_20210316_023903_ 156_25_Q789_corrected" to set the programmable clock to 156.25 MHz.
- iii) Click "Set 8A34001 FMC2 Frequency" to confirm the clock configuration.
- iv) Wait until the parameters displayed on the right side are updated. Ensure that the clock frequency for Q7 Q9 is set to 156.25.

VHK158 board

Use the system controller to confirm the current clock frequency of the programmable clock on the board as follows:

- i) Press the "ENTER" key to display login console, and log in with the username: "petalinux".
- ii) Enter the following command:
 > sudo cat /sys/kernel/debug/clock/clock_summary
 This command displays the current clock frequency on the FPGA board.
- iii) Verify that the clock frequency values for "rc21008a-0_out0-6" are set to 156.25 MHz, as shown in Figure 11.



Figure 11 Current Clock Frequency of VHK158 Board

If the clock frequencies for "rc21008a-0_out0-6" are not set to 156.25 MHz, follow these steps to configure the new clock values using the BEAM tool:

i) Open the BEAM tool by following the sections: "Board and Requirements", "Board setup and Connection", and "Launching the GUI", available in this link:

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2273738753/Versal+Evaluation+Board+-+System+Controller+-+Update+6#BEAM

- ii) In the BEAM tool, click "TEST THE BOARD" as shown Figure 12.
- iii) Click "Board Settings" and select "Set Clock" from the top menu bar.
- iv) Choose the clock configuration for the "8A34001" with the profile: "8A34001_2020-0318_156MHz".
- v) Click "Set" and wait for the status to display a "check mark" icon, indicating that the configuration is complete.

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Figure 12 Programmable Clock Configuration for VHK158

7) Close the Serial console of the third USB Serial Port and open the Serial console of the first USB Serial port using the same configuration: Baud rate=115,200, Data=8-bit, Parity=None, and Stop bits=1-bit.



Figure 13 Serial console of the First USB Serial Port



8) Download configuration file and firmware to the FPGA board. Open the Vivado TCL shell and navigate to the download directory that contains the BAT file, PDI file, and ELF file. Run the BAT file, as shown in Figure 14.

Vivado 2023.2 Tcl Shell - C:\Xilinx\Vivado/2023.2\bin\vivado.bat -mode tcl -	\times
<pre>****** Vivado v2023.2 (64-bit) **** SW Build 4029153 on Fri Oct 13 20:14:34 MDT 2023 **** SW Build 4028589 on Sat Oct 14 00:45:43 MDT 2023 **** SharedData Build 4025554 on Tue Oct 10 17:18:54 MDT 2023 *** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved. ** Copyright 2022-7 Navigate to download directory Vivado% cd D:/download</pre>	^
Vivado% toe200gadvtest_vpk120.bat Run the configuration file	~

Figure 14 FPGA Configuration Using Script File on Vivado TCL Shell

- 9) On the Serial console, the welcome message will be displayed.
 - i) Enter '0' to initiate the TOE200GADV-IP initialization in Client mode, which will send an ARP request to retrieve the PC's MAC address.
 - ii) The default parameters for Client mode will be displayed on the console.

	 ♦ : User Input ♦ : User Output
+++ TOE200GADVIP Demo [IPVer = 1.0] Input mode : [0] Client [1] Server [4	Input '0' to initialize in Client mode
+++ Current Network Parameter +++ Window Update Gap = 16 Last Packet Mode = DUP Mode = CLIENT FPGA MAC address = 0x000102030405 FPGA IP = 192.168.200.42 Target IP = 192.168.200.25	
Session Port $\langle FPGA - \rangle$ Target> 0 60000 -> 61000 1 60001 -> 61001 2 60002 -> 61002 3 60003 -> 61003	Default Client's parameters displayed on boot-up screen
Press 'x' to skip parameter setting:	•

Figure 15 Boot-up Message of the TOE200GADV-IP Demo



However, if there is an Ethernet connection problem and the link status is down, an error message will be displayed instead of the welcome message, as shown in Figure 16.

+++ TOE200GADVIP Demo [IPVer = 1.0] +++	Error message and
Link Down! Please check cable connection Current Ethernet MAC status	Ethernet status displayed when Ethernet link is down
RX ClockError RX ClockError RX Alignment LockError RX Block LockError Remote FaultNot Detect	
Link Down! Please check cable connection Current Ethernet MAC status IX ClockOK RX ClockError RX Alignment LockError RX Block LockError RA Block LockError Remote FaultNot Detect	

Figure 16 Error message when the Ethernet link is down

- iii) Select the parameter profile.
 - To skip parameter setting and use the default parameters to start system initialization, input 'x', as shown in Figure 17.
 - If any other key is entered, the menu for changing parameters will appear, similar to the "Reset TCPIP parameters" menu.

For detailed examples of running the main menu of TOE200GADV-IP, refer to the "dg_toe200gadvip_ instruction" document.

	Reset using default parameter
Press 'x' to skip pa	rameter setting X
IP initialization co	mplete Main Menu
TOE200GADU-IP me	nu
[0] : Display TCPIP p	parameters
[1] : Reset TCPIP pa	rameters
[2] : Half duplex Te	st (IOEIP - Target)
[3] : Full duplex Te	st (IOEIP <-> Target)
[4] : Ping reply Tes	t (FGPA <-> Target)

Figure 17 Initialization Complete

<u>Note</u>: Transfer performance in the demo is limited by the PC performance. The best performance can be achieved when the test is run using FPGA-to-FPGA connection.



3 Test environment setup when using two FPGAs

Before running the demo using two FPGAs, please prepare the following.

- Two FPGA development boards, which can be either the same or different boards: VPK120 and VHK158 boards.
- 200G Ethernet cable: QSFP56 AOC cable.
- USB cable connecting the FPGA to the PC.
 - VPK120: a micro USB cable for programming FPGA and Serial console
 - VKH158: a USB type-C cable for programming FPGA and Serial console.
- Vivado tool for programming FPGA installed on PC.



Figure 18 TOE200GADV-IP Demo (FPGA<->FPGA)



The steps for setting up a test environment using two FPGAs are described below.

To get started with the demo, follow steps 1) - 8) of topic 2 (Test environment setup when using FPGA and PC) to set up the FPGA board and QSFP56 connection. Once you have completed the configuration for two FPGA boards, a menu will be displayed on the console for selecting Client mode, Server mode, or Fixed-MAC mode. Follow the detailed steps below to continue the demo.

- 1) Open the Serial console for FPGA board#1 and FPGA board#2, which are set to initialize in Server, Client, or Fixed-MAC mode. An example of initialization in Server-Client mode is provided below.
 - i) Set '1' on the console of FPGA board#1 for running in Server mode.
 - ii) Set '0' on the console of FPGA board#2 for running in Client mode.
 - iii) The default parameters for the selected mode will be displayed on the console, as shown in Figure 19.



Figure 19 Input Modes for Each FPGA Console

<u>Note</u>: The rules for setting the initialization mode are below.

- If the first board is initialized in Server mode, the other board must be initialized in Client mode.
- If the first board is initialized in Fixed-MAC mode, the other board can be run in Client mode or Fixed-MAC mode.
- 2) Input 'x' to use default parameters or use other keys to change parameters. The parameters of Server mode must be set before Client mode.
 - i) Set parameters on the Server console (board#1 console).
 - ii) Set parameters on the Client console (board#2 console) to start IP initialization by transferring ARP packet.
 - iii) After finishing the initialization process, "IP initialization complete" and the main menu are displayed on the Server and Client consoles.



Board#1 console	Board#2 console	
Board# FoonSolo	Bould#2 consolo	I User Input
		• : User Output
+++ TOE200GADUIP Demo [IPVer = 1.0] +++	+++ TOE200GADVIP Demo [IPVer = 1.0] +++	
Input mode : [0] Client [1] Server [2] Fixed => 1	Input mode : [0] Client [1] Server [2] F	ixed => 0
+++ Current Network Parameter +++ Window Update Gap = 16 Last Packet Mode = DUP Mode = SERUER FPGA MAC address = 0x00112233445 	++++ Current Network Parameter +++ Window Update Gap = 16 Last Packet Mode = DUP Mode = CLIENT FPGA MAC address = 0x000102030405 IP = 192-168-200.42	
Target IP = 192.168.200.4 default parameter on	Target IP = 192.168.200.25 defa	ult parameter on
Session Port <fpga -=""> Target> Server console</fpga>	Session Port <fpga -=""> Target> Clie</fpga>	nt console
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	
Press 'x' to skip parameter setting x IP initialization complete	Press 'x' to skip parameter setting X IP initialization complete	iii. Main menu
TOE200GADU-IP menu [0] : Display TCPIP parameters [1] : Reset TCPIP parameters [2] : Half duplex Test (TOEIP - Target) [3] : Full duplex Test (TOEIP (-> Target) [4] : Ping reply Test (FGPA (-> Target)	TOE200GADU-IP menu [0] : Display TCPIP parameters [1] : Reset TCPIP parameters [2] : Half duplex Test (TOEIP - Target) [3] : Full duplex Test (TOEIP <-> Target [4] : Ping reply Test (FGPA <-> Target)	,

Figure 20 Main Menu of TOE200GADV-IP

4 Revision History

Revision	Date (D-M-Y)	Description
1.00	4-Dec-24	Initial version release