FPGA Setup for TOE200GADV-IP

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Rev1.00 4-Dec-2024

1 Introduction

This document provides a guide on setting up an FPGA board and preparing the necessary test environment to run the TOE200GADV-IP demo. The user has the option to create two test environments for transferring TCP payload data via a 200G Ethernet connection using TOE200GADV-IP. Figure 1 illustrates these two options.

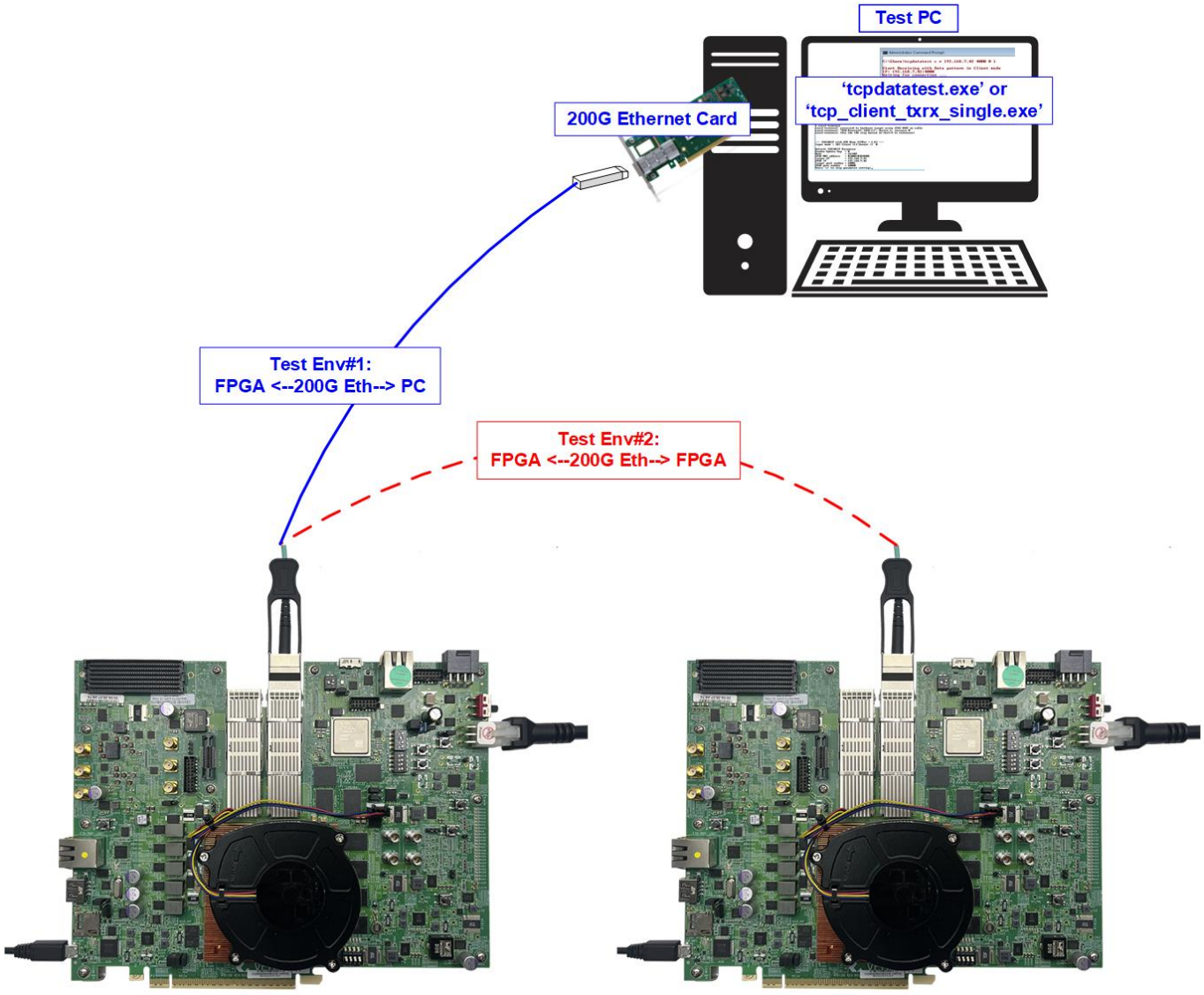

Figure 1 Test Environment for the Demo

The first test environment requires one FPGA board and a PC with a 200G Ethernet card for data transfer. The PC runs a test application, such as 'tcpdatatest.exe' (half-duplex test) or 'tcp_client_txrx_single.exe' (full-duplex test). Serial console is also run on the PC to act as the user interface console.

The second test environment involves two FPGA boards. Both boards run the TOE200GADV-IP with different initialization mode assigned (Client, Server, or Fixed-MAC).

2 Test environment setup when using FPGA and PC

Before running the demo using an FPGA and PC, please prepare the following.

- FPGA development boards: VPK120 or VHK158 board.
- PC with a 200 Gigabit Ethernet card installed.
- 200G Ethernet cable: QSFP56 AOC cable.
- USB cable connecting the FPGA to the PC.
  - VPK120: a micro USB cable for programming FPGA and Serial console
  - VKH158: a USB type-C cable for programming FPGA and Serial console.
- Test application provided by Design Gateway for running on PC: “tcpdatatest.exe” and “tcp_client_txrx_single.exe”.
- Vivado tool for programming FPGA installed on PC.

  Note: The hardware listed below is an example for running the demo.

  - *200G Network Adapter: NVIDIA MCX623105AC-VDAT ConnectX-6 Ethernet Adapter Card*
    https://docs.nvidia.com/networking/display/nvidia-connectx-6-dx-ethernet-adapter-cards-user-manual.pdf
  - *QSFP56 AOC cable*
    https://www.sfpcables.com/200g-qsfp56-to-qsfp56-aoc-850nm-3-20-meter-mel-3m-mel-3m
  - *Target PC:*
    Motherboard: ASUS Z690M-PLUS D4
    CPU: Intel i5-12600K CPU 3.6 GHz
    RAM: 64 GB DDR4
    OS: 64-bit Windows10 OS

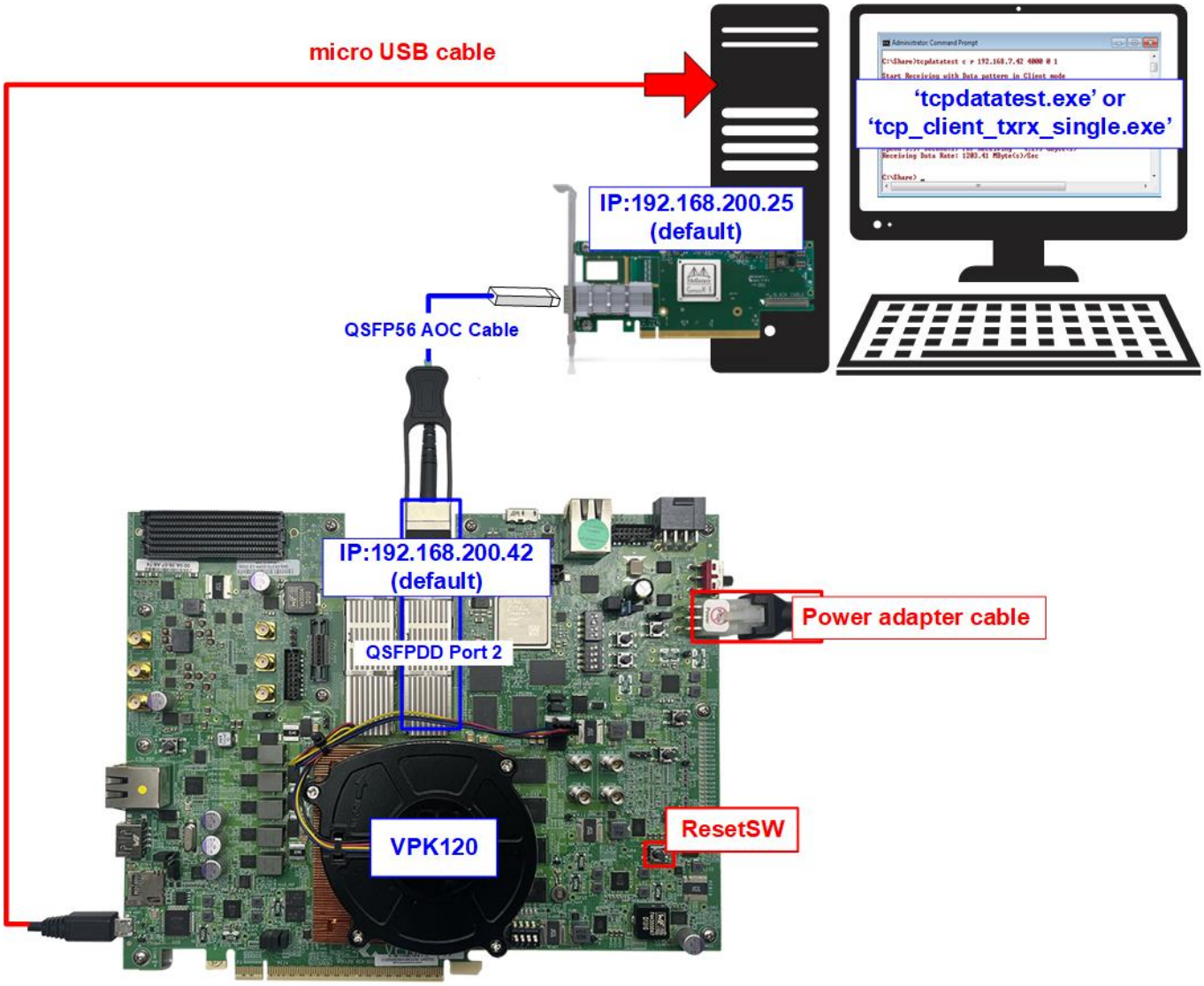

Figure 2 TOE200GADV-IP Demo (FPGA<->PC) on VPK120

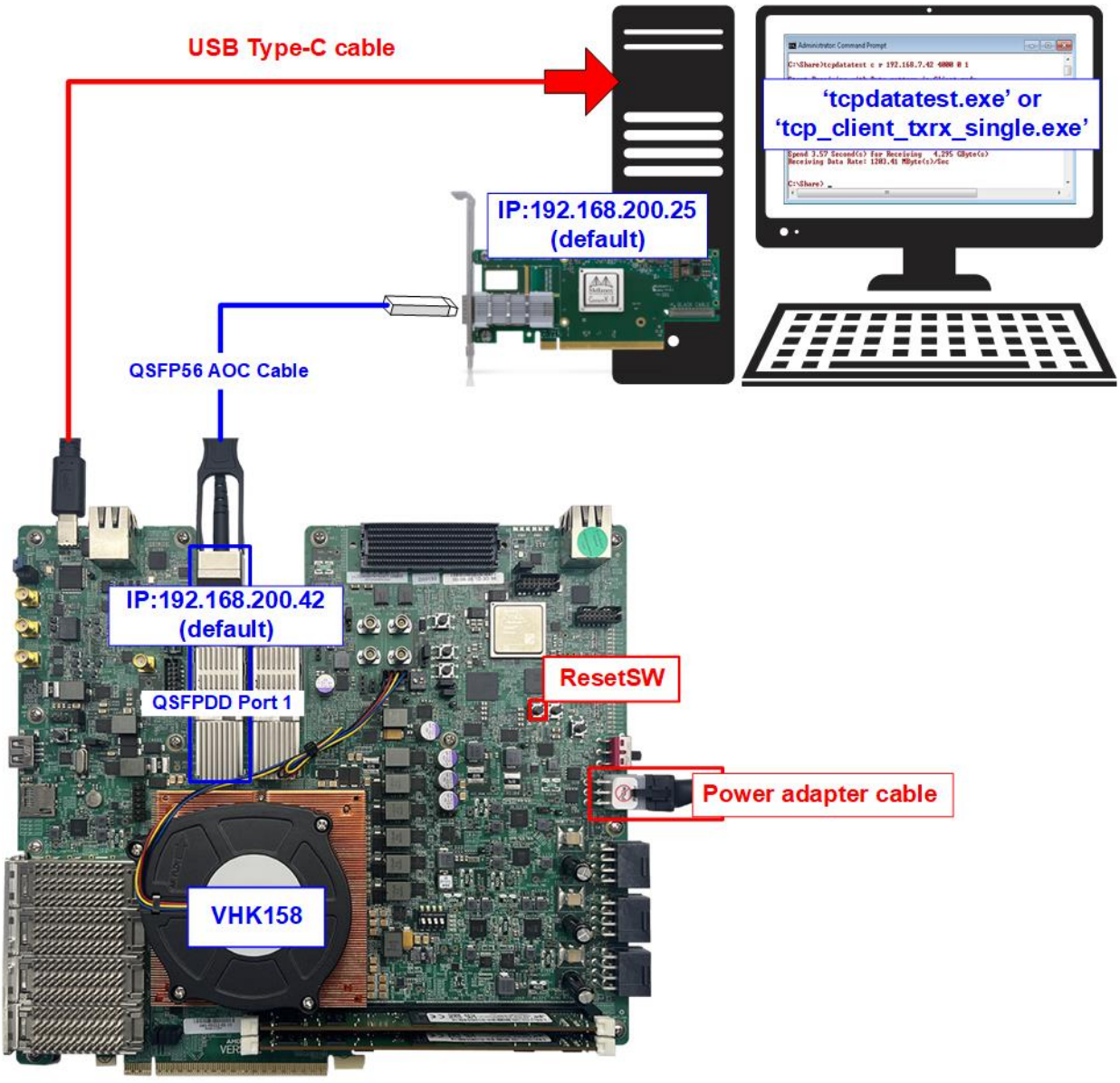

Figure 3 TOE200GADV-IP Demo (FPGA<->PC) on VHK158

The steps for setting up a test environment using an FPGA board and a PC are described below.

1) Set up the FPGA board by setting DIP switch (SW1) to be “ON ON ON ON” and (SW3) to be “OFF ON” to boot from JTAG.

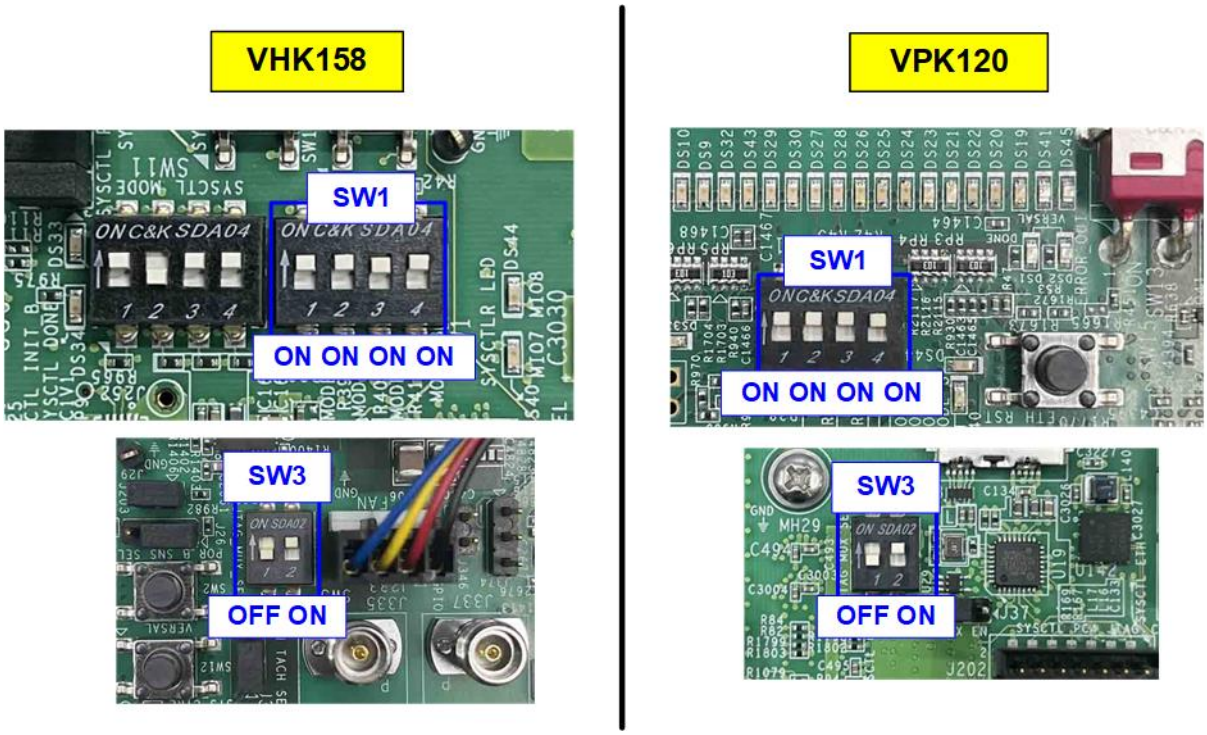

Figure 4 FPGA Board Boot Setting

2) Establish a connection between the FPGA board and the PC by connecting a 200G Ethernet cable. Insert QSFP56 AOC cable between the FPGA board and the PC, as shown in Figure 5.

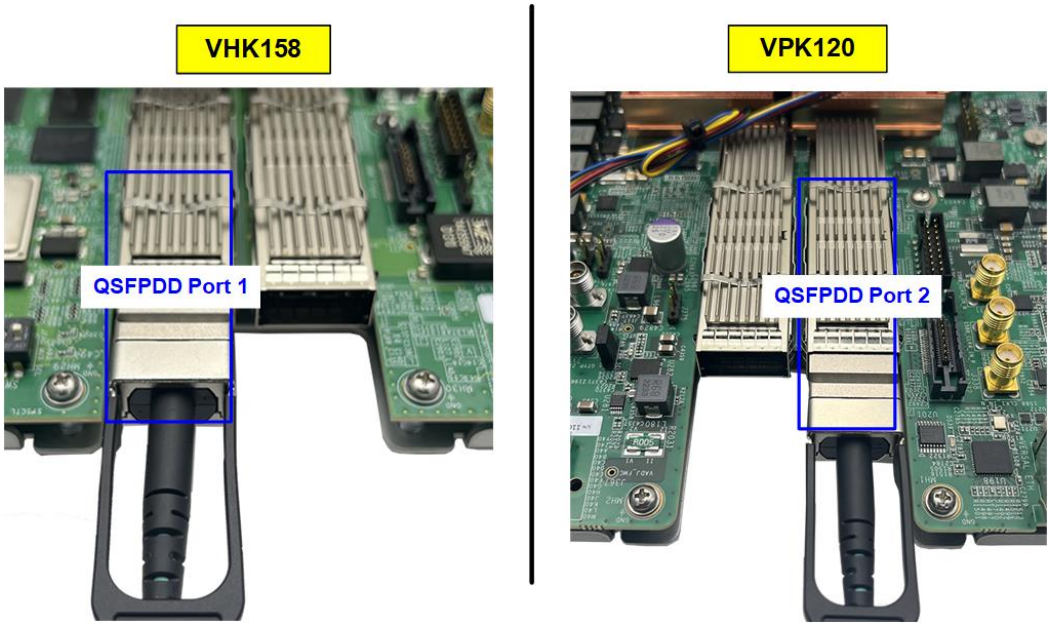

Figure 5 200G Ethernet Connection

3) Connect USB cable from the FPGA board to PC for JTAG programming and Serial console. The PC should detect and recognize three USB Serial Ports.
   - VPK120 board: Connect a micro USB cable.
   - VHK158 board: Connect a USB Type-C cable.

4) Open a Serial console and connect to the third USB Serial port with following settings: Baud rate=115,200, Data=8-bit, Parity=None, and Stop bits=1-bit.

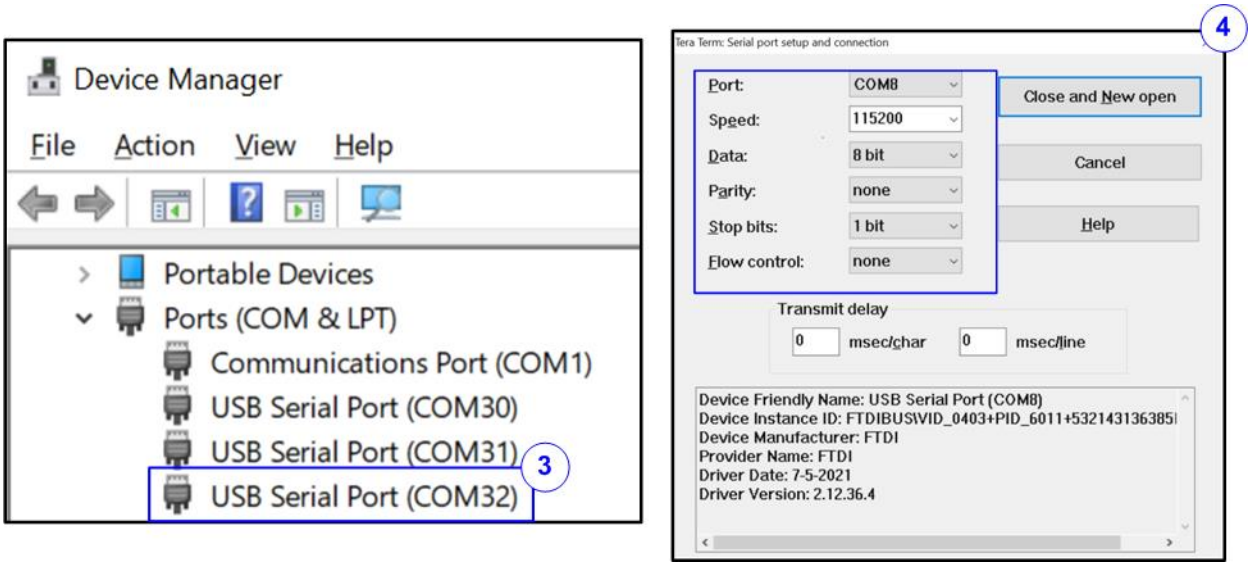

Figure 6 Serial Console for Boot-up

5) Power on the FPGA board.

VPK120 board

i) Wait for the boot message to display on the console.
   - If the message “Connect to this XSDB server use host Xilinx-versal-system-controller-20221 and port 54321” is displayed (as shown in the right window of Figure 7), proceed to step (6).
   - If the message from the BEAM tool is displayed (as shown in the left window of Figure 7), continue to the next step to disable the BEAM tool and enable the user to run “Board User Interface” for clock configuration.

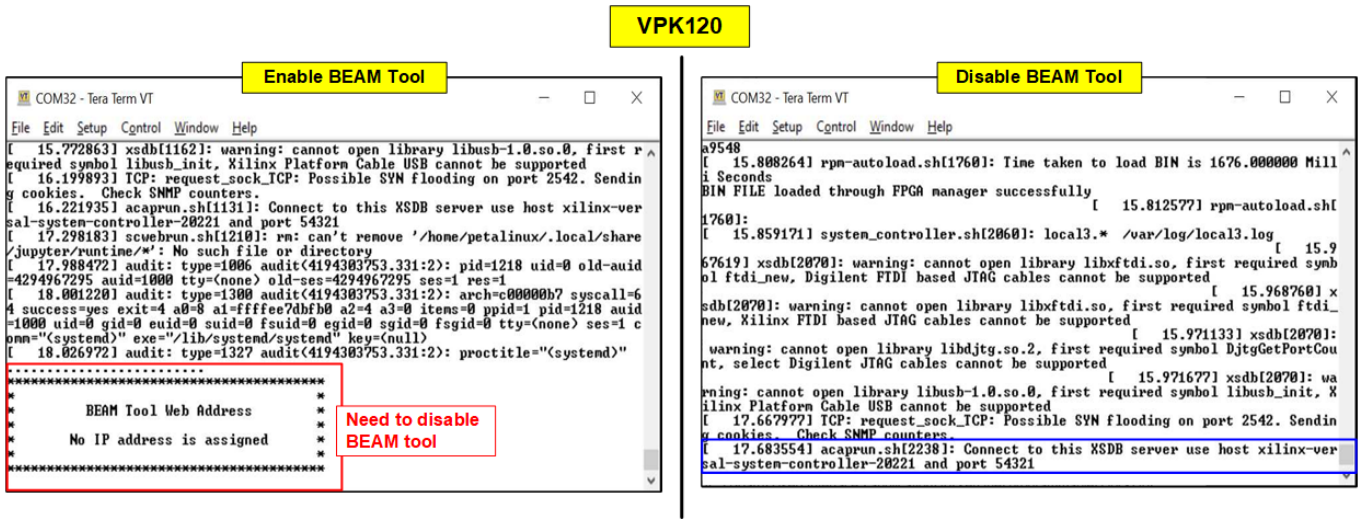

Figure 7 Boot-up Message for VPK120 Board

ii) Close the Serial console to avoid port collisions.

iii) Open the “VPK120 – Board User Interface” application and click “Enable BF on system BSP”, as shown in Figure 8.

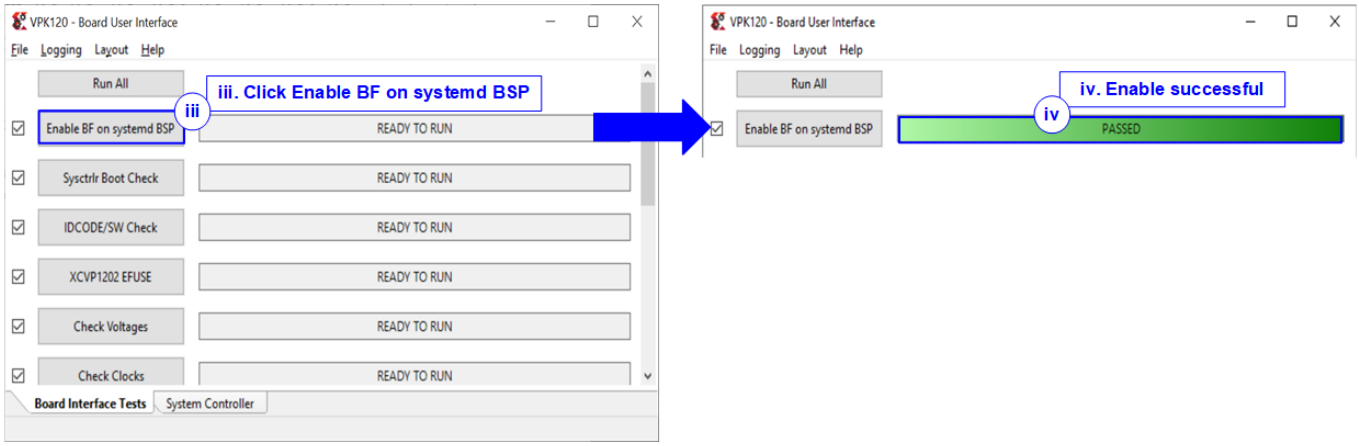

Figure 8 Enable Board Framework on VPK120

iv) Wait until the message “PASSED” is displayed in the “Enable BF on system BSP” status.
v) Power off and on the board. Re-open the Serial console and check the boot message to ensure the BEAM tool is disabled.

VHK158 board

The Board User Interface is not available for the VHK158 board. Instead, the BEAM tool is used, and its status is displayed in the boot-up message, as shown in Figure 9.

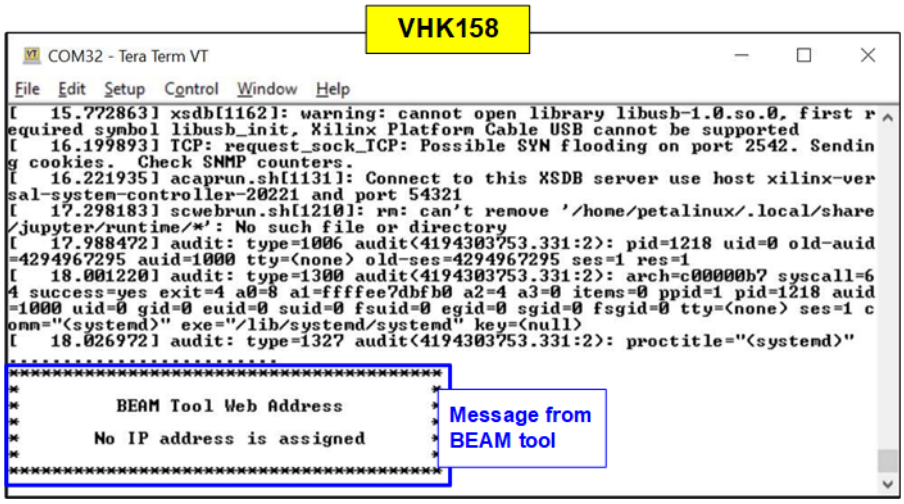

Figure 9 Boot-up Message of BEAM tools for VHK158

6) To configure the programmable clock for the FPGA board, determine whether your board requires a programmable clock setup. If the board has already used the desired clock frequency, you do not need to re-configure it.

VPK120 board

i) Close the Serial console to avoid port collisions and open the “VPK120 – Board User Interface” application.

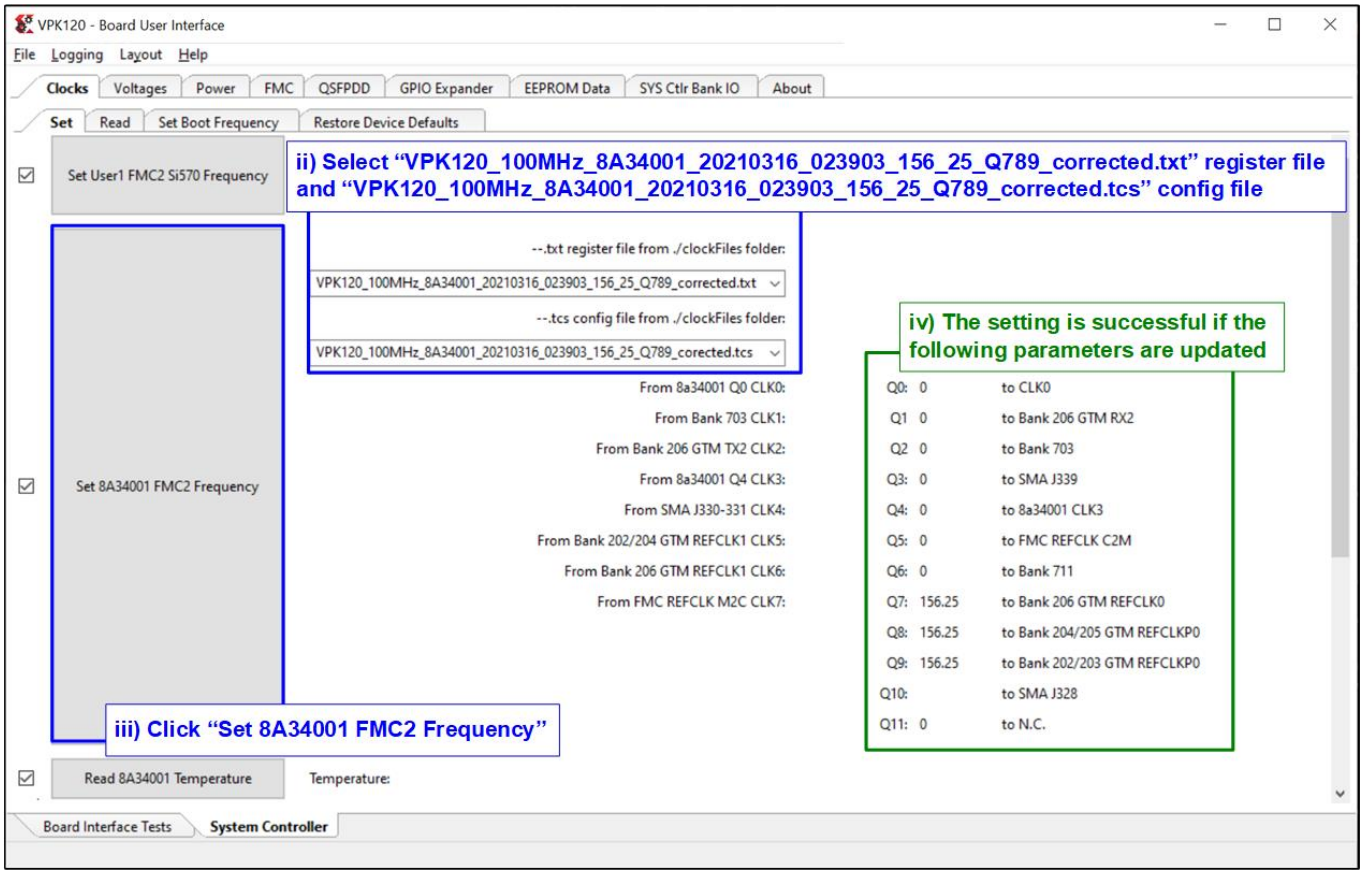

Figure 10 Reference Clock Programming for VPK120

ii) Select the register file and config file option to the profile: “VPK120_100MHz_8A34001_20210316_023903_156_25_Q789_corrected” to set the programmable clock to 156.25 MHz.
iii) Click “Set 8A34001 FMC2 Frequency” to confirm the clock configuration.
iv) Wait until the parameters displayed on the right side are updated. Ensure that the clock frequency for Q7 – Q9 is set to 156.25.

VHK158 board

Use the system controller to confirm the current clock frequency of the programmable clock on the board as follows:

i) Press the “ENTER” key to display login console, and log in with the username: “petalinux”.
ii) Enter the following command:
>> sudo cat /sys/kernel/debug/clock/clock_summary
This command displays the current clock frequency on the FPGA board.
iii) Verify that the clock frequency values for “rc21008a-0_out0-6” are set to 156.25 MHz, as shown in Figure 11.

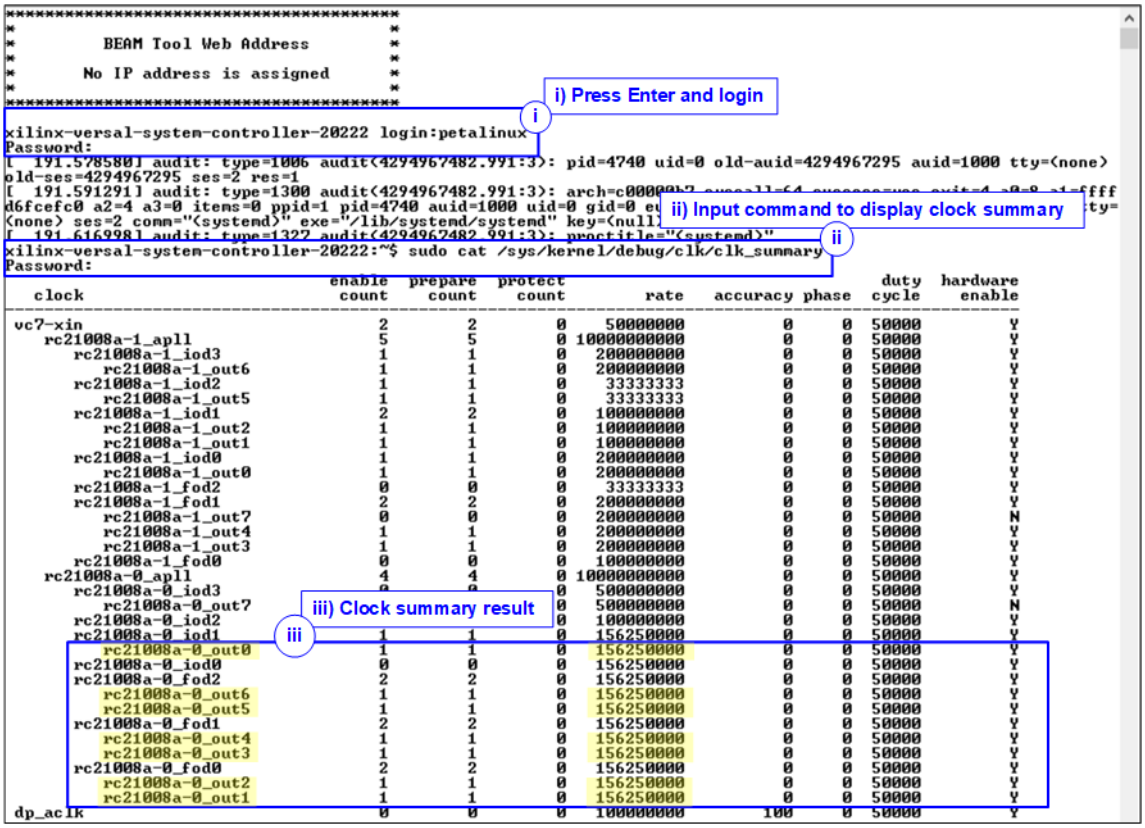

Figure 11 Current Clock Frequency of VHK158 Board

If the clock frequencies for “rc21008a-0_out0-6” are not set to 156.25 MHz, follow these steps to configure the new clock values using the BEAM tool:

i) Open the BEAM tool by following the sections: “Board and Requirements”, “Board setup and Connection”, and “Launching the GUI”, available in this link:

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2273738753/Versal+Evaluation+Board+-+System+Controller+-+Update+6#BEAM

ii) In the BEAM tool, click “TEST THE BOARD” as shown Figure 12.
iii) Click “Board Settings” and select “Set Clock” from the top menu bar.
iv) Choose the clock configuration for the “8A34001” with the profile: “8A34001_2020-0318_156MHz”.
v) Click “Set” and wait for the status to display a “check mark” icon, indicating that the configuration is complete.

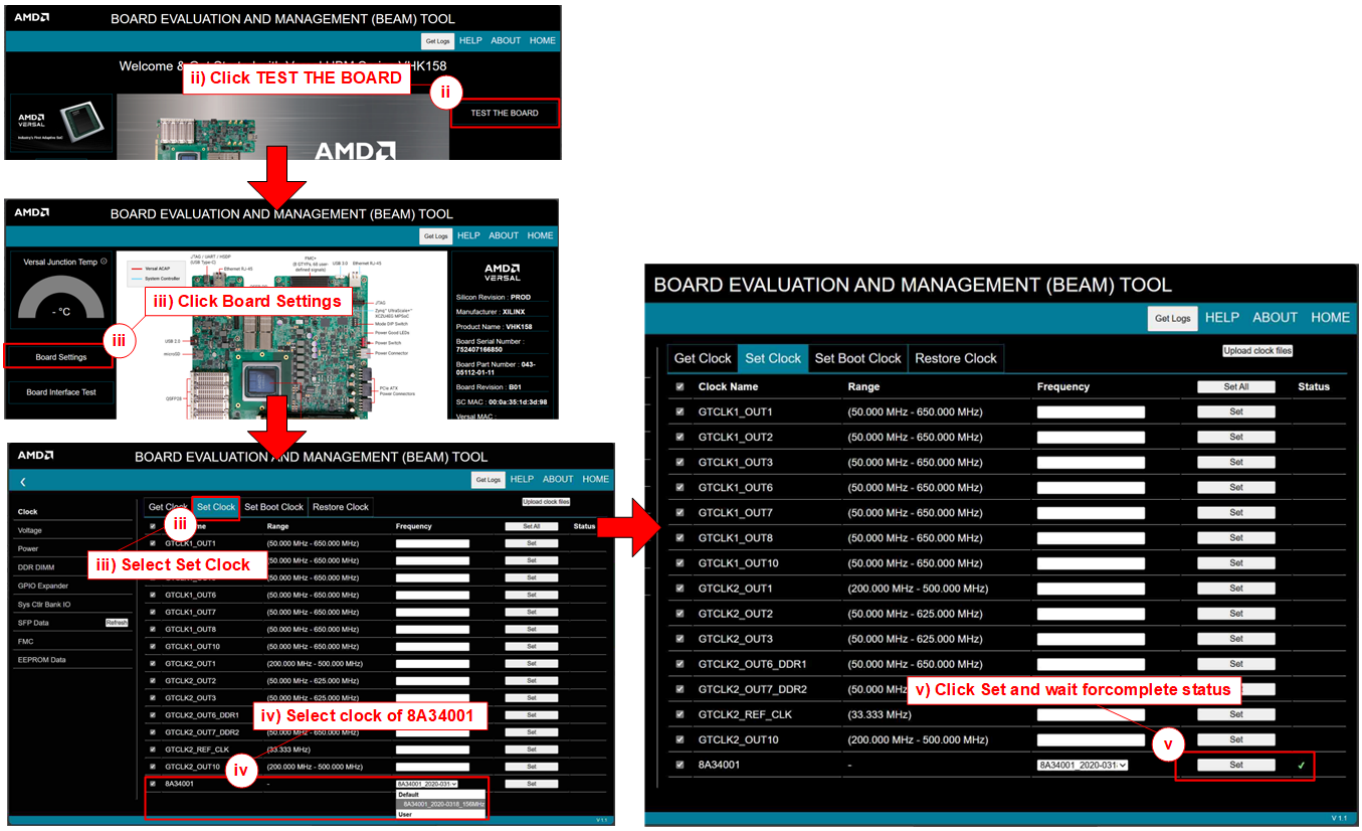

Figure 12 Programmable Clock Configuration for VHK158

7) Close the Serial console of the third USB Serial Port and open the Serial console of the first USB Serial port using the same configuration: Baud rate=115,200, Data=8-bit, Parity=None, and Stop bits=1-bit.

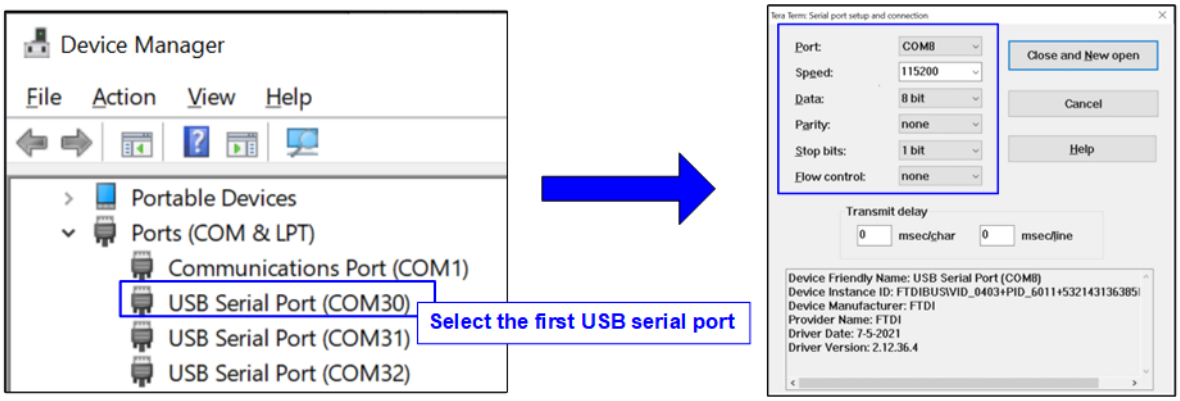

Figure 13 Serial console of the First USB Serial Port

8) Download configuration file and firmware to the FPGA board. Open the Vivado TCL shell and navigate to the download directory that contains the BAT file, PDI file, and ELF file. Run the BAT file, as shown in Figure 14.

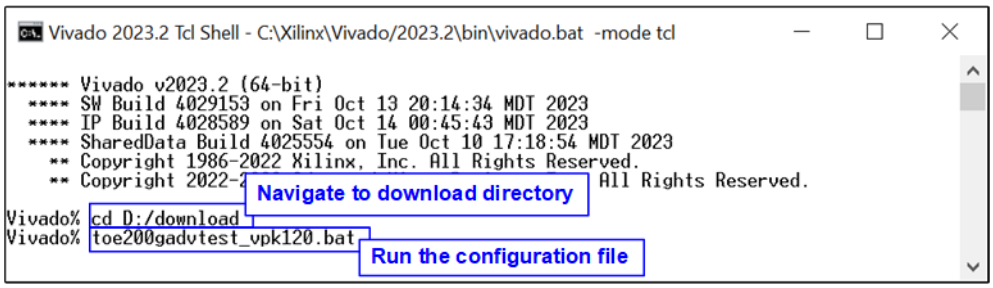

Figure 14 FPGA Configuration Using Script File on Vivado TCL Shell

9) On the Serial console, the welcome message will be displayed.

   i) Enter '0' to initiate the TOE200GADV-IP initialization in Client mode, which will send an ARP request to retrieve the PC's MAC address.
   ii) The default parameters for Client mode will be displayed on the console.

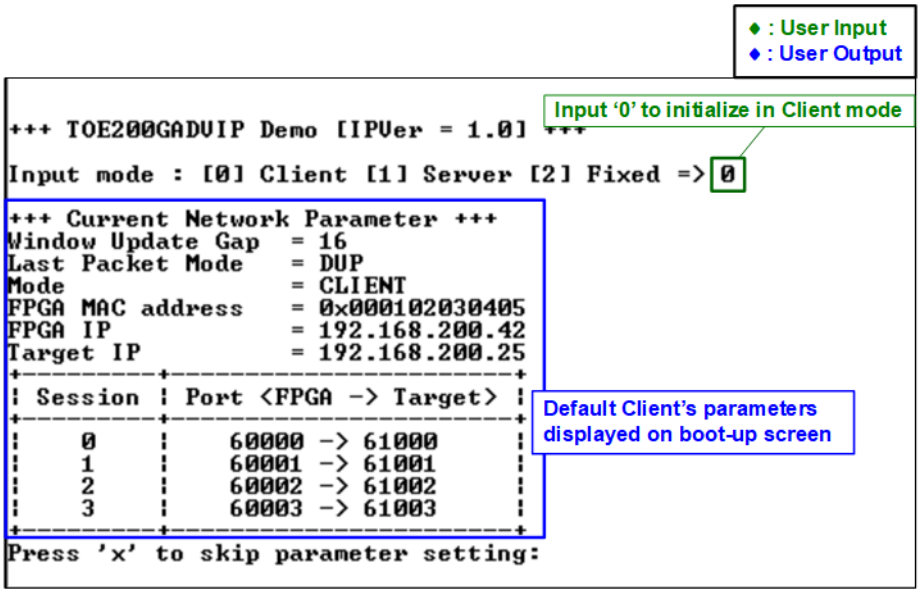

Figure 15 Boot-up Message of the TOE200GADV-IP Demo

However, if there is an Ethernet connection problem and the link status is down, an error message will be displayed instead of the welcome message, as shown in Figure 16.

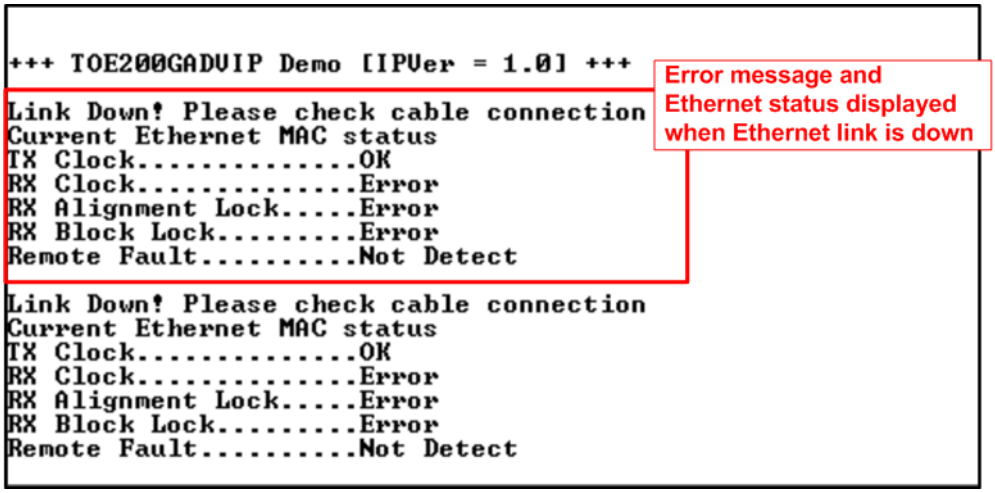

Figure 16 Error message when the Ethernet link is down

iii) Select the parameter profile.

- To skip parameter setting and use the default parameters to start system initialization, input 'x', as shown in Figure 17.
- If any other key is entered, the menu for changing parameters will appear, similar to the "Reset TCPIP parameters" menu.

For detailed examples of running the main menu of TOE200GADV-IP, refer to the "dg_toe200gadvip_ instruction" document.

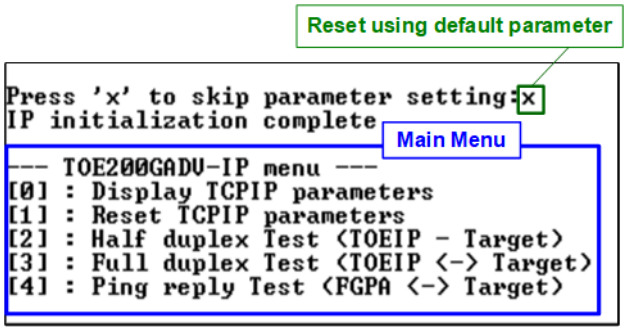

Figure 17 Initialization Complete

Note: Transfer performance in the demo is limited by the PC performance. The best performance can be achieved when the test is run using FPGA-to-FPGA connection.

3 Test environment setup when using two FPGAs

Before running the demo using two FPGAs, please prepare the following.

- Two FPGA development boards, which can be either the same or different boards: VPK120 and VHK158 boards.
- 200G Ethernet cable: QSFP56 AOC cable.
- USB cable connecting the FPGA to the PC.
  - VPK120: a micro USB cable for programming FPGA and Serial console
  - VKH158: a USB type-C cable for programming FPGA and Serial console.
- Vivado tool for programming FPGA installed on PC.

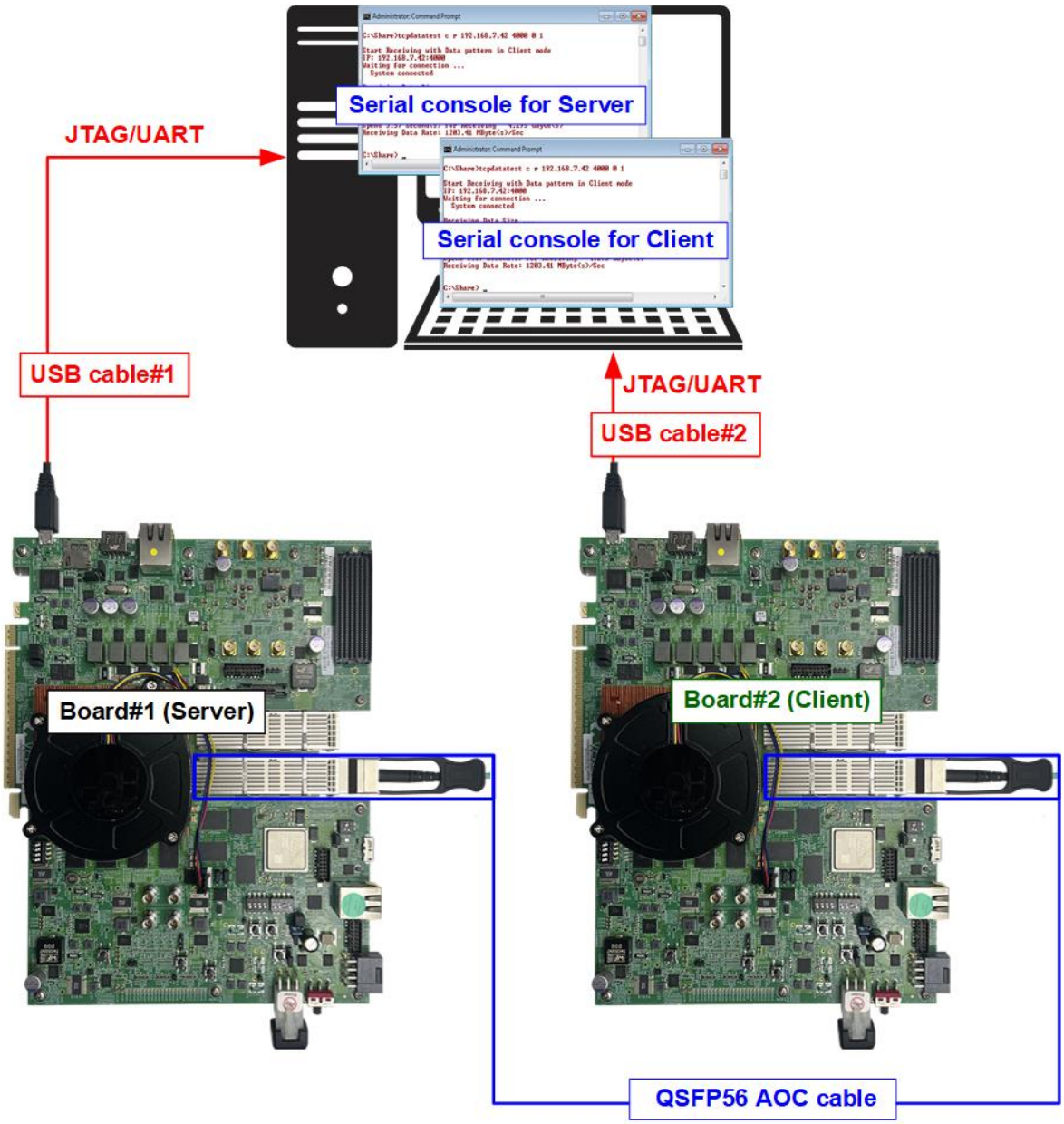

Figure 18 TOE200GADV-IP Demo (FPGA<->FPGA)

The steps for setting up a test environment using two FPGAs are described below.

To get started with the demo, follow steps 1) – 8) of topic 2 (Test environment setup when using FPGA and PC) to set up the FPGA board and QSFP56 connection. Once you have completed the configuration for two FPGA boards, a menu will be displayed on the console for selecting Client mode, Server mode, or Fixed-MAC mode. Follow the detailed steps below to continue the demo.

1) Open the Serial console for FPGA board#1 and FPGA board#2, which are set to initialize in Server, Client, or Fixed-MAC mode. An example of initialization in Server-Client mode is provided below.

   i) Set '1' on the console of FPGA board#1 for running in Server mode.
   ii) Set '0' on the console of FPGA board#2 for running in Client mode.
   iii) The default parameters for the selected mode will be displayed on the console, as shown in Figure 19.

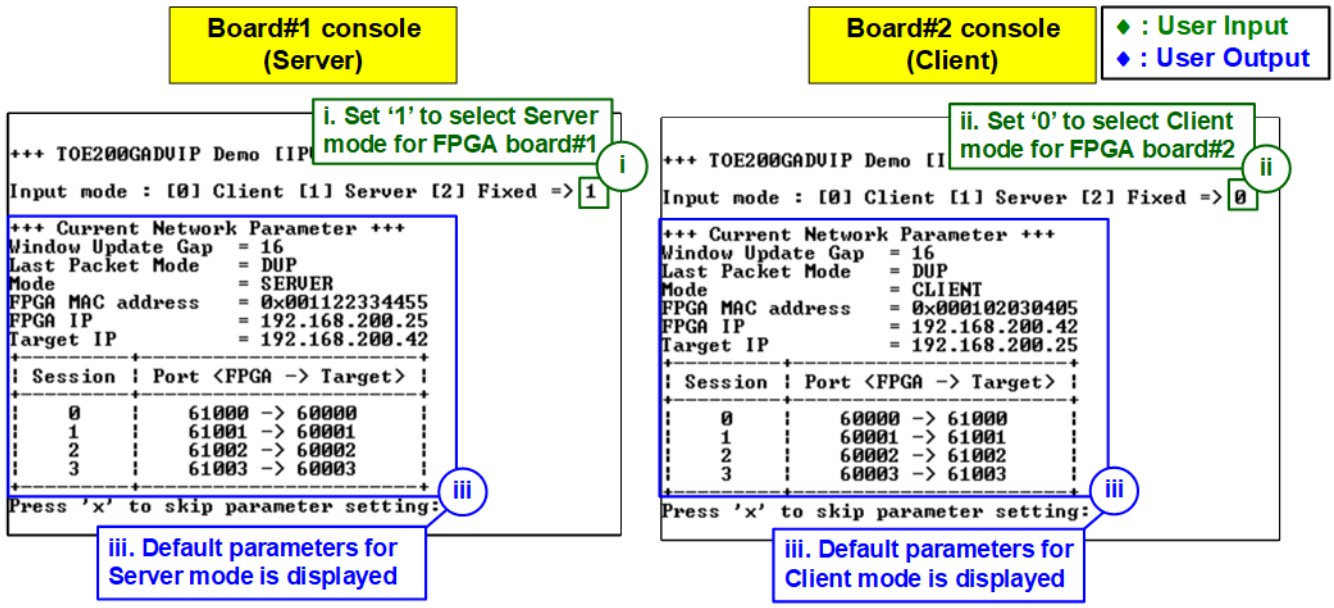

Figure 19 Input Modes for Each FPGA Console

Note: The rules for setting the initialization mode are below.

- *If the first board is initialized in Server mode, the other board must be initialized in Client mode.*
- *If the first board is initialized in Fixed-MAC mode, the other board can be run in Client mode or Fixed-MAC mode.*

2) Input 'x' to use default parameters or use other keys to change parameters. The parameters of Server mode must be set before Client mode.

   i) Set parameters on the Server console (board#1 console).
   ii) Set parameters on the Client console (board#2 console) to start IP initialization by transferring ARP packet.
   iii) After finishing the initialization process, "IP initialization complete" and the main menu are displayed on the Server and Client consoles.

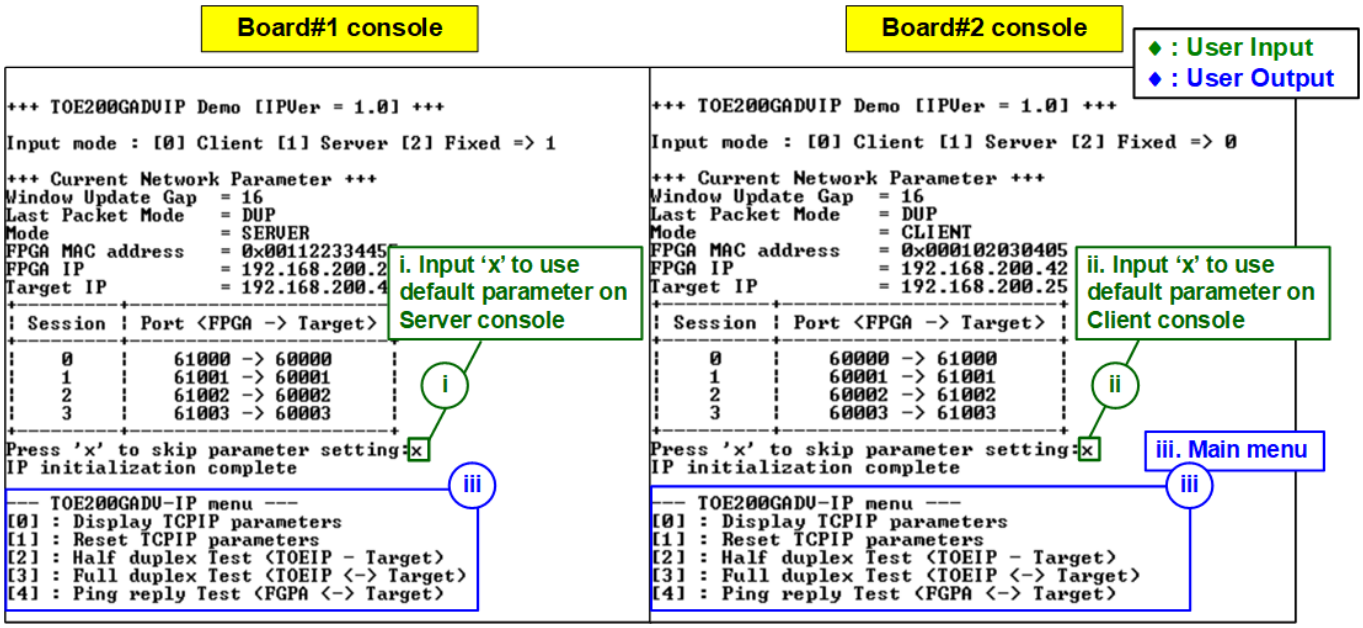

Figure 20 Main Menu of TOE200GADV-IP

4 Revision History

Revision	Date (D-M-Y)	Description
1.00	4-Dec-24	Initial version release

