

FPGA Setup for TOE/UDP1G IP with CPU Demo

Rev3.0 10-Nov-20

This document describes how to setup FPGA board and prepare the test environment for running TOE1G-IP or UDP1G-IP demo. The user can setup two test environments for transferring TCP data or UDP data via 1Gb Ethernet connection by using TOE1G-IP or UDP1G-IP, as shown in Figure 1-1.

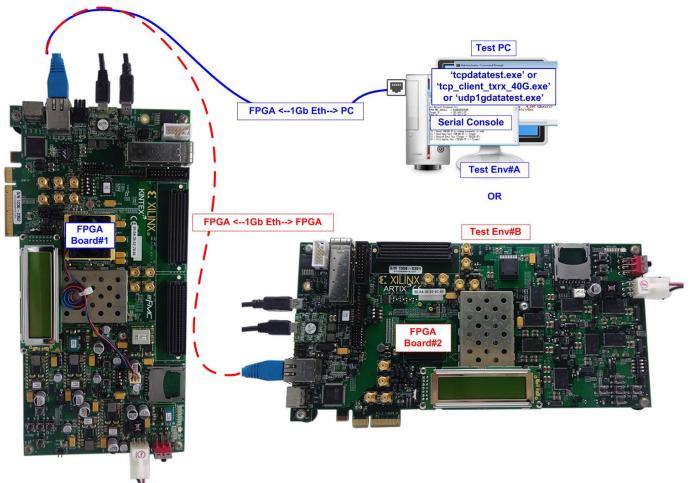


Figure 1-1 Two test environments for running the demo

First uses one FPGA board and Test PC with 1Gb Ethernet card for transferring the data. Test PC runs test application, i.e., tcpdatatest (half-duplex test for TOE1G-IP), tcp_client_txrx_40G for (full-duplex test for TOE1G-IP) or udp1gdatatest (test application for UDP1G-IP). Also, Serial console is run on Test PC to be user interface console.

Second uses two FPGA boards which may be different board or the same board. Both boards run TOE1G-IP or UDP1G-IP demo with assigning the different initialization mode (Client for Server) for transferring data.



1 Test environment setup when using FPGA and PC

Before running the test, please prepare following test environment.

- FPGA development boards: ZC706/KC705/AC701 board
- PC with 1 Gigabit Ethernet or connecting with 1 Gigabit Ethernet card
- 1Gb Ethernet connection: Cat5e or Cat6 cable for between FPGA and PC/FPGA <u>Note</u>: When using ZC706, SFP+ to RJ45 adapter for connecting to SFP+ connector on ZC706 board must be used.
- micro USB cable for programming FPGA, connecting between FPGA board and PC
- mini USB cable for Serial console, connecting between FPGA board and PC
- Test application provided by Design Gateway for running on Test PC: TOE1G-IP: "tcpdatatest.exe" and "tcp_client_txrx_40G.exe" UDP1G-IP: "udp1gdatatest.exe"
- Serial console software such as TeraTerm installed on PC. The setting on the console is Baud rate=115,200, Data=8-bit, Non-parity and Stop=1.
- Vivado tool for programming FPGA, installed on PC



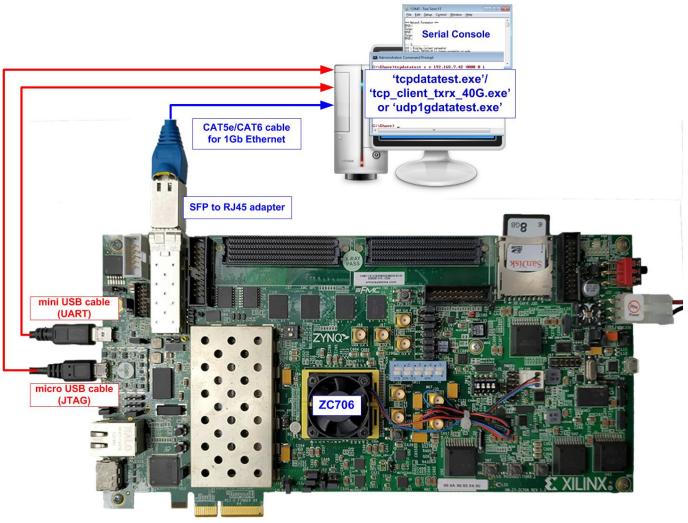
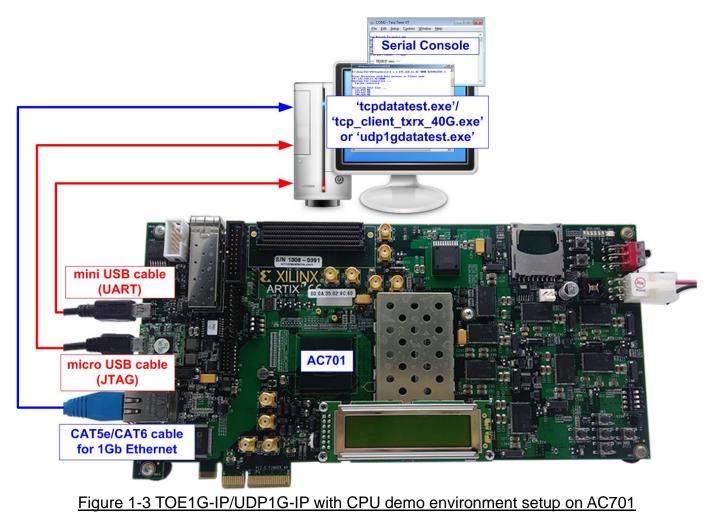


Figure 1-1 TOE1G-IP/UDP1G-IP with CPU demo (FPGA <-> PC) on ZC706



dg_toeudp1gip_fpgasetup_xilinx.doc Ele Edit Setup Control Window Help Serial Console 'tcpdatatest.exe'/ 'tcp_client_txrx_40G.exe'
 or 'udp1gdatatest.exe' C € XILINX. mini USB cable 🙆 #FMC KINTEX (UART) C C 00:0A 35:02:78.64 micro USB cable (JTAG) KC705 0 CAT5e/CAT6 cable for 1Gb Ethernet S/N 1230-2352 Figure 1-2 TOE1G-IP/ UDP1G-IP with CPU demo (FPGA <-> PC) on KC705







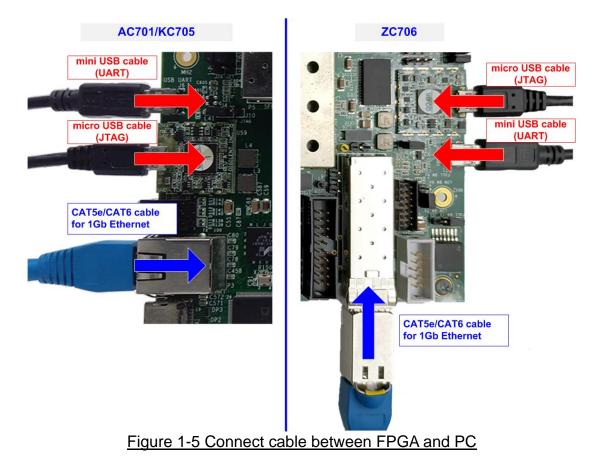
The step to setup test environment by using FPGA and PC is described in more details as follows.

- 1) Power off system.
- 2) Connect micro USB cable and mini USB cable from FPGA board to PC for JTAG programming and USB UART (Serial Console).
- 3) Connect power supply to FPGA development board.
- 4) For ZC706, connect SFP to RJ45 adapter into SFP+ connector on ZC706 board.



Figure 1-4 Connect SFP to RJ45 adapter to ZC706

5) Connect CAT5e or CAT6 cable between RJ45 on FPGA board to PC



- 6) Power on FPGA board.
- 7) Open Serial console to connect to FPGA board. Serial setting is Baud rate = 115,200, Data=8-bit, Non-parity, and Stop = 1.



- 8) Download and program configuration file and firmware to FPGA board.
 - a) For ZC706 board, open Vivado TCL shell and change current directory to download folder which includes demo configuration file. Type "xxx1gcputest_zc706.bat", as shown in Figure 1-6.

Vivado 2017.4 Tcl Shell - E:\Program\Xilinx\Vivado\2017.4\bin\vivado.bat -mode tcl —	>	<
		^
Vivado% cd D:/Temp/download		
Vivado% udp1gcputest_zc706.bat_		
		¥
Figure 1-6 Example command script for download to ZC706 by Vivado to	ol	

b) For AC701/KC705 board, configure FPGA by using Vivado, as shown in Figure 1-7.

Vivado 2017.4	HARDWARE MANAGER - unconnected
Eile Flow Iools Window Help Q- Quick Access	Open target No hardware target is open. Open target
HLx Editions	Hardware Auto Connect
Quick Start Create Project > Open Project >	Open New Target HARDWARE M AGER - localhost/xilinx_tcf/Digile d. Click Program device There are no debug cores. Program device Refresh device
Open Example Project >	Hardware ? _ □ ⊡ × Q, ★ ♦ Ø ▶ ≫ ■ ✿
Tasks Manage IP > a. Click Open Hardware Manager	Name Status ✓ Il localhost (1) Con
Open Hardware Manager > Xilinx Tcl Store >	xc7k325t_0 (1) Programmed XADC (System Monitor)
🍌 Program Device	×
	e and download it to your hardware device. You es file that corresponds to the debug cores ming file. e. Click "" to select Programming file (TOE1GCPUTest.bit/UDP1GCPUTest.bit)
Bitstream file: D:/Temp/T	OE1GCPUTest.bit 🛞
Debu <u>a</u> probes file:	
Enable end of startup check	x
3	Program Cancel
	f. Click Program button to start FPGA programming
Figure 1-7 Program	FPGA by Vivado for AC701/KC705

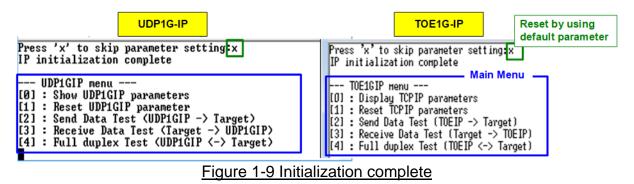


- 9) On serial console, welcome message is displayed.
 - a. Input '0' to initialize TOE1G-IP/UDP1G-IP in client mode (ask PC MAC address by sending ARP request).
 - b. Default parameter in client mode is displayed on the console.

UDP1G-IP	TOE1G-IP	
UDP1GIP with CPU Demo [Ver = 1.6] Input mode : [0] Client [1] Server => 0	TOE1GIP with CPU Demo [IPVer = 2. Input mode : [O] Client [1] Server =)	Input '0' to initialize ,25 in client mode ♪┃
Default UDP1GIP Parameter Mode = CLIENT FPGA MAC address = 0x000102030405 FPGA IP = 192.168.11.42 Target IP = 192.168.11.25 FPGA port number = 4000 Target port number (Target->FPGA) = 61000	Target IP = 192.168.11.25 FPGA IP = 192.168.11.42	Default client parameters, displayed on boot-up screen
Target port number (Target / Target) = 60000 Press 'x' to skip parameter setting:	Target port number = 60001 FPGA port number = 60000 Press 'x' to skip parameter setting:	

Figure 1-8 Message after system boot-up

c. User enters 'x' to skip parameter setting for using default parameters to begin system initialization, as shown in Figure 1-9. If user enters other keys, the menu for changing parameter is displayed, similar to "Reset TCPIP/UDPIP parameters" menu. The example when running the main menu is described in "dg_toe1gip_cpu_instruction" or "dg_udp1gip_cpu_instruction document.



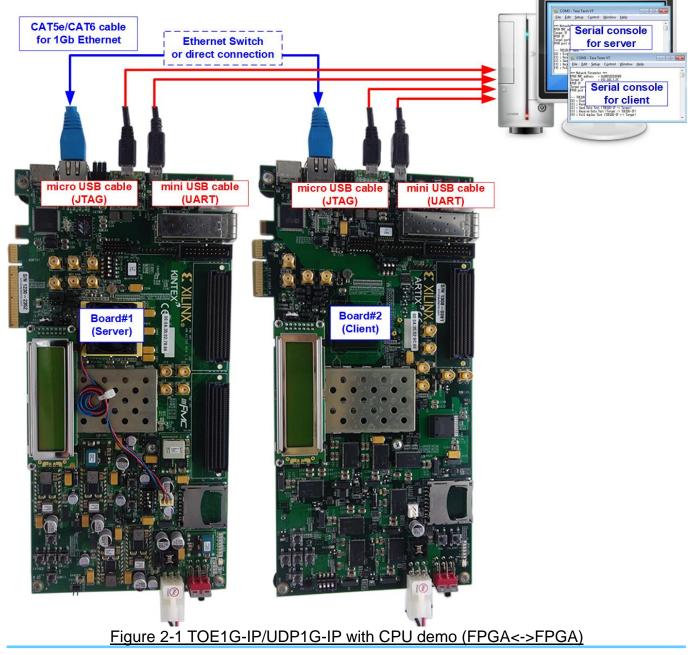
<u>Note</u>: Transfer performance in the demo depends on Test PC resource in Test platform.



2 Test environment setup when using two FPGAs

Before running the test, please prepare following test environment.

- Two FPGA development boards which are the same board or the different board, ZC706/KC705/AC701
- Cat5e or Cat6 cable for 1 Gb Ethernet connection between two FPGA boards (Ethernet connection between two FPGA boards could be connected directly or connected through other network devices such as Ethernet switch) *Note: When using ZC706, insert SFP to RJ45 adapter to SFP+ connector on FPGA board.*
- Connect micro USB cable and mini USB cable for programming FPGA and Serial console between each FPGA board and PC (two sets are used for two FPGA boards)
- Serial console software such as TeraTerm, installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming FPGA, installed on PC





The step to setup test environment by using two FPGAs is described in more details as follows.

Follow step 1) - 8) of topic 1 (Test environment setup when using FPGA and PC) to prepare FPGA board for running the demo. After two FPGA boards have been configured completely, Serial console displays the menu to select client mode or server mode. The step after FPGA configuration is described as follows.

- 1) Open Serial console for board#1 and board#2 which are initialized as Server and Client respectively.
 - a. Set '1' on Serial console of FPGA board#1 for running server mode.
 - b. Set '0' on Serial console of FPGA board#2 for running client mode.
 - c. Default parameters for server or client are displayed on the console, as shown in Figure 2-2.

COM10 - Tera Term	r _ UDP1G	-IP COM26	- Tera Term V	Client	_	
<u>File Edit Setup Control</u> Set mod	le for FPGA board#1 o [Ver = 1.6]	UDP1G	Setup Control	mode for Demo [Ve	select client FPGA board#	
Input mode : [0] Client [1] Server => 1 Default UDP1GIP Parameter Mode = SERVER PPGA MAC address = 0x001122334455 PPGA IP = 192.168.11.25 FPGA IP = 192.168.11.42 PPGA port number = 60000 Carget port number (Target->FPGA) = 4000 Carget port number (FPGA->Target) = 60000 c Press 'x' to skip parameter setting:						
	efault parameters for er mode is displayed			•	t parameters f de is displaye	
	n. Set '1' to select server mode for FPGA board#1 Demo [IPVer = 2.25(a)-	<u>File Edit S</u>	Tera Term VT etup C <u>o</u> ntrol P with CPU A : [0] Clier	mode for Fi	$- \Box$ select client PGA board#2 $er = 2.25$ $bruer = 20$]
Default TOE1GIP Parama Window Update Gap = (Mode = S FPGA MAC address = (Target IP = 3	eter SERUER 3×001122334455 192.168.11.42 192.168.11.25 \$0000	- Default TO Window Upd Mode FPGA MAC a Target IP FPGA IP Target por FPGA port	EIGIP Paramo ate Gap = ddress = = : = : = : t number = !	eter 0 CLIENT 0×00010203 192.168.13 192.168.13 60001 60000	30405 L.25 L.42 C	
	It parameters for node is displayed Figure 2-2	2 Input mo	client mode	arameters fo is displayed		



2) Input 'x' to use default parameters or other keys to change parameters. The parameters of server mode must be set before client mode.

When running TOE1G-IP,

- a. Set parameters on server Serial console.
- b. Set parameters on client Serial console to start IP initialization by transferring ARP packet.
- c. After finishing initialization process. "IP initialization complete" and main menu are displayed on server console and client console.

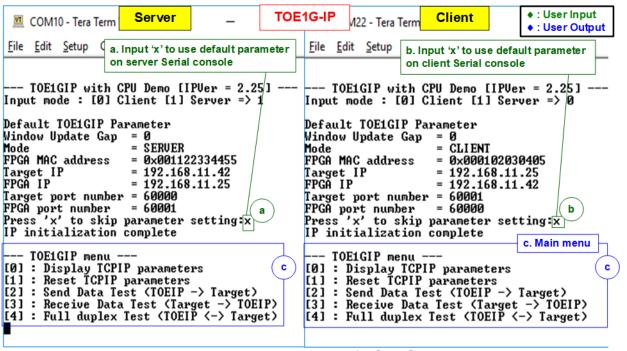


Figure 2-3 Main menu of TOE1G-IP



When running UDP1G-IP,

- a. For server mode, if user does not change default parameters, input 'x' to skip parameter setting.
- b. For client mode, user must change target port number (Target->FPGA) to use same value as target port number (FPGA->Target).
- c. After finishing initialization process. "IP initialization complete" and main menu are displayed on server console and client console.

💆 COM10 - Tera Term VT Server		P1G-IP	6 - Tera Term VT	Client		: User Input : User Output
COM10-Tera Term VT Server - UDI <u>File Edit Setup Control Window H</u> <u>File Edit Setup Control Window H</u> <u>Default parameters</u> <u>for server mode</u> <u>Input mode : [0] Client [1] Server => 1</u> <u>Default UDP1GIP Parameter</u> <u>Mode = SERVER</u> <u>FPGA MAC address = 0x001122334455</u> <u>FPGA MAC address = 0x0011223344555</u> <u>FPGA IP = 192.168.11.25</u> <u>Target IP = 192.168.11.42</u> <u>FPGA port number (Target->FPGA) = 4000</u> <u>Target port number (FPGA->Target) = 4000</u> <u>Target port number (FPGA->Target) = 4000</u> <u>Press 'x' to skip parameter setting:</u> <u>Use default parameter</u>		<u>File Edit</u> <u>Default</u> <u>Mode</u> <u>PFGA MAC</u> <u>PFGA PD</u> <u>Target 1</u> <u>Target 1</u> <u>Target 1</u> <u>Input m</u> <u>Invalid</u> Input FI Invalid Input FI Invalid	<u>Setup Control Window</u> LGIP with CPU Demo [1 ode : [0] Client [1] UDP1GIP Parameter = CLIENT C address = 0x0001021 = 192.168.	<u>Help</u> Ver = 1.6] - Server => 0 030405 11.42 11.25 >FPGA> = 610 arget> = 600 setting[y] Server =>[pt change pt change	Defaul for clie 190 190 Input t	t parameters ent mode o set parameter ue to use old value
	Figure 2-4	Invalid Input Fi Invalid Input Ta Invalid UDP1GIP Mode FPGA MAG FPGA MAG FPGA IP Target I Target I Target MARNING	input : Parameter n PGA port number : n input : Parameter n arget port number (Ta arget port number (F input : Parameter n Parameter = CLIENT C address = 0×0001021 = 192.168.	ot change arget->FPGA) PGA->Target) ot change 030405 11.42 11.25 >FPGA) = 600 IP setting	Alue for both T . : 60000 . : n New p for clie	arameters ent mode er on Test app



3 Revision History

Revision	Date	Description		
1.0	2-Nov-18	Initial version release		
2.0	31-Jul-20	Remove test result on the console		
3.0	10-Nov-20	TOE1G-IP and UDP1G-IP		