

UDP1G-IP Demo Instruction

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UDP1G-IP Demo Instruction

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1 Overview

This document shows the example to run UDP1G-IP demo by using two test environments. First is run by using one FPGA board transferring UDP data with TestPC which runs test application for transferring UDP data via 1Gb Ethernet. Test performance and data loss rate on the first environment is limited by the resource on TestPC. Second is run by using two FPGA boards for transferring 1Gb Ethernet data together. The second environment achieves the best performance for transferring UDP data via 1Gb Ethernet by using UDP1G-IP and data is not lost when the hardware signal is in good quality.

In the document, topic 2 shows the example to set up 1Gb Ethernet card on TestPC to get the good performance for transferring data via 1Gb Ethernet when running the test by using the first test environment, FPGA and Test PC. Topic 3 shows the example console and test result when running under the first test environment. Finally, topic 4 shows the example console when running the second test environment, FPGA and FPGA. More details of each topic are described as follows.



2 PC Setup

Before running the demo, please check the network setting on PC. The example for setting the network is shown as follows.

2.1 IP Setting

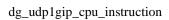
Network and Sharing Center			
🔶 🐳 🛧 🛉 🙀 🔶 Control Pa	nel > Network and Internet > Netwo	ork and Sharing Center 🗸 🗸 Search	۱C
Control Panel Home	View your basic network information and set up connections		
Change adapter settings	View your active networks		
Change advanced sharing settings	Network Public network	Access type: Internet 2 Connections: <u>Ethernet</u>	
	Change your networking settings – Figure 2-1 IPv4 se	etting	

- 1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
- 2) Click Gigabit Ethernet icon which is used to connect with FPGA board.

Ethernet Status	× Ethernet Properties	
eneral	Networking	
Connection	Connect using: 1-Gb LAN connect	ion
IPv4 Connectivity: No Internet a	ccess Intel(R) Ethemet Connection (7) I219-V	
IPv6 Connectivity: No network a	Config	
Media State: En	abled	ure
Duration: 01:	56:55 This connection uses the following items:	
Speed: 1.0	Gbps	
	File and Printer Sharing for Microsoft Networks	
Details	QoS Packet Scheduler 4	
	Internet Protocol Version 4 (TCP/IPv4)	
	Microsoft Network Adapter Multiplexor Protocol	
uctivity		
		>
Sent — Rec	eived 5	-
	Install Uninstall Proper	ties
Bytes: 39,299,554 503,07	3,087 Description	
3	Transmission Control Protocol/Internet Protocol. The def	fault
Properties Diagnose	wide area network protocol that provides communication	1
Ulable Diagrose	across diverse interconnected networks.	
	Close	
		Cance

Figure 2-2 Select IP address setting menu

- 3) Click Properties button in Ethernet Status window.
- 4) Select "TCP/IPv4".
- 5) Click Properties button in Ethernet Properties window.





Internet Protocol Version 4 (TCP/IPv4)	Properties X				
General					
You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings.					
Obtain an IP address automatically					
• Use the following IP address:	(6a)				
IP address:	192 . 168 . 11 . 25				
Subnet mask:	255.255.255.0				
Default gateway:					
Obtain DNS server address autom	atically				
• Use the following DNS server addr	resses:				
Preferred DNS server:					
Alternate DNS server:					
Validate settings upon exit	Advanced				
	6b OK Cancel				
Figure 2-3 Setting I	P address for PC				

6) Set IP address = 192.168.11.25 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.



2.2 Speed and Frame Setting

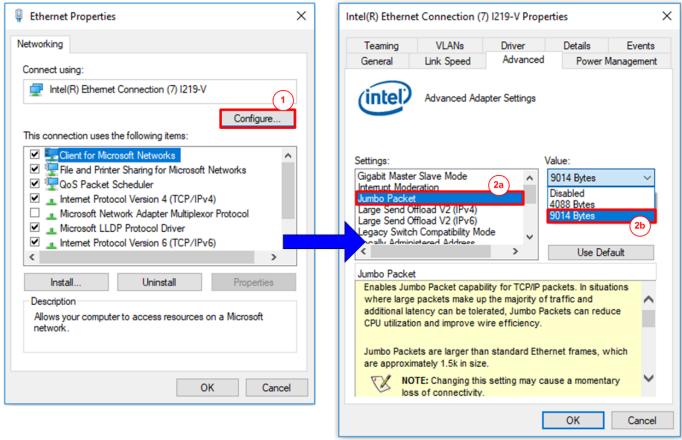


Figure 2-4 Jumbo frame setting

- 1) Click Configure button in Ethernet Properties window.
- 2) On Advanced Tab, select "Jumbo Packet" and then set Value to "9014 Bytes" for Jumbo Frame support.



3) On Link Speed, select "1 Gbps Full Duplex" and click OK button, as shown in Figure 2-5.

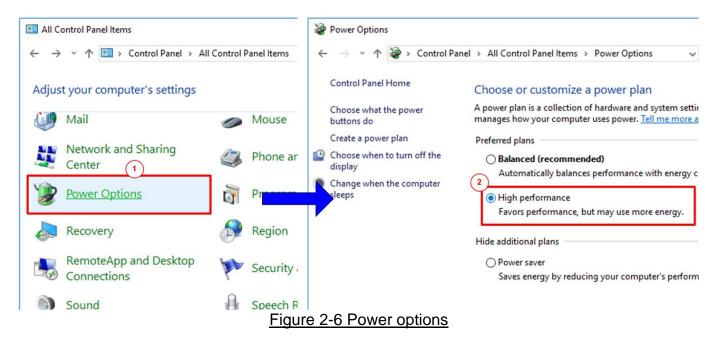
Teaming	VLANs	Driver	Details	Events
General	Link Speed	Advanced	Power M	lanagement
(intol)	Link Speed and	d Duplex Settings	5	
line	Intel(R) PROSe	t Version: 23.2.0	1006	
Link Status				
Speed:	1.00 Gbp	s Full Duplex (EE	E: Active)	
Speed and Du	plex:			
1.0 Gbps Full		~	Diagnostic	s
Auto Negotiati	and the second	_		
10 Mbps Half	Duplex		Identify Ada	ator
10 Mbps Full [100 Mbps Hai			identity Add	
100 Mbps Full	Duplex			
1.0 Gbps Full		default, Inte		
		t, you can set the		
	natch those of the			
settings to n				
Settings to n				
	nation icon			
	mation icon			
Inform		the device is not	linked at its	
Inform	displayed when t	the device is not hat case, if your		to

Figure 2-5 Set link speed = 1 Gbps



2.3 Power Option Setting

- 1) Open Control Panel and select Power Options, as shown in the left window of Figure 2-6.
- 2) Set High Performance plan, as shown in the right window of Figure 2-6.





2.4 Firewall Setting

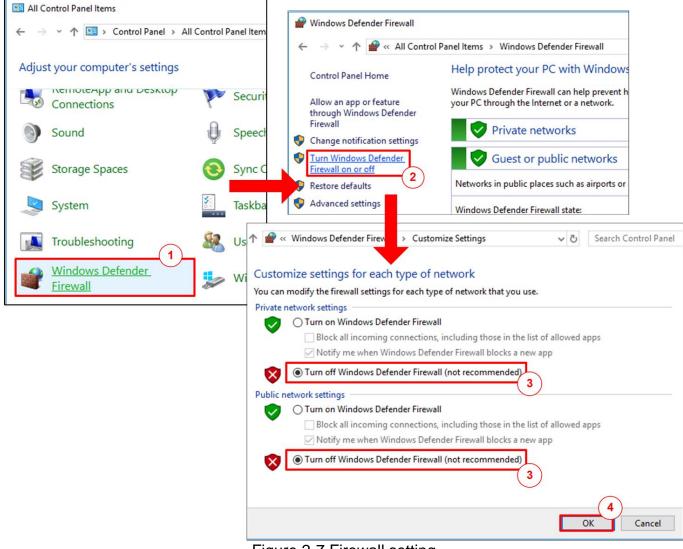


Figure 2-7 Firewall setting

- 1) Open Control Panel and select Windows Firewall.
- 2) Click "Turn Windows Firewall on or off".
- 3) Select Turn off Firewall under Private and Public network settings.
- 4) Click OK button to confirm the setting.



3 Test result when using FPGA and TestPC

3.1 Display UDPIP parameters

Select '0' to check current parameter in the demo. There are seven parameters displayed on the console.

+++ Current Network Parameter +++ Mode = CLIENT				
FPGA MAC address = 0x000102030405 FPGA IP = 192.168.11.42 FPGA port number = 4000	Curre parame			
Target IP = 192.168.11.25 Target port number (Target-)FPGA) = 6 Target port number (FPGA-)Target) = 6				
UDP1GIP menu [0] : Display UDPIP parameters [1] : Reset UDPIP parameter [2] : Send Data Test (UDPIP -> Target) [3] : Receive Data Test (Target -> UDPIP) [4] : Full duplex Test (UDPIP <-> Target)				

Figure 3-1 Display current parameter result

- 1) Mode : Mode of UDP1G-IP to run as server or client. To run with PC, please input '0' to initialize as client mode.
- 2) FPGA MAC address : 48-bit hex value to be MAC address of FPGA. Default value is 0x000102030405.
- 3) FPGA IP : IP address of FPGA. Default value is 192.168.11.42. Note: This value is used to be FPGA IP address, parameter for test application on PC.
- 4) Target IP : IP address of destination device (1 Gb Ethernet on PC). Default value is 192.168.11.25.
- 5) FPGA port number: Port number of FPGA. Default value is 4000. <u>Note</u>: This value is used to be FPGA port, parameter for test application on PC.
- 6) Target port number (Target->FPGA) : Port number of the destination device to send data to FPGA. Default value is 61000.
 <u>Note</u>: This value is used to be PC port, parameter for test application on PC in transmit mode.
- 7) Target port number (FPGA->Target) : Port number of the destination device to receive data from FPGA. Default value is 60000. <u>Note</u>: This value is used to be PC port, parameter for test application on PC in received mode.

To change some parameters, user can set by using menu [1] (Reset UDPIP parameter).



3.2 Reset UDPIP parameters

Select '1' to reset the IP and change IP parameters.

This menu is used to change IP parameters or send reset to UDP1G-IP. After user selects this menu, the current parameters are displayed on the console. User inputs 'x' to use the same parameters or other keys to change some parameters. After the parameters are set, reset signal is sent to UDP1G-IP.

There are seven parameters to set in this menu. Each parameter is verified by CPU. The parameter is updated to UDP1G-IP when the input is valid. If the input is not valid, the parameter does not change. After user inputs all parameters, IP is reset. The description of each parameter is shown in topic 3.1 (Display) and the range of each parameter is described as follows.

- 1) Mode : '0' to initialize the IP as client mode.
- 2) FPGA MAC address : 12-digit of hex value. Add "0x" to be prefix to input as hex value.
- 3) FPGA IP address : A set of four decimal digits is separated by ".". The valid range of each decimal digit is 0-255.
- 4) FPGA port number : Valid range is 0-65535.
- 5) Target IP address : A set of four decimal digits, similar to FPGA IP address. This value is IP address of Test PC.
- 6) Target port number (Target->FPGA)
- : Valid range is 0-65535.
- 7) Target port number (FPGA->Target)
- : Valid range is 0-65535.

After finishing all parameter assignment, new parameters are displayed on the console. Next, reset signal is sent to the IP for loading new parameters. Finally, "IP initialization complete" is shown after IP completes initialization process, as shown in Figure 3-2.



User Input +++ Reset UDPIP +++ User Output Current parameter before changing +++ Current Network Parameter +++ = CLIENT Mode FPGA MAC address FPGA IP = 0x000102030405 = 192.168.11.42 = 4000 FPGA port number FrGH port number - 1000 Target IP = 192.168.11.25 Target port number (Target->FPGA) = 61000 Target port number (FPGA->Target) = 60000 Press 'x' to skip parameter setting: Input mode : [0] Client [1] Server => n Invalid input : Parameter not change Input FPGA MAC address : n Invalid input : Parameter not change Input other keys (not 'x') to set parameter Input invalid value Invalid input : Parameter not change Input FPGA IP address : n to use same value Invalid input : Parameter not change Input FPGA port number : 50000 Input Target IP address : n Invalid input : Parameter not change Input Target port number (Target->FPGA) Input valid value to change parameter : n Invalid input : Parameter not change Input Target port number (FPGA->Target) Invalid input : Parameter not change : n +++ Current Network Parameter +++ = CLIENT Mode FPGA MAC address FPGA IP = 0x000102030405 = 192.168.11.42 New parameter = 50000 = 192.168.11.25 FPGA port number Target IP Target IP = 192.168.11.25 Target port number (Target->FPGA) = 61000 Target port number (FPGA->Target) = 60000 WARNING: Please also change IP setting and port number on Test appli IP initialization complete Reset complete -- UDP1GIP menu [0] : Display UDPIP parameters [1] : Reset UDPIP parameter Send Data Test (UDPIP -> Target) [2]: [3] : Receive Data Test (Target -> UDPIP) [4] : Full duplex Test (UDPIP <-> Target)

Figure 3-2 Change IP parameter result



3.3 Send Data Test

To transfer data from FPGA to PC, select '2' to run send data test on FPGA and prepare "udpdatatest.exe" on PC to receive data. User sets test parameters on FPGA for sending data through the console. On PC, user sets test parameters of "udpdatatest.exe" to receive data through Command prompt. The step to run the test is described as follows.

- 1) On FPGA console, set two parameters under send data test menu.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
 - b) Input packet size: Unit of packet size is byte. Valid value is 1 8972. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.

<u>Note</u>: When packet size is more than 1472, the packet output from UDP1G-IP is jumbo frame size. In this case, Test PC must support jumbo frame.

- 2) If all inputs are valid, the recommended parameters to run test application on PC are displayed. After that, "Press any key to start data sending ..." is displayed to begin data sending when user enters some keys.
- 3) On Command prompt, user runs the application by using the recommended parameters. There are five parameters for "udpdatatest".

>> udpdatatest [Dir] [FPGAIP] [FPGAPort] [PCPort] [ByteLen] <Pattern> <Timeout>

- a) Dir : Set 'r' to receive test data from FPGA
- b) FPGA IP : Set the same value as FPGA IP address
- c) FPGA port : Set the same value as FPGA port number
- d) PC port : Set the same value as target port number (FPGA->Target)
- e) ByteLen : Set the same value as "Input transfer size" of step 1a)
- f) Pattern : '1'- enable data verification, '0'-disable data verification. Default value is '1'.
- g) Timeout : Timeout in msec unit. Valid value is 100-65536.

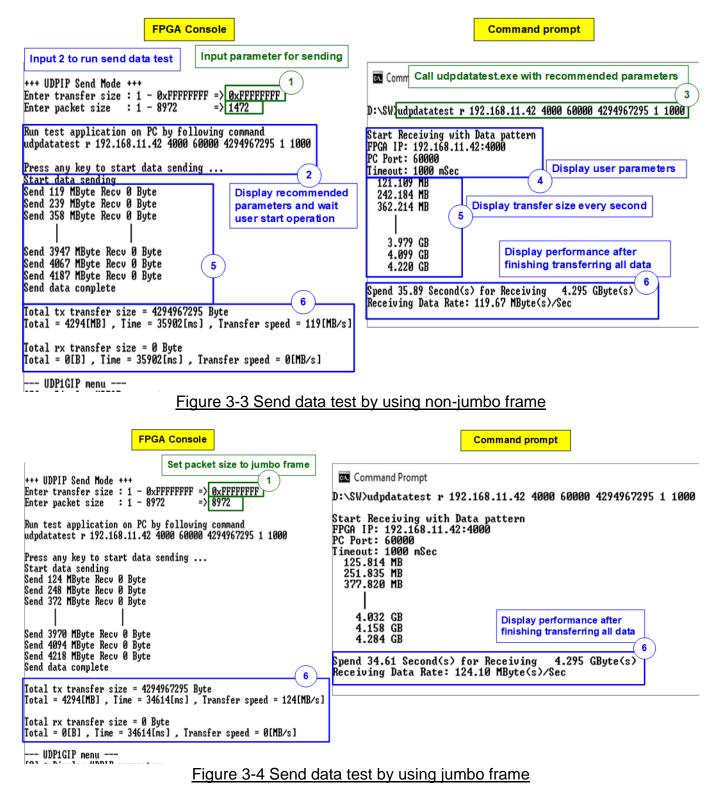
It is recommended to set to 1000 (1 sec). Default value is 100.

- 4) After running test application, the summary of setting parameter is displayed. After that, PC waits received data from FPGA.
- 5) On FPGA console, user enters any key(s) to start sending data. During transferring data, current transfer size is displayed on FPGA console (transmit size) and Command prompt (receive size) every second.
- 6) "Send data complete" is displayed on FPGA console after all data are sent. On PC, test application is finished by one of two conditions. First, total data have been received (no lost data is found within networking). Second is timeout condition when no additional data is received more than 1 second. After timeout is found, timeout message with the 1st error position is displayed. Finally, total transfer size and performance are displayed on FPGA console (transmit performance) and Command prompt (receive performance).



Figure 3-3 shows the example of send data test when using non-jumbo frame size. The left window is FPGA console while the right window is Command prompt on PC.

Figure 3-4 shows the example of send data test when using jumbo frame size. Performance when running jumbo frame is better than non-jumbo frame.





When some inputs are invalid, "Out-of-range input" is displayed. After that, the operation is cancelled, as shown in Figure 3-5 - Figure 3-6.

> +++ UDPIP Send Mode +++ Enter transfer size : 1 - 0xFFFFFFFF => 0x10000000 Out-of-range input Error transfer size - UDP1GIP menu ---- UDP1GIP menu ---[0] : Display UDPIP parameters [1] : Reset UDPIP parameter [2] : Send Data Test (UDPIP -> Target) [3] : Receive Data Test (Target -> UDPIP) [4] : Full duplex Test (UDPIP <-> Target) Figure 3-5 Error from invalid transfer size +++ UDPIP Send Mode +++ Enter transfer size : 1 - ØxFFFFFFF => ØxFFFFFFFF Enter packet size : 1 - 8972 => 8973 Enter packet size Out-of-range input Error packet size - UDP1GIP menu --- UDFIGIP menu --[0] : Display UDPIP parameters
> [1] : Reset UDPIP parameter
> [2] : Send Data Test (UDPIP -> Target)
> [3] : Receive Data Test (Target -> UDPIP)
> [4] : Full duplex Test (UDPIP <-> Target)

Figure 3-6 Error from invalid packet size



3.4 Receive Data Test

To transfer data from PC to FPGA, select '3' to run receive data test on FPGA and prepare "udpdatatest.exe" on PC to send data. User sets test parameters on FPGA for receiving data through FPGA console. On PC, user sets parameters of "udpdatatest.exe" to send data through Command prompt. The step to run the test is shown as follows.

- 1) On FPGA console, set two parameters under send data test menu.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
 - b) Input data verification mode: '0'-disable data verification, '1'-enable data verification sent from PC.
- 2) If all inputs are valid, the recommended parameters to run test application on PC are displayed. After that, "Wait data from Target ..." is displayed on the console when IP is ready to receive data from PC.
- 3) On Command prompt, user runs the application by using the recommended parameters. There are five parameters for "udpdatatest".
 - >> udpdatatest [Dir] [FPGAIP] [FPGAPort] [PCPort] [Bytelen]
 - a) Dir : Set 't' to send test data from FPGA
 - b) FPGA IP : Set the same value as FPGA IP address
 - c) FPGA port : Set the same value as FPGA port number
 - d) PC port : Set the same value as target port number (Target->FPGA)
 - e) Bytelen : Set the same value as "Input transfer size" of step 1a)
- 4) After running test application, test application starts sending data out to FPGA. During transferring data between FPGA and PC, current transfer size is displayed on both FPGA console (receive size) and Command prompt (transmit size) every second.
- 5) "Receive data complete" is displayed on FPGA console after FPGA receives all data or 1-second timeout is found. Finally, total transfer size and performance are displayed on FPGA console (receive performance) and Command prompt (transmit performance).



Figure 3-7 shows the example of receive data test when disabling data verification mode on FPGA. The left window is test result on FPGA console while the right window is test result on Command prompt.

Figure 3-8 shows the example of receive data test when enabling data verification mode on FPGA. While PC sends incremental data to FPGA. When verification module is failed, error message is displayed.

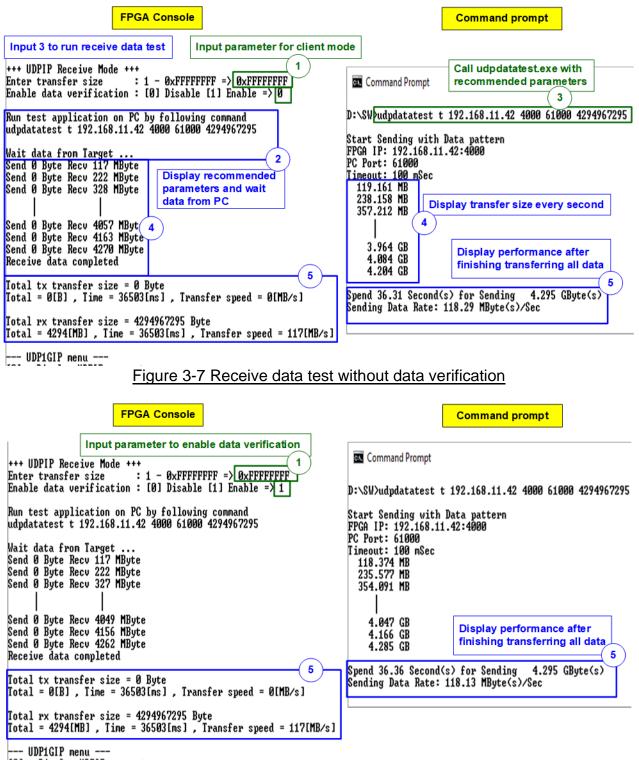


Figure 3-8 Receive data test with enable data verification



3.5 Full duplex Test

Select '4' to run full duplex test to transfer data between FPGA and PC in both directions at the same time. User sets test parameters on FPGA console. On PC, user opens two applications on two command prompts for sending and receiving data with FPGA by using different port number. The step to run the test is described as follows.

- 1) On FPGA console, set three parameters under full duplex test.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal unit.
 - b) Input packet size: Unit of packet size is byte. Valid value is 1 8972. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal unit.
 - c) Input data verification mode: '0'-disable data verification, '1'-enable data verification.

2) When all inputs are valid, the recommended parameters for two applications are displayed, sending data test and receiving data test. Next, "Press any key to start data sending ..." is displayed to wait until user starts IP sending data.

3) On PC, open two Command prompts to run the test applications by using the recommended parameters.

Seven parameters are applied for the 1st Command prompt (receiving data). >> udpdatatest [Dir] [FPGAIP] [FPGAPort] [PCPort] [ByteLen] <Pattern> <Timeout>

Five parameters are applied for the 2nd Command prompt (sending data). >> udpdatatest [Dir] [FPGAIP] [FPGAPort] [PCPort] [ByteLen]

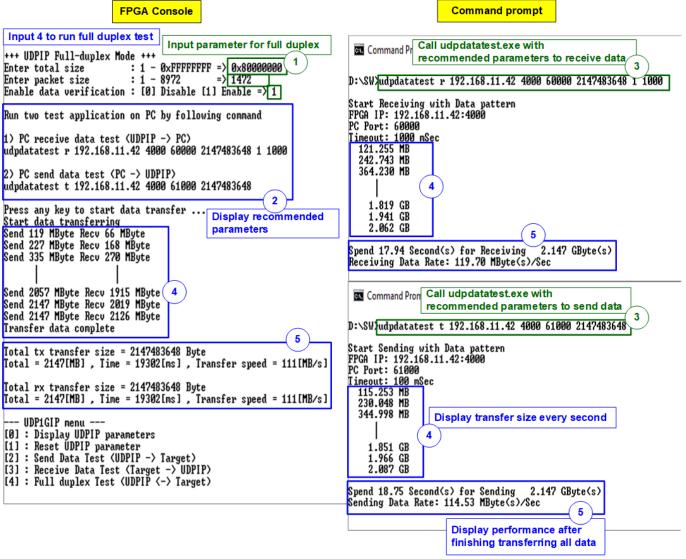
- a) Dir : Set 'r' to the 1st command prompt
 - Set 't' to the 2nd command prompt
- b) FPGA IP : Set the same value as FPGA IP address
- c) FPGA port : Set the same value as FPGA port number
- d) PC port : Set the same value as target port number (FPGA->Target) for the 1st command prompt. Set the same value as target port number (Target->FPGA) for the 2nd command prompt.
- e) Bytelen : Set the same value as "Input transfer size" of step 1a)
- f) Pattern : '1'- enable data verification, '0'-disable data verification. Default value is '1'.
- g) Timeout : Timeout in msec unit. Valid value is 100-65536.

It is recommended to set to 1000 (1 sec). Default value is 100.

- 4) On FPGA console, press any key(s) to start sending data to PC. After that, current transfer size in both directions is displayed on FPGA console and two command prompts every second.
- 5) "Transfer data complete" is displayed on FPGA console after UDP1G-IP finishes sending and receiving all data. Finally, total transfer size and performance are displayed on FPGA console and Command prompt.



As shown in Figure 3-9, transfer performance when running full duplex with data verification is displayed. The left window is the test result on FPGA console while the right window is the test result on Command prompt (the upper window is receive performance and the lower window is transmit performance).







4 Test result when using two FPGAs

4.1 Display UDPIP parameters

Select '0' to check current parameter in the demo. There are seven parameters displayed on the console.

	Current parameters on server	Current parameters on client
Mode FPGA M FPGA I FPGA po Target Target	rrent Network Parameter +++ = SERVER AC address = 0×001122334455 P = 192.168.11.25 ort number = 60000 IP = 192.168.11.42 port number (Target->FPGA) = 4000 port number (FPGA->Target) = 4000	+++ Current Network Parameter +++ Mode = CLIENT FPGA MAC address = 0x000102030405 FPGA IP = 192.168.11.42 FPGA port number = 4000 Farget IP = 192.168.11.25 Farget port number (Target-)FPGA) = 60000 Farget port number (FPGA-)Target) = 60000
[0] :] [1] :] [2] :] [3] :]	P1GIP menu Display UDPIP parameters Reset UDPIP parameter Send Data Test (UDPIP -> Target) Receive Data Test (Target -> UDPIP) Full duplex Test (UDPIP <-> Target)	UDP1GIP menu [0] : Display UDPIP parameters [1] : Reset UDPIP parameter [2] : Send Data Test (UDPIP -> Target) [3] : Receive Data Test (Target -> UDPIP) [4] : Full duplex Test (UDPIP <-> Target)

Figure 4-1 Display current parameter result

1) Mode

: Mode of UDP1G-IP to run as server or client.

'0'- Client, '1'- Server

- 2) FPGA MAC address : 48-bit hex value to be MAC address of FPGA. Default value is 0x000102030405 (client mode) or 0x001122334455 (server mode).
- 3) FPGA IP : IP address of FPGA. Default value is 192.168.11.42 (client mode) or 192.168.11.25 (server mode).
- 4) FPGA port number : Port number of FPGA. Default value is 4000 (client mode) or 60000 (server mode).
- 5) Target IP : IP address of destination device. Default value is 192.168.11.25 (client mode) or 192.168.11.42 (server mode).
- 6) Target port number (Target->FPGA) : Port number of the destination device to send data to UDP1G-IP. Default value is 60001 (client mode) or 4000 (server mode).

In client mode, this value must be changed from 60001 to 60000 (the same value as default value of Target port number for FPGA -> Target).

7) Target port number (FPGA->Target) : Port number of the destination device to receive data from UDP1G-IP. Default value is 60000 (client mode) or 4000 (server mode).

To change some parameters, user can use menu [1] (Reset UDPIP parameter).



4.2 Reset UDPIP parameter

Select '1' to reset the IP and change IP parameters.

This menu is applied for changing IP parameters or sending reset to UDP1G-IP. After user selects this menu, the current parameters are displayed on the console. User enters 'x' to use the same parameters while other keys are entered for changing some parameters. After the parameters are set, reset signal is sent to UDP1G-IP.

There are seven parameters which can be modified by user. When user enters invalid value such as 'n', the parameter does not change. After setting parameters completely, IP is reset. The description of each parameter is shown in topic 4.1 (Display UDPIP parameters) and the range of each parameter is described as follows.

<u>Note:</u>

- 1. When user desires to reset parameters on server, the client FPGA must be also reset. Server must be reset firstly to wait until ARP request sent by client.
- 2. Target port number for sending and receiving data must be similar.
- 3. Parameter of client and server must be similar, i.e.
 - a. Target IP of server = FPGA IP of client
 - b. FPGA IP of server = Target IP of client
 - c. Target port number of server (both Tx and Rx direction) = FPGA port number of client
 - d. FPGA port number of server = Target port number of client (both Tx and Rx direction)

1) Mode : '0'- Client, '1'- Server.

<u>Note</u>: Two FPGA boards must run in different mode (one is client and another is server).

- 2) FPGA MAC address : 12-digit of hex value. Add "0x" as a prefix for hex input.
- 3) FPGA IP address : A set of four decimal digits is separated by ".". The valid range of decimal digit is 0-255.
- 4) FPGA port number : Valid range is 0-65535.
- 5) Target IP address : A set of four decimals, similar to FPGA IP address.
- 6) Target port number (Target->FPGA) : Valid range is 0-65535.
- 7) Target port number (FPGA->Target) : Valid range is 0-65535.

After finishing all parameter assignment, new parameters are displayed on FPGA console. Next, reset signal is sent to the IP to load new parameters. Finally, "IP initialization complete" is shown after IP completes initialization process, as shown in Figure 4-2.



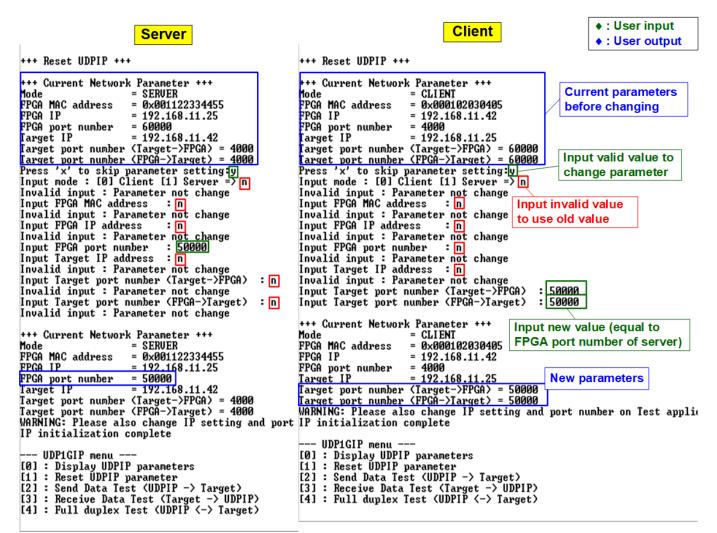


Figure 4-2 Change IP parameter result



4.3 Send and Receive data Test (Half-duplex test)

The operation to send and receive data test of server and client mode is similar. So, this topic describes the menu to transfer data between two FPGA boards. The first board runs receive data test (select menu '3') and the second board runs send data test (select menu '2').

User sets test parameters through FPGA console. The step to run the test is described as follows.

- 1) On FPGA console under menu 3 (receive data test), set two parameters.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
- b) Input data verification mode: '0'-disable data verification, '1'-enable data verification.
- 2) When all inputs are valid, "Wait data from Target ..." is displayed.
- 3) On FPGA console under menu 2 (send data test), set two parameters.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input. This value must be equal to transfer size under receive data test.
 - b) Input packet size: Unit of packet size is byte. Valid value is 1 8972. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.

<u>Note</u>: When packet size is more than 1472, the packet output from UDP1G-IP is jumbo frame. User needs to confirm that network device supports jumbo frame when two FPGA boards connect through the network device.

- 4) If all inputs are valid, "Press any key to start data sending ..." is displayed. User enters some key(s) to start sending data.
- 5) During transferring data, current transfer size is displayed on both FPGA consoles every second.
- 6) "Send data complete" or "Receive data completed" are displayed on FPGA console after finishing transferring all data. Finally, total transfer size and performance are displayed on both FPGA consoles.

Figure 4-3 shows the example to transfer data between two FPGAs by using non-jumbo frame size. Left window is FPGA console from FPGA running receive data test and right window is FPGA console from FPGA running send data test.

Figure 4-4 shows the example of transfer data between two FPGAs by using jumbo frame size. When using jumbo frame size, performance is better than non-jumbo frame.

When some inputs are invalid, "Out-of-range input"/"Invalid input" is displayed and the operation is cancelled, as shown in Figure 3-5 - Figure 3-6 (similar to FPGA<->PC test).



Send Receive Input '3' to run receive data test Input '2' to run send data test Input receiver parameter Input sender parameter +++ UDPIP Send Mode +++ +++ UDPIP Receive Mode +++ 3 1 Enter transfer size : 1 - 0xFFFFFFF => 0xFFFFFFFF Enter transfer size : 1 - 0xFFFFFFFF => 0xFFFFFFFF Enter packet size : 1 - 8972 Enable data verification : [0] Disable [1] Enable => 1 => 1472 The same value Run test application on PC by following command udpdatatest t 192.168.11.25 60000 4000 4294967295 Run test application on PC by following command as re-udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 as receiver 2 Wait data from Target ... Send Ø Byte Recv 119 MByte Send Ø Byte Recv 227 MByte Press any key to start data sending ... Wait data from Target Start data sending Send 119 MByte Recv Ø Byte Send 358 MByte Recv Ø Byte 5 Display transfer size every second Send Ø Byte Recv 335 MByte 5 Send Ø Byte Recv 4103 MByte Send Ø Byte Recv 4211 MByte Send 3947 MByte Recv Ø Byte Send 4067 MByte Recv Ø Byte Display performance after Send Ø Byte Recy 4294 MByte finishing transferring all data 6 Receive data completed Send 4187 MByte Recv Ø Byte 6 Send data complete Total tx transfer size = 0 Byte Total = 0[B] , Time = 36101[ms] , Transfer speed = 0[MB/s] Iotal tx transfer size = 4294967295 Byte Iotal = 4294[MB] , Time = 35902[ms] , Transfer speed = 119[MB/s] Total rx transfer size = 4294967295 Byte Total = 4294[MB] , Time = 36101[ms] , Transfer speed = 118[MB/s] Total rx transfer size = 0 Byte Total = O[B] , Time = 35902[ms] , Transfer speed = O[MB/s] UDP1GIP menu ---101 - UDP1GIP menu ---Figure 4-3 Send/receive data test by using non-jumbo frame Send Receive +++ UDPIP Receive Mode +++ +++ UDPIP Send Mode +++ Enter transfer size : 1 - 0xFFFFFFF => 0xFFFFFFFF Enter transfer size : 1 - 0xFFFFFFFF => 0xFFFFFFFF => 8972 3 Enable data verification : [0] Disable [1] Enable => 1 Enter packet size : 1 - 8972 Set jumbo Run test application on PC by following command frame size udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 Run test application on PC by following command udpdatatest t 192.168.11.25 60000 4000 4294967295 Wait data from Target Press any key to start data sending ... Send Ø Byte Recv 124 MByte Start data sending Send Ø Byte Recv 235 MByte Send 124 MByte Recv Ø Byte Send Ø Byte Recv 347 MByte Send 248 MByte Recv Ø Byte Send 372 MByte Recv Ø Byte Send Ø Byte Recv 4032 MByte Send Ø Byte Recv 4144 MByte Send 3970 MByte Recv 0 Byte **Display performance after** Send Ø Byte Recv 4256 MByte Send 4094 MByte Recv 0 Byte finishing transferring all data 6 Receive data completed Send 4218 MByte Recv Ø Byte 6 Send data complete Total tx transfer size = 0 Byte Iotal = 0[B] , Time = 34801[ms] , Transfer speed = 0[MB/s] Total tx transfer size = 4294967295 Byte Total = 4294[MB] , Time = 34614[ms] , Transfer speed = 124[MB/s] Iotal rx transfer size = 4294967295 Byte Iotal = 4294[MB] , Time = 34801[ms] , Transfer speed = 123[MB/s] Total rx transfer size = 0 Byte [otal = 0[B] , Time = 34614[ms] , Transfer speed = 0[MB/s] --- UDP1GIP menu ---UDP1GIP menu ----Figure 4-4 Send data test by using jumbo frame

13-Jun-23



4.4 Full duplex Test

Select '4' to run full duplex test by two FPGAs transferring data in both directions at the same time and the same port number. User sets test parameters through NiosII command shell. Firmware in the demo is designed to start full duplex by server FPGA before client FPGA. The step to run the test is shown as follows.

- 1) On server NiosII command shell, set three parameters under full duplex test.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
 - b) Input packet size: Unit of packet size is byte. Valid value is 1 8972. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
 - c) Input data verification mode: '0'-disable data verification, '1'-enable data verification sent from PC.
- 2) When all inputs are valid, "Wait data from Target ..." is displayed.
- 3) On client NiosII command shell, set three parameters under full duplex test.
 - a) Input transfer size: Unit of transfer size is byte. Valid value is 0x1 0xFFF_FFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input. This input must be same as transfer size input of server FPGA.
 - b) Input packet size: Unit of packet size is byte. Valid value is 1 8972. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
 - c) Input data verification mode: '0'-disable data verification, '1'-enable data verification sent from PC.
- 4) When all inputs are valid, "Press any key to start data transfer .." is displayed. After that, user enters some key(s) to start full duplex test.
- 5) During transferring data, current transfer size is displayed on both NiosII command shells every second.
- 6) "Transfer data complete" is displayed on both NiosII command shells. Finally, total transfer size and performance are displayed on both NiosII command shells.

Figure 4-5 and Figure 4-6 show full duplex test when running by using non-jumbo frame and jumbo frame size. The left window is NiosII command shell of server FPGA while the right window is NiosII command shell of client FPGA.



Initialized as Server	Initialized as Client
Enter total size : 1 - 0xFFFFFFF => 0xFFFFFFF Enter packet size : 1 - 8972 => 1472	+++ UDPIP Full-duplex Mode +++ Input parameters Enter total size : 1 - 0xFFFFFFFF Enter packet size : 1 - 8972 Enable data verification : [0] Disable [1] Enable => 1
Run two test application on PC by following command	Run two test application on PC by following command The same value as Server
	1) PC receive data test (UDPIP -> PC) udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000
	2) PC send data test (PC -> UDPIP) udpdatatest t 192.168.11.42 4000 60000 4294967295
Wait data from Target Wait data from Target Start data transferring Send 119 MByte Send 119 MByte Recv 119 MByte Send 227 MByte Recv 227 MByte Send 335 MByte Recv 335 MByte 5	Press any key to start data transfer Start data transferring Send 119 MByte Recu 119 MByte Send 227 MByte Recu 227 MByte Send 335 MByte Recu 335 MByte
Send 4211 MByte Recv 4211 MByte Send 4294 MByte Recv 4294 MByte	Send 3996 MByte Recv 3996 MByte Send 4103 MByte Recv 4104 MByte Send 4211 MByte Recv 4211 MByte Fransfer data complete
Total tx transfer size = 4294967295 Byte Total = 4294[MB] , Time = 36101[ms] , Transfer speed = 118[MB/s]	Fotal tx transfer size = 4294967295 Byte Fotal = 4294[MB] , Time = 36004[ms] , Transfer speed = 119[MB/s]
Total rx transfer size = 4294967295 Byte Total = 4294[MB] , Time = 36101[ms] , Transfer speed = 118[MB/s]	[otal rx transfer size = 4294967295 Byte [otal = 4294[MB] , Time = 36004[ms] , Transfer speed = 119[MB/s]
UDP1GIP menu	UDP1GIP menu
Figure 4-5 Full duplex test	when using non-jumbo frame
Initialized as Server +++ UDPIP Full-duplex Mode +++ 1 Enter total size : 1 - 0xFFFFFFFF => 0xFFFFFFFF Enter packet size : 1 - 8972 Enable data verification : [0] Disable [1] Enable => 1	Initialized as Client +++ UDPIP Full-duplex Mode +++ Enter total size : 1 - 0xFFFFFFF => 0xFFFFFFF Enter packet size : 1 - 8972 => 8972 Enable data verification : [0] Disable [1] Enable => 1
Run two test application on PC by following command	Run two test application on PC by following command
1> PC receive data test (UDPIP -> PC)	
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000	1) PC receive data test (UDPIP -> PC) udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000 2) PC send data test (PC -> UDPIP>	udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 2) PC send data test (PC -> UDPIP)
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000 2) PC send data test (PC -> UDPIP> udpdatatest t 192.168.11.25 60000 4000 4294967295 Wait data from Target Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte	udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 2) PC send data test (PC -> UDPIP) udpdatatest t 192.168.11.42 4000 60000 4294967295 Press any key to start data transfer Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000 2) PC send data test (PC -> UDPIP> udpdatatest t 192.168.11.25 60000 4000 4294967295 Wait data from Target Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 347 MByte Recv 347 MByte Send 4033 MByte Recv 4032 MByte Send 4144 MByte Recv 4144 MByte Send 4256 MByte Recv 4256 MByte Send 4256 MByte Recv 4256 MByte	udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 2) PC send data test (PC -> UDPIP) udpdatatest t 192.168.11.42 4000 60000 4294967295 Press any key to start data transfer Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 347 MByte Recv 347 MByte Send 4033 MByte Recv 4033 MByte Send 4033 MByte Recv 4145 MByte Send 4256 MByte Recv 4256 MByte Transfer data complete Total tx transfer size = 4294967295 Byte
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000 2) PC send data test (PC -> UDPIP> udpdatatest t 192.168.11.25 60000 4000 4294967295 Wait data from Target Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 347 MByte Recv 347 MByte Send 4033 MByte Recv 4032 MByte Send 4144 MByte Recv 4032 MByte Send 4144 MByte Recv 4144 MByte Send 4256 MByte Recv 4256 MByte Transfer data complete Total tx transfer size = 4294967295 Byte Total = 4294[MB], Time = 34801[ms], Transfer speed = 123[MB/s] Total rx transfer size = 4294967295 Byte	udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 2) PC send data test (PC -> UDPIP) udpdatatest t 192.168.11.42 4000 60000 4294967295 Press any key to start data transfer Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 347 MByte Recv 347 MByte Send 4033 MByte Recv 4033 MByte Send 4033 MByte Recv 4145 MByte Send 4256 MByte Recv 4256 MByte Transfer data complete Total tx transfer size = 4294967295 Byte
udpdatatest r 192.168.11.25 60000 4000 4294967295 1 1000 2) PC send data test (PC -> UDPIP> udpdatatest t 192.168.11.25 60000 4000 4294967295 Wait data from Target Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 347 MByte Recv 347 MByte Send 4033 MByte Recv 4032 MByte Send 4144 MByte Recv 4032 MByte Send 4256 MByte Recv 4144 MByte Send 4256 MByte Recv 4256 MByte Transfer data complete Total tx transfer size = 4294967295 Byte Total = 4294[MB], Time = 34801[ms], Transfer speed = 123[MB/s] Total rx transfer size = 4294967295 Byte Total = 4294[MB], Time = 34801[ms], Transfer speed = 123[MB/s] UDP1GIP menu	udpdatatest r 192.168.11.42 4000 60000 4294967295 1 1000 2) PC send data test (PC -> UDPIP) udpdatatest t 192.168.11.42 4000 60000 4294967295 Press any key to start data transfer Start data transferring Send 124 MByte Recv 124 MByte Send 235 MByte Recv 235 MByte Send 4033 MByte Recv 4033 MByte Send 4033 MByte Recv 4033 MByte Send 4256 MByte Recv 4145 MByte Send 4256 MByte Recv 4256 MByte Transfer data complete Iotal tx transfer size = 4294967295 Byte Iotal rx transfer size = 4294967295 Byte Iotal rx transfer size = 4294967295 Byte



5 Revision History

Revision	Date	Description
1.0	3-Mar-17	Initial version release
2.0	10-Nov-20	Remove hardware setup from the document