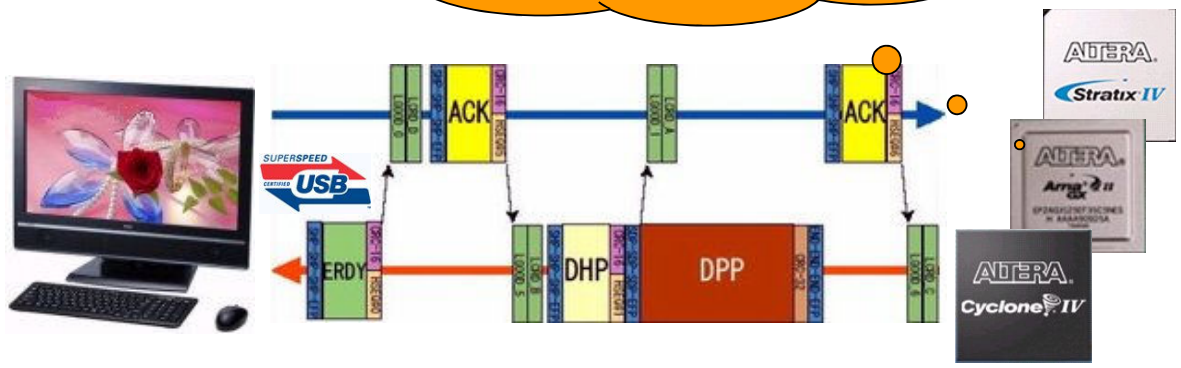
USB3.0 Device IP for Altera

Ver1.1AE

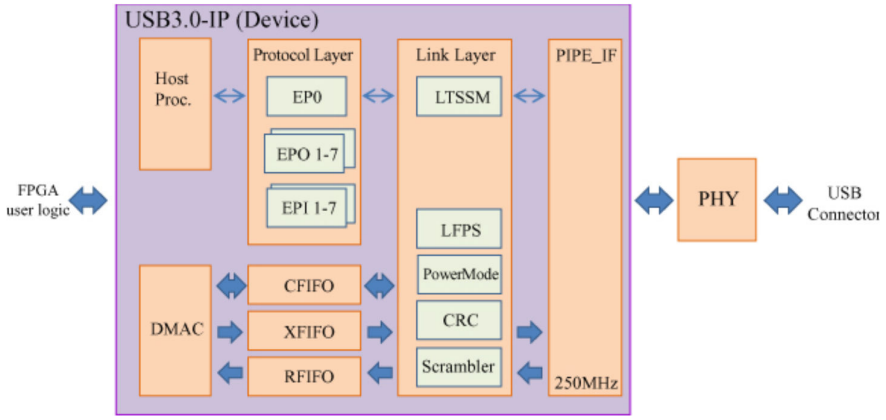
Supports Stratix-IV / Arria-II / Cyclone-IV



Enchant your product with SuperSpeed!

USB3.0-IP Core introduction

- **IP Core to support USB3.0 SuperSpeed for Device (USB3D-IP)**
- **Includes Protocol&Link Layer as well as DMAC, Host I/F, and PIPE I/F**
- **Practical implementation is provided by reference design.**



USB3.0-IP Core merit1

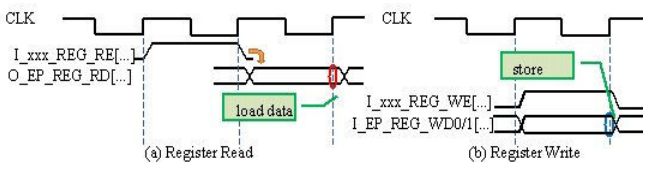
- Supports SuperSpeed(5.0Gbps) of USB3.0 Standard.
- Provides controller function of USB Device.
- Connects with external PHY device. (TUSB1310A of T.I)
- Includes USB3.0 PIPE interface. (250MHz@16bit)
- Saves FPGA resource usage by limiting SuperSpeed only.

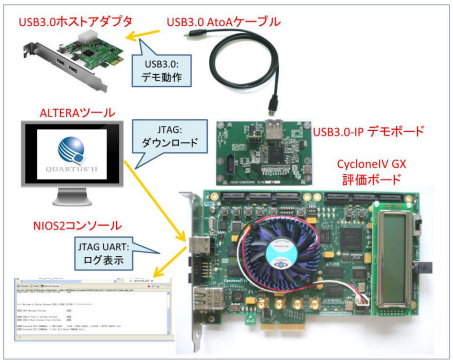
Family	Example Device	Fmax (MHz)	Combinational ALUTs[4] Logic Elements	Registers[1]	Pin[2]	Block Memori bit	PLL	GXB	Design Tools
CycloneIV GX	EP4CGX150DF31C7	130	7,507	3,699	68	18,432	2	0	QuartusII 10.1
Arria II GX	EP2AGX125EF35C4	147	4,689	3,825	68	9,216	2	0	QuartusII 10.1

USB3.0-IP resource report (1 Control, 2 IN/OUT each)

USB3.0-IP Core merit2

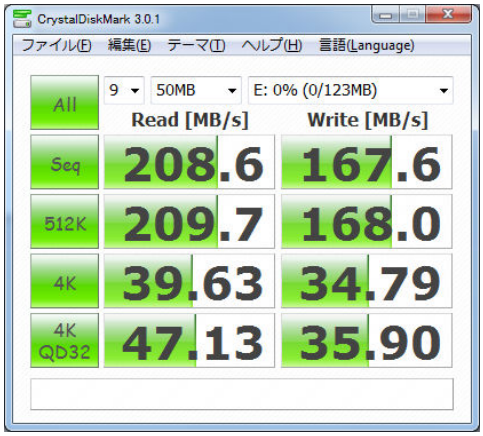
- Supports 15 IN/OUT Endpoints at maximum.
  - 1 Control Endpoint
  - 7 IN/OUT Endpoints each at maximum.
- Supports all transport type.
  - (Control/Bulk/Isochronous/Interrupt)
- Real board evaluation with Altera FPGA board
- Simple and easy connection user I/F.





Device-IP Core performance

- **Best performance in existing USB3.0 system.**
  - **High performance at both sequential and random access.**
  - **Provides design that minimizes overhead.**



USB3D-IP benchmark result

(Reference: competitor result)

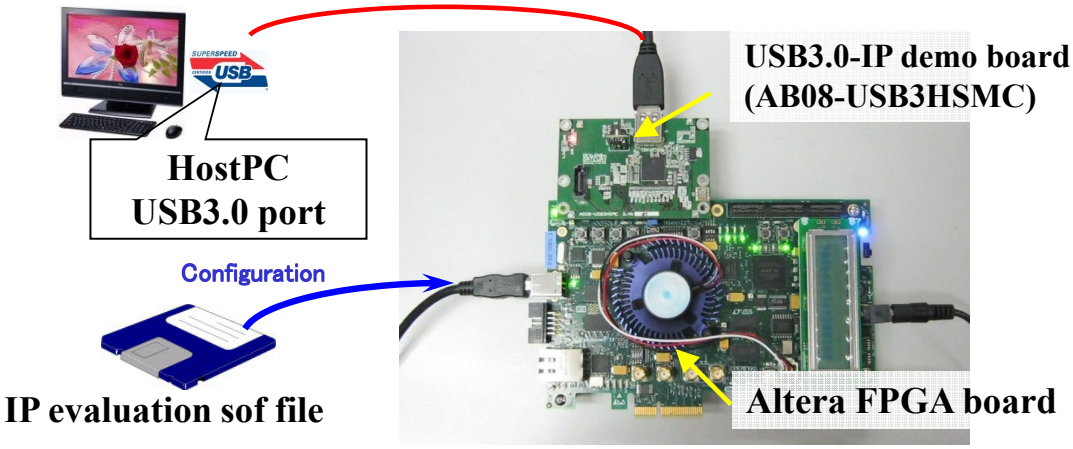
Core product line up

- **Supported FPGA and product information**
  - **USB3D-IP-S4:**
    - **USB3D-IP core for Stratix-IV**
  - **USB3D-IP-A2:**
    - **USB3D-IP for Arria-II**
  - **USB3D-IP-C4:**
    - **USB3D-IP for Cyclone-IV**

- **Next production plan**
  - **Host-IP core under development**

Evaluation sof-file

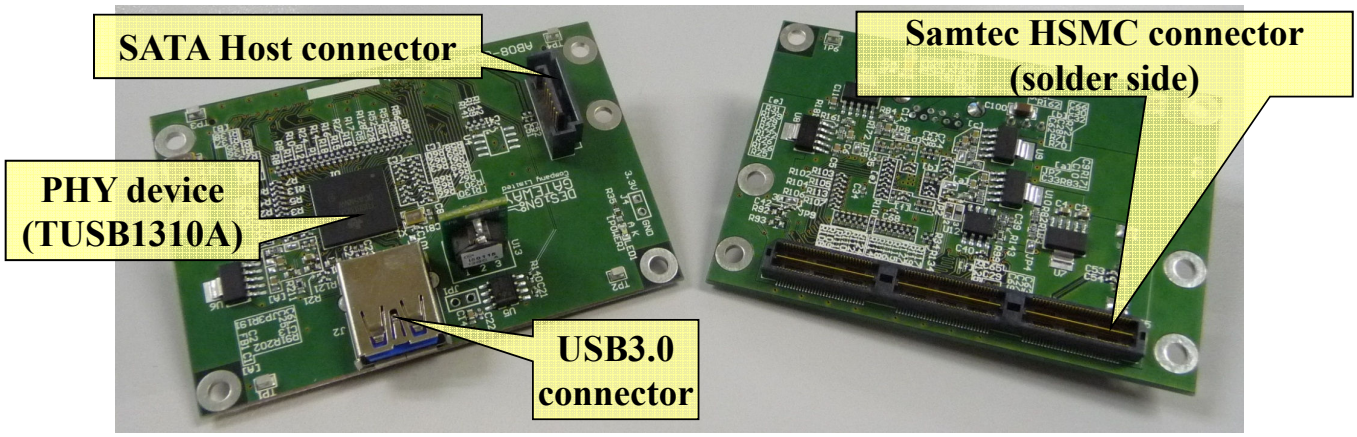
- Free sof-file for evaluation using Altera FPGA board
  - Cyclone-IV GX / Arria-II GX / Stratix-IV GX board
- Demo board (AB08-USB3HSMC) is required



USB3.0-IP evaluation environment

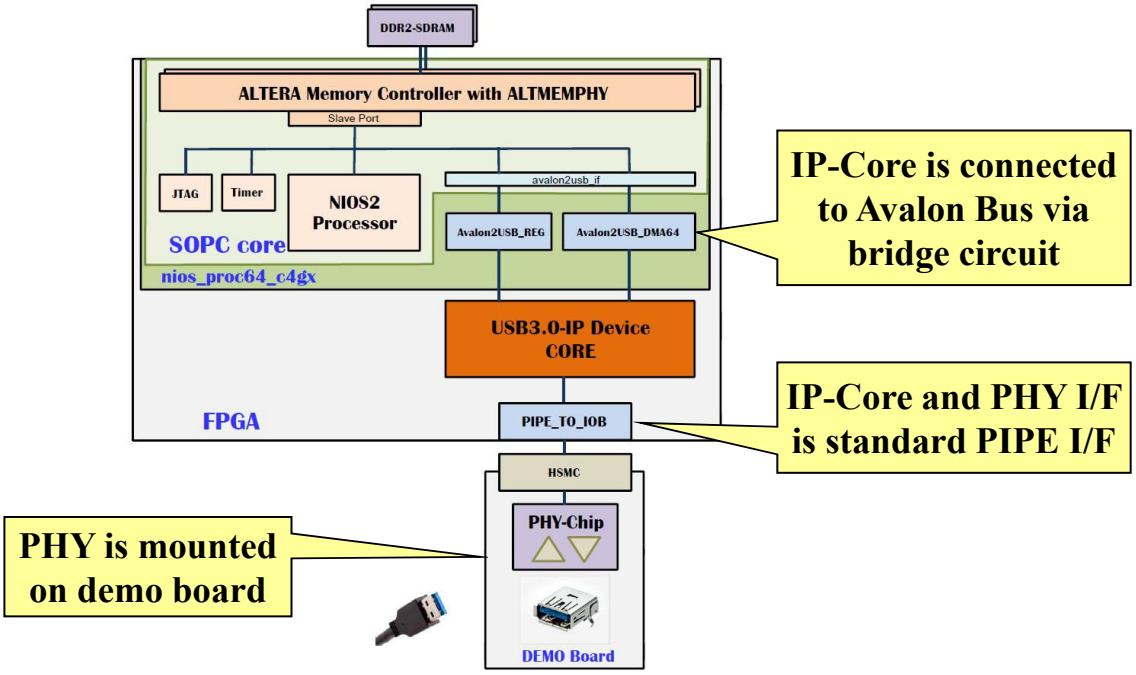
Demo board（AB08-USB3HSMC)

- Connects with Altera standard HSMC extention I/F
- Mounts TUSB1310A (T.I) and peripheral circuit
- Mounts additional SATA Host connector



AB08-USB3HSMC

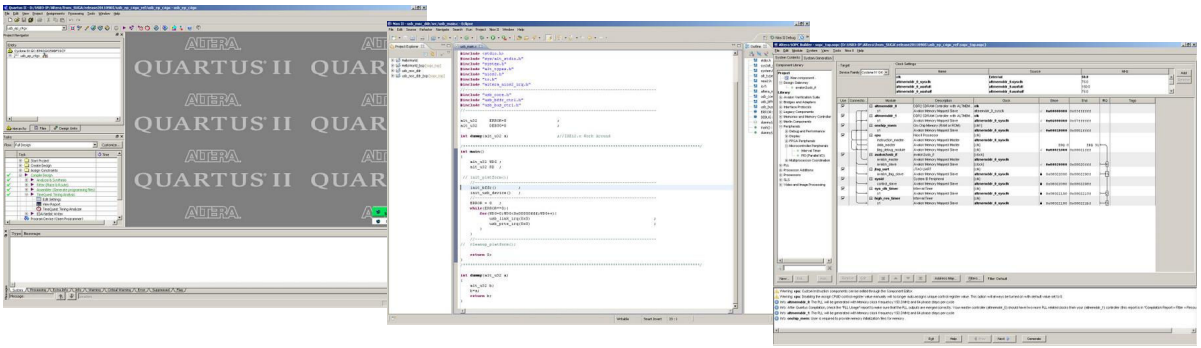
Reference Design Project



Reference Design block diagram

Reference Design (Summary)

- **Real operation on Altera FPGA board and demo board.**
  - **QuartusII/NiosII project of evaluation sof-file**
- **Provides all HDL source code except IP-Core**
  - **Also provides NiosII firmware by C source**



Reference Design (Device function)

- **HostPC can recognize storage class device**
- **Emulate RamDisk by DDR memory on FPGA board**

Inquiry

- **Detailed technical information on Web site**
- **http://www.design-gateway.com/ or**
- **http://www.dgway.com/products/IP/USB3-IP/Altera/index-E.html**
- **Inquiry**
  - **Design Gateway Co.,Ltd.**
  - **E-mail : sales@design-gateway.com**
  - **FAX : +662-261-2290**

Revision History

Rev.	Date	Description
1.1AE	2012/07/11	Release English presentation