USB3D-IP (USB3.0-Device function IP) demo manual

Rev 1.3E / 15 May, 2015

This document describes USB3D-IP (USB3.0 device function IP-Core) evaluation procedure using Altera evaluation board (CycloneIV GX board, CycloneVE board, and ArriaV GX starter board) or Xilinx evaluation board (SP605, ML605, KC705, and ZC706 board) and USB3.0 adapter board with evaluation sof-file or bit-file

1. Evaluation Environment

This demo design operates under following environment shown at Figure 1.

1-1 Altera Environment

For Altera USB3.0 Device-IP evaluation, user must arrange following environment.

- Altera evaluation board (Cyclone IV GX board in this example)
- USB3.0 adapter board from DesignGateway [Part# AB08-USB3HSMC]
- USB3.0 A to A cable attached with adapter board.
- Altera sof-file download tool (programmer) and NiosII console.
- Host PC with USB3.0 port. (PCIe extension USB3.0 host card is also available, however, such PCIe extension host card is sensitive to analog characteristics such as error occurrence at some PCIe slot position. And PCIe extension host card cannot provide enough transfer performance when PCIe interface is 1-lane and not GEN2 but GEN1 speed because GEN1 1-lane PCIe I/F limits its performance to 2.5Gbps=200Mbyte/s at maximum.)

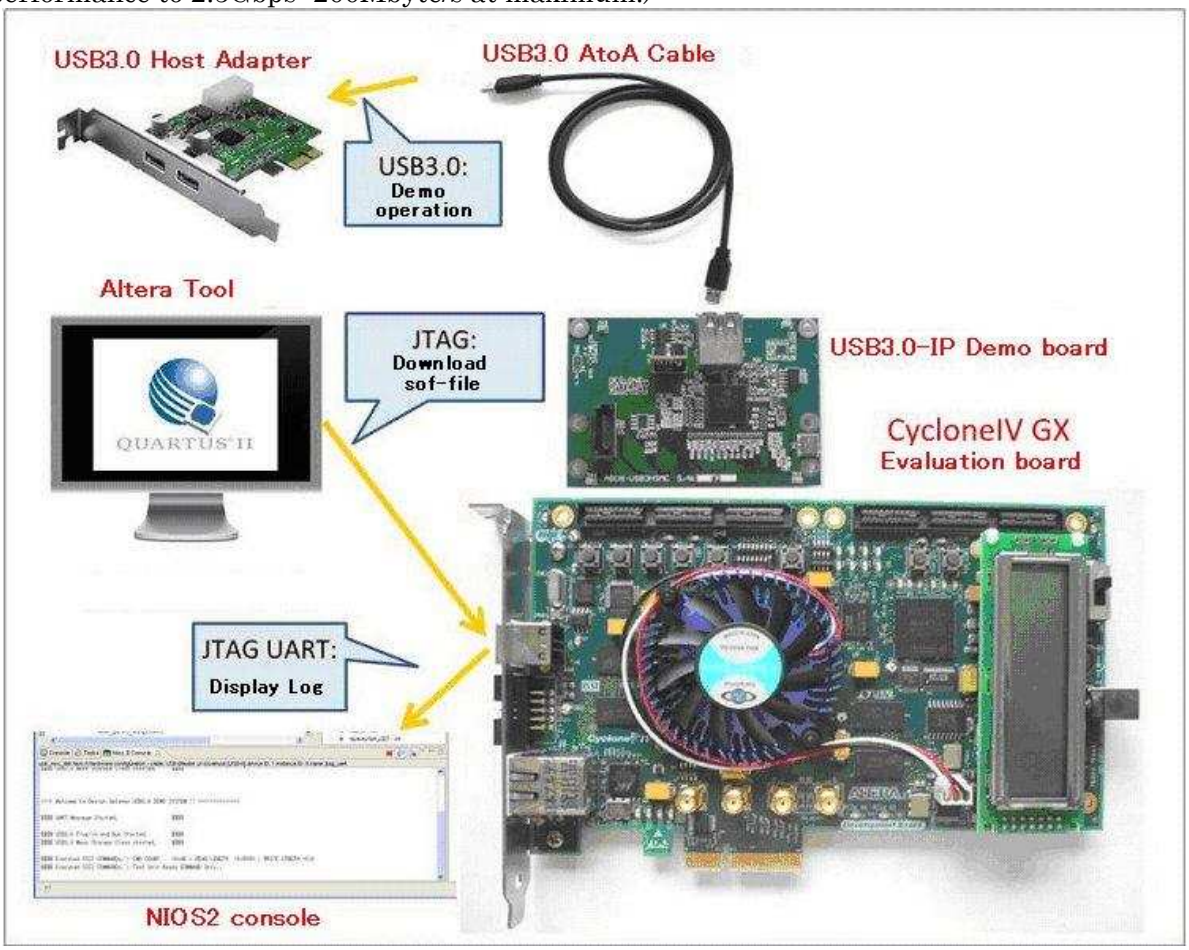

Figure 1: Altera demo environment for USB3D-IP evaluation

(Notes) Evaluation sof-file has 1-hour time limit operation after FPGA configuration.

1-2 Xilinx Environment

For Xilinx USB3.0 Device-IP evaluation, user must arrange following environment.

- Xilinx evaluation board (SP-605 in this example)
- USB3.0 adapter board from DesignGateway [Part# AB07-USB3FMC]
- USB3.0 A to A cable attached with adapter board.
- Xilinx bit-file download tool (iMPACT) and serial console such as Teraterm.
- Host PC with USB3.0 port. (PCIe extension USB3.0 host card is also available, however, such PCIe extension host card is sensitive to analog characteristics such as error occurrence at some PCIe slot position. And PCIe extension host card cannot provide enough transfer performance when PCIe interface is 1-lane and not GEN2 but GEN1 speed because GEN1 1-lane PCIe I/F limits its performance to 2.5Gbps=200Mbyte/s at maximum.)

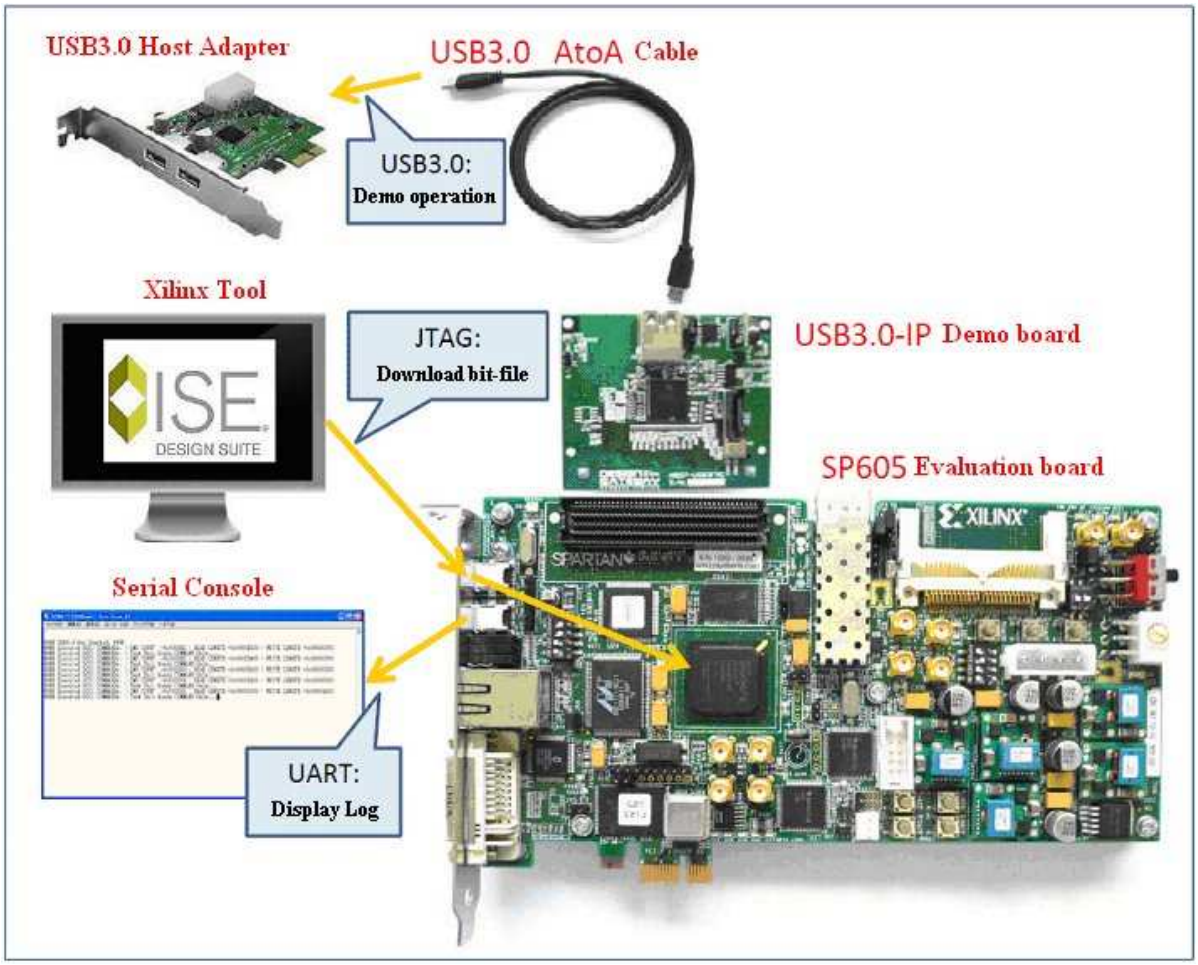

Figure 2: Xilinx demo environment for USB3D-IP evaluation

(Notes) Evaluation bit-file has 1-hour time limit operation after FPGA configuration.

2. Evaluation procedure

2-1 Altera Evaluation Procedure

For Altera USB3.0 Device-IP evaluation, follow evaluation procedure below.

- Check that both Altera board (CycloneIV GX/CycloneVE/ArriaV GX starter board) and adapter board are powered off.
- Connect USB Cable to USB connector on Altera board (J4 for CycloneIV GX board/J10 for CycloneVE board/J14 for ArriaV GX starter board) for JTAG programming and JTAG UART operation.
- Set HSMC interface voltage of CycloneIV GX board to 2.5V. (Short J3 header. Refer to CycloneIV GX board manual for more detail.)
- Connect adapter board (AB08-USB3HSMC) to HSMC connector.
- Confirm that JP1 on the adapter board is not jumped (OFF).
- Connect USB3.0 AtoA cable with USB connector on the adapter board.
- Connect opposite side of USB3.0 AtoA cable to the USB3.0 connector of the Host PC.

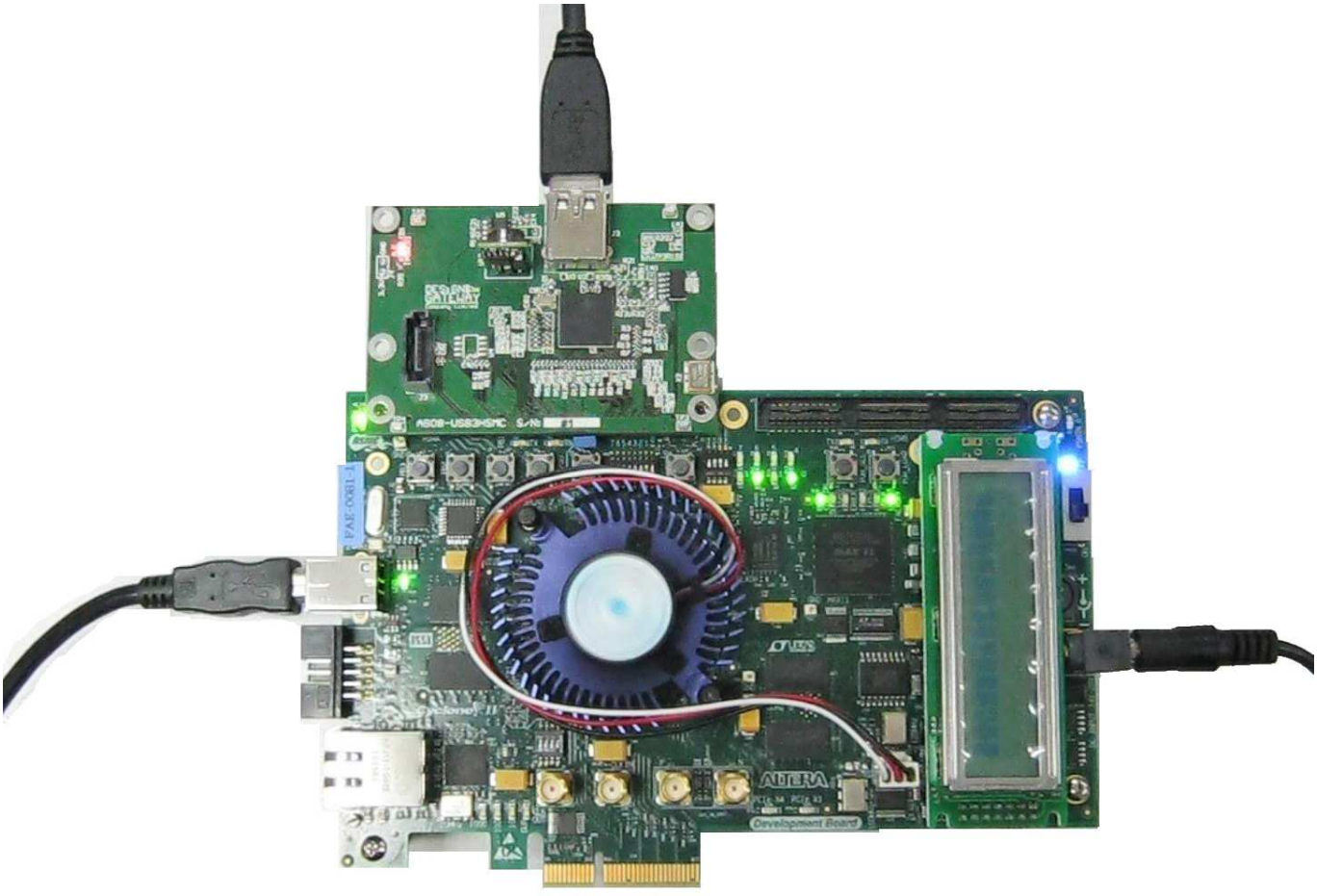

Figure 3: Adapter board connection to CycloneIV GX board

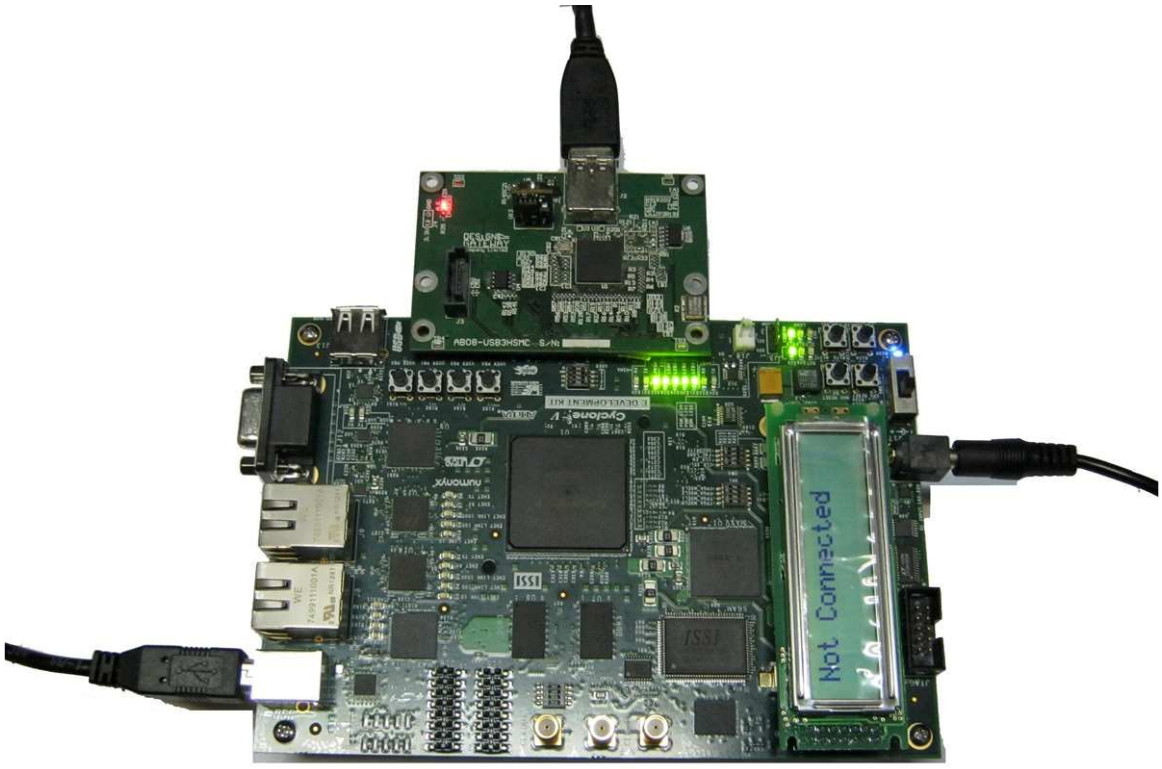

Figure 4: Adapter board connection to CycloneVE board

Figure 5: Adapter board connection to ArriaV GX starter board

- Power up all boards, run ALTERA Programmer on the PC, and download evaluation sof-file to the FPGA. After download finish, close Programmer software. (At this timing, (FPGA operation is already running and FPGA is waiting JTAG UART output.)
- Run nios2-terminal from "ALTERA NIOS2 Command Shell" as below Figure 6.

Figure 6: start nios2-terminal

- When JTAG UART starts its operation, it shows message as Figure 7. If nios2-terminal cannot start or this message is not appeared, check USB cable or download settings of Programmer.

Figure 7: Device operation start message

- After sof-file download finish and JTAG UART operation start, check USER_LED0-3 status near by HSMC connector on the Altera board. See Table 1 for LED definition. Note that LED0 blinks and other LEDs are OFF when USB cable is unplugged. When USB cable is connected again, LED will change its state as shown in Figure 8.

LED	Status	Description
LED0	OFF	Altera FPGA configuration is not completed.
	Blink	VBUS is not detected. USB cable is not plugged correctly for example.
	ON	USB cable is plugged correctly and FPGA detects VBUS presence.
LED1	OFF	USB3.0 Mass Storage Class operation is not started yet. Altera board might have problem such as memory initialization fail.
	ON	USB3.0 Mass Storage Class operation is started successfully.
LED2	OFF	Cannot initialize USB3.0 LINK process. Check HSMC connection of the demo board. Check that USB3.0 cable is the demo board attached cable.
	ON	USB3.0 LINK initialization completed successfully.
LED3	OFF	USB3.0 Mass Storage Class detection by HostPC is not completed. It is possible that signal quality problem exists in the host USB3.0 adapter or device driver has some problem.
	ON	USB3.0 Mass Storage Class detection by HostPC is completed successfully.

Table 1: LED definition of Altera board

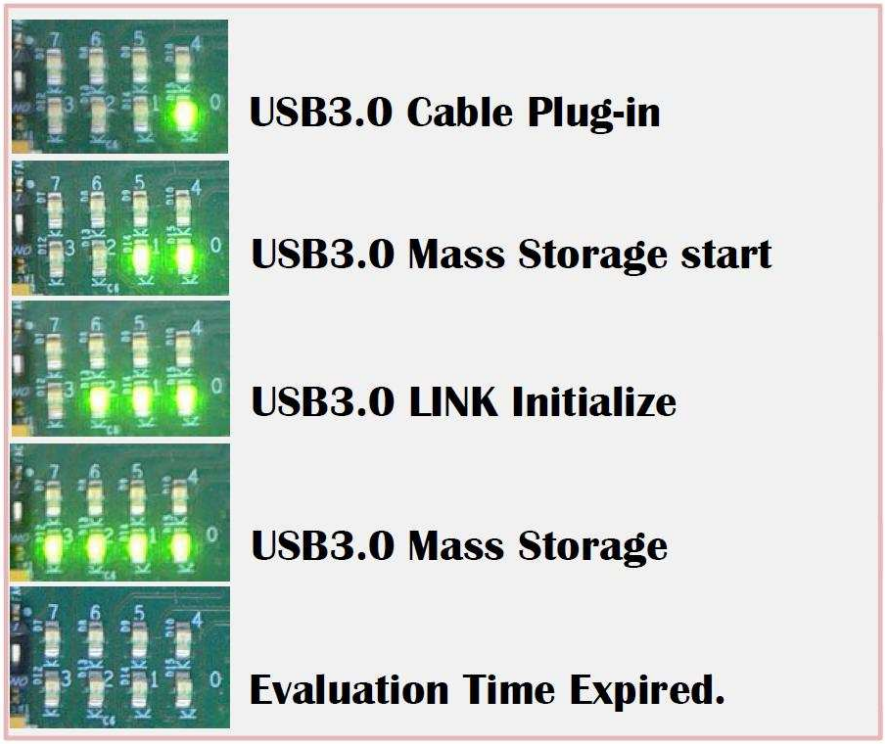

Figure 8: USB3.0 device operation LED0-LED3 status on Altera board

※ All LED will be OFF when 1-hour time limitation is expired.

- After FPGA operation starts, at least following Figure 9 message will appear on the serial console.

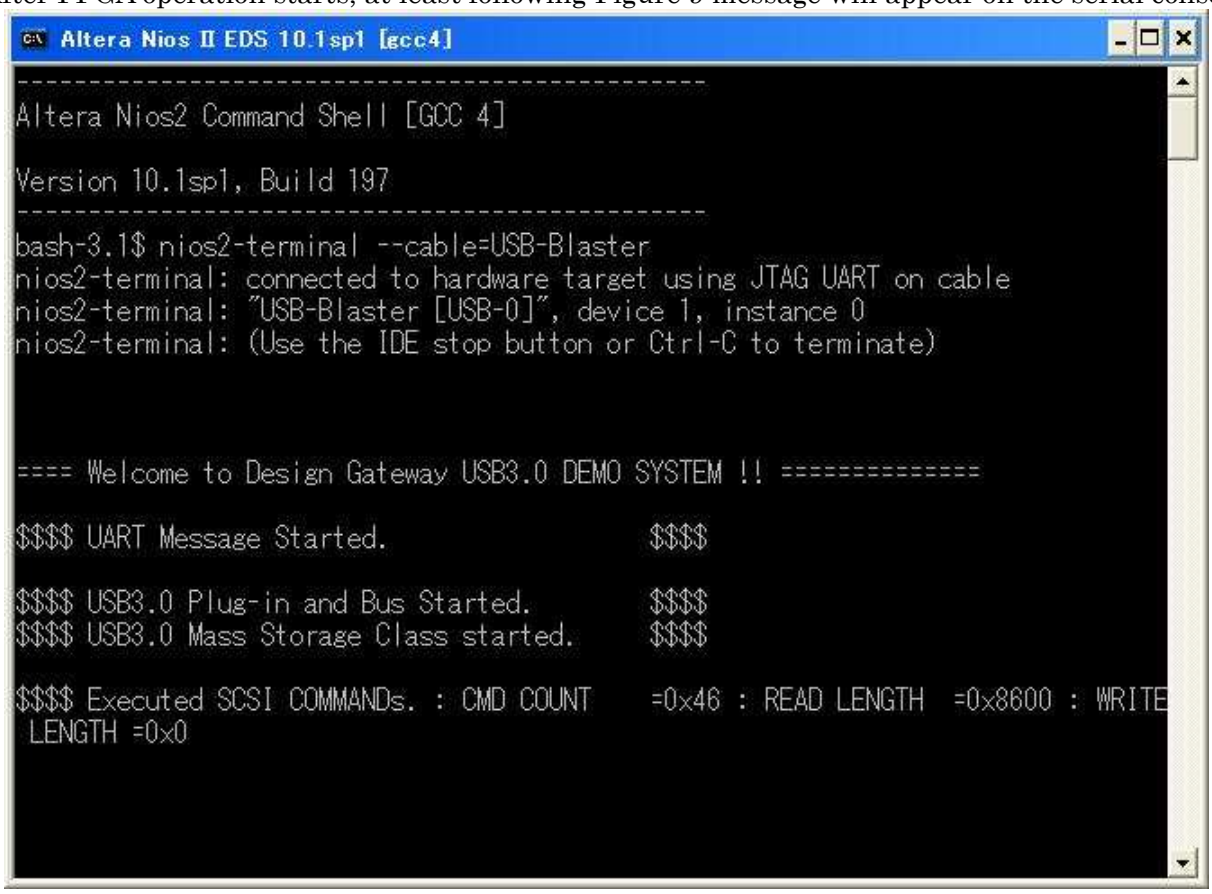

Figure 9: Mass Storage Class operation start message

2-2 Xilinx Evaluation Procedure

For Xilinx USB3.0 Device-IP evaluation, follow evaluation procedure below.

- Check that both Xilinx board (SP605/ML605/KC705/ZC706 board) and adapter board are powered off.
- a) SP605/ML605: Connect USB mini-cable#1 to USB mini-connector on Xilinx board (J4 for SP605/J22 for ML605) for JTAG programming.
  b) KC705/ZC706: Connect USB micro cable to USB micro connector on Xilinx board (U29 for KC705/U30 for ZC706) for JTAG programming.
- Connect USB mini-cable#2 to USB mini-connector on Xilinx board (J23 for SP605/J21 for ML605/J6 for KC705/J21 for ZC706) for serial console I/F on HostPC.
- Confirm that FMC interface voltage is 2.5V, and then connect adapter board (AB07-USB3FMC) to the FMC-LPC connector on Xilinx board.
- Confirm that JP1 on the adapter board is not jumped (OFF).
- Connect USB3.0 AtoA cable with USB connector on the adapter board.
- Connect opposite side of USB3.0 AtoA cable to the USB3.0 connector of the Host PC.

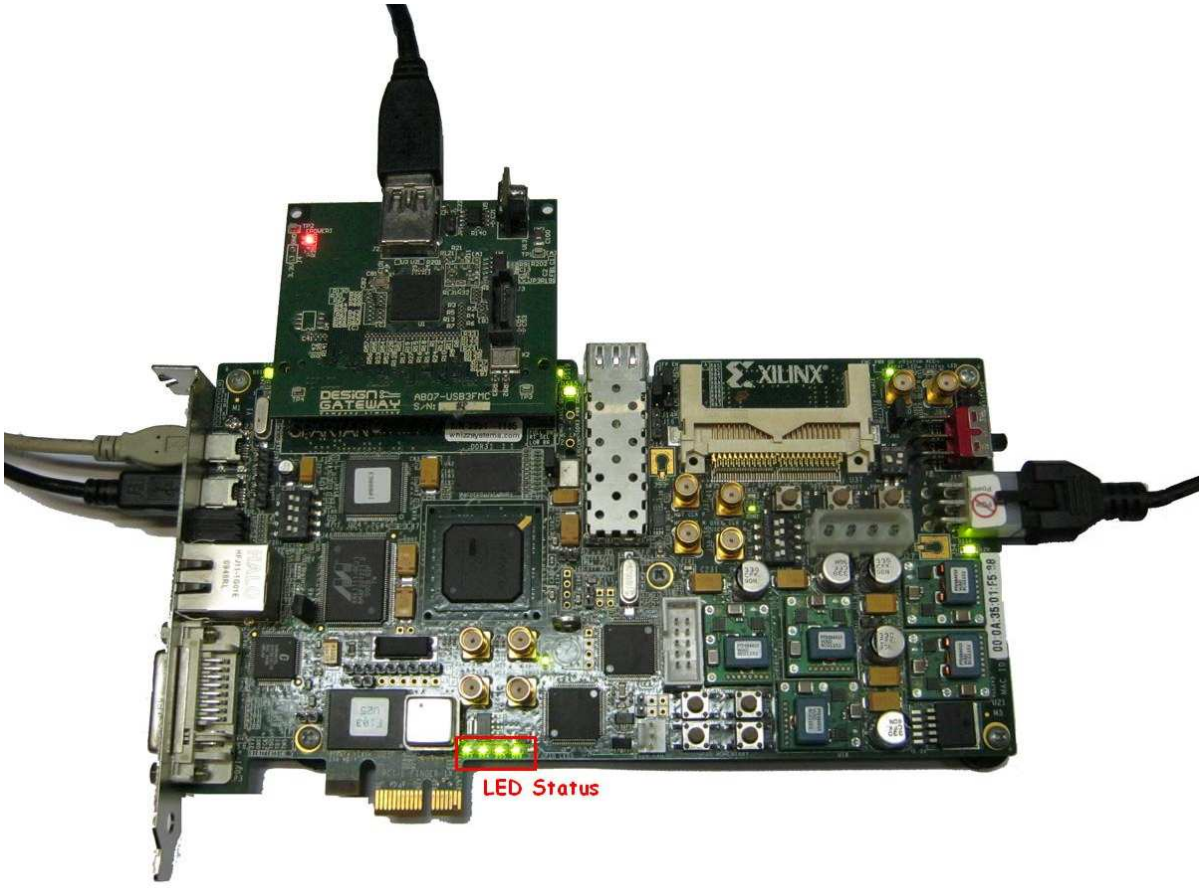

Figure 10: Adapter board connection to SP605

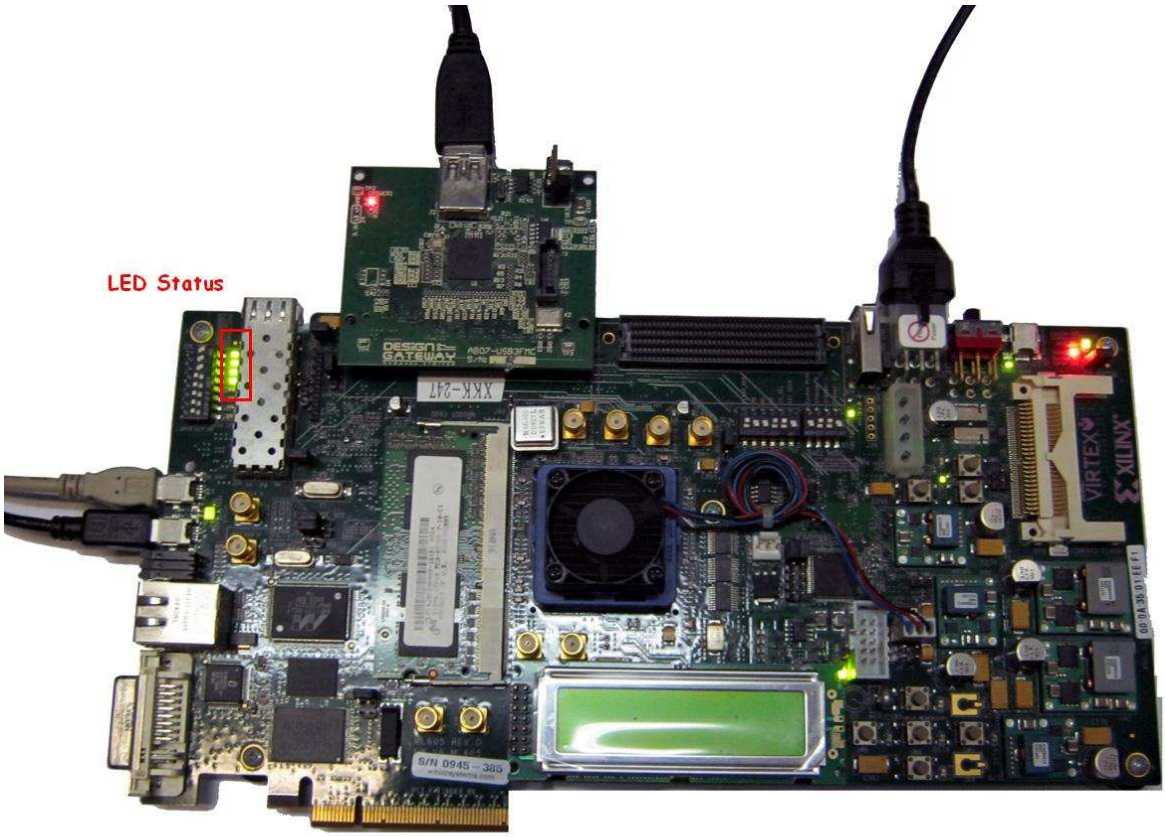

Figure 11: Adapter board connection to ML605

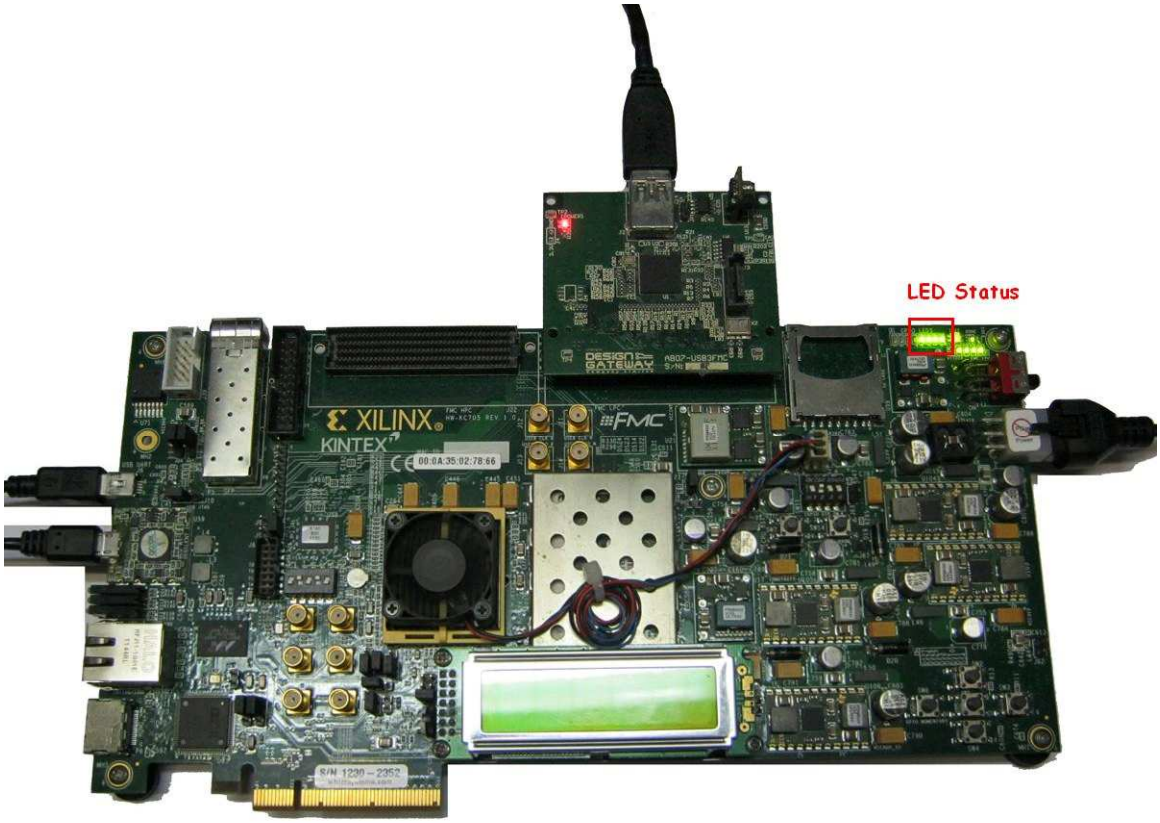

Figure 12: Adapter board connection to KC705

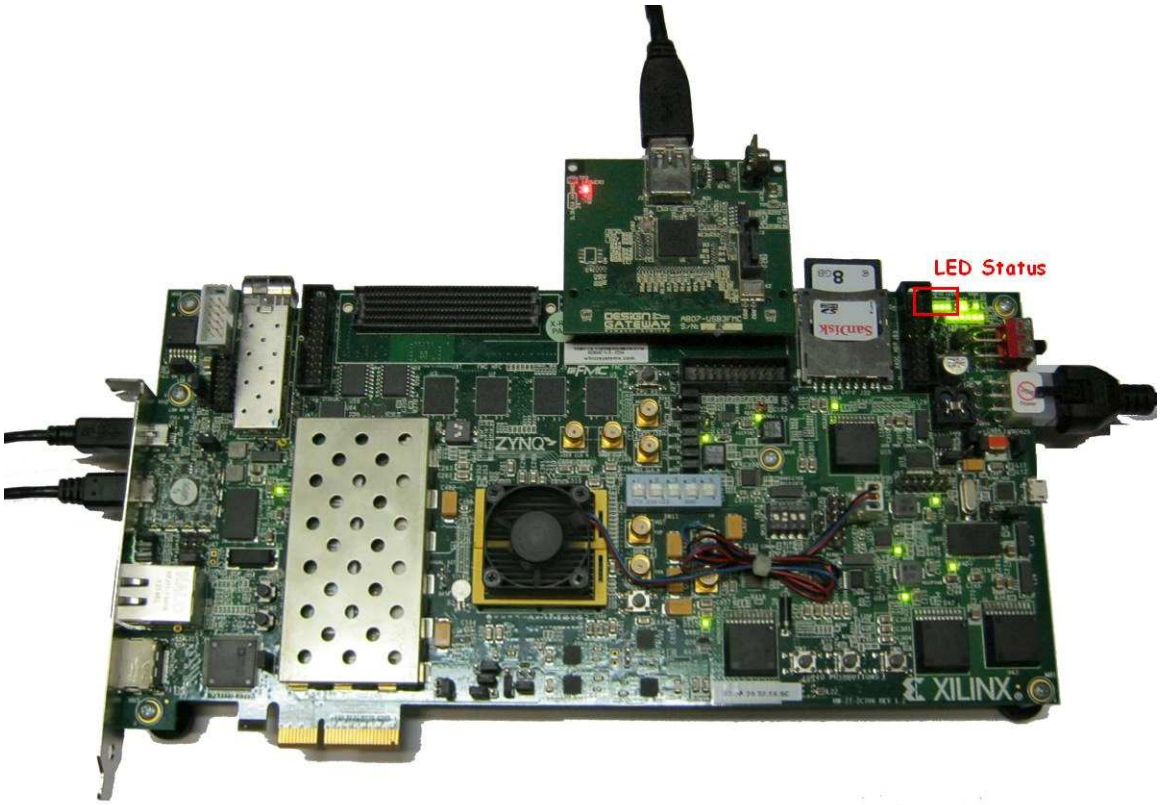

Figure 13: Adapter board connection to ZC706

- Power up all demo device, run serial terminal (TeraTerm for example) and set following communication parameter
  Baud Rate = 115,200 Data = 8bit Stop Bit = 1 Parity = None
- a) Start iMPACT and download evaluation bit-file to FPGA.
  b) For ZC706 board only, set SW11="00000" to configure PS from JTAG, and set SW4="01" to connect JTAG to USB-to-JTAG interface, as shown in Figure 14 and Figure 15. After that, open ISE command prompt and run bat file to download bit-file and elf-file to FPGA, as shown in Figure 16.

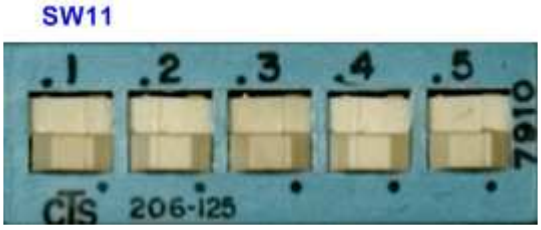

Figure 14: SW11 setting on ZC706 board

Figure 15: SW4 setting on ZC706 board

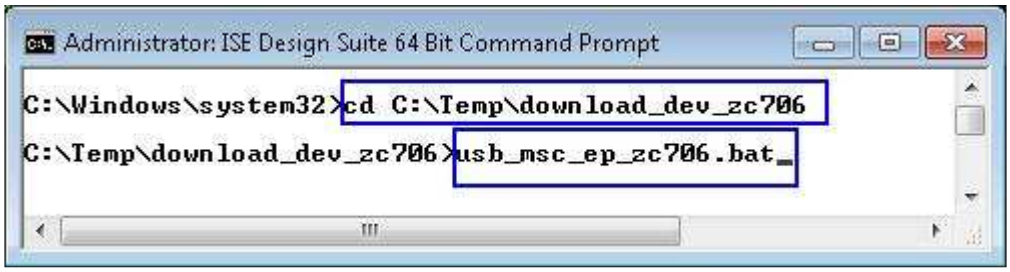

Figure 16: Run bat file to program bit and elf file on ZC706 board

- After bit-file download finish, check GPIO_LED0-3 status on Xilinx board. See table-2 for LED definition. Note that LED0 blinks and other LEDs are OFF when USB cable is unplugged. When USB cable is connected again, LED will change its state as shown in Figure 17.

LED	Light	Description
DS3/LED0	OFF	SP-605 FPGA configuration is not completed.
	Blink	VBUS is not detected. USB cable is not plugged correctly for example.
	ON	USB cable is plugged correctly and detects VBUS presence.
DS4/LED1/R	OFF	USB3.0 Mass Storage Class operation is not started yet. SP-605 board might have problem such as memory initialization fail.
	ON	USB3.0 Mass Storage Class operation is started successfully.
DS5/LED2/C	OFF	Cannot initialize USB3.0 LINK process. Check FMC connection of the demo board. Check that USB3.0 cable is the demo board attached cable.
	ON	USB3.0 LINK initialization completed successfully.
DS6/LED3/L	OFF	USB3.0 Mass Storage Class detection by HostPC is not completed. It is possible that signal quality problem exists in the host USB3.0 adapter or device driver has some problem.
	ON	USB3.0 Mass Storage Class detection by HostPC is completed successfully.

Table-2: LED definition of SP605 board

Figure 17: USB3.0 device operation LED status on SP605 board

※ All LED will be OFF when 1-hour time limitation is expired.

- After FPGA operation starts, at least following Figure 18 message will appear on the serial console. (same meaning of DS4). If Figure 18 message does not appear, check serial (USB mini) cable as well as serial communication parameters.

Figure 18: Device operation start message

- When communication with HostPC is successfully started, following Figure 19 message will appear on the serial console (same meaning of DS6).

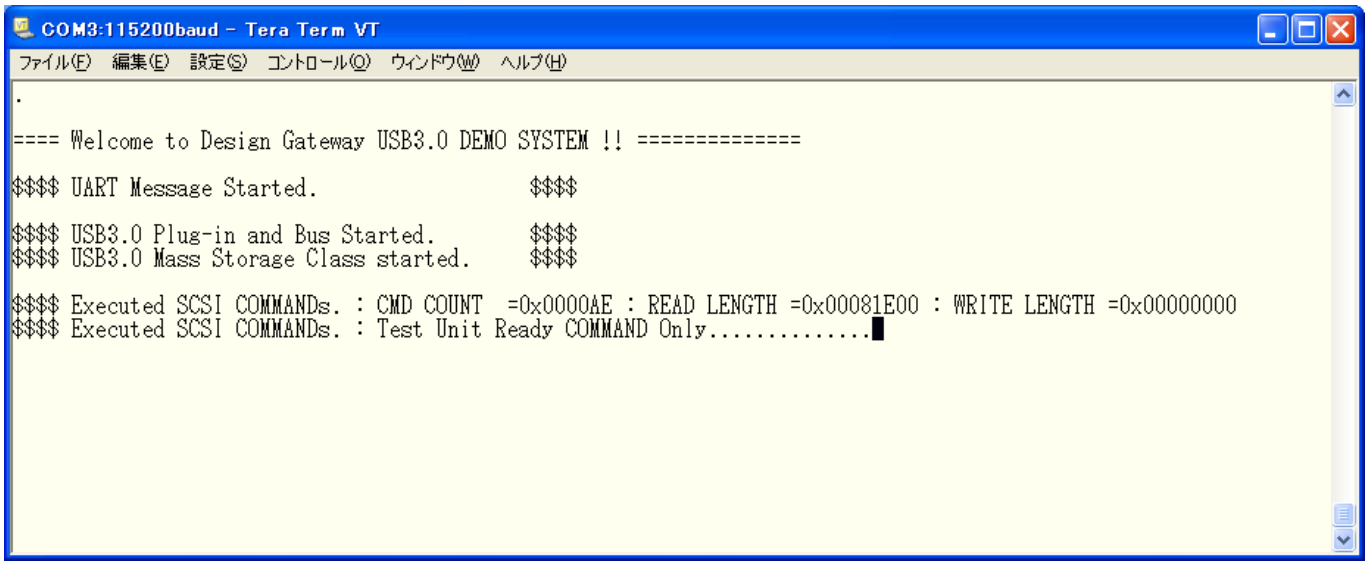

Figure 19: Mass Storage Class operation start message

3. Demo operation example

- The demo design emulates general USB removable drive so that user can check same functions and operations. However, the demo design has following limitation.
  (1) The demo design uses on-board 128Mbytes DDR memory and assigns 127Mbytes as a storage memory space.
  (2) Because storage memory is volatile, stored data on the DDR memory will be disappeared when power is off and user must execute format after every power cycle.

1. Windows on the HostPC will firstly request format after power cycle of demo design.
   So user must execute normal format operation.
   If Windows does not show message, then execute format manually, however in this case, enough care must be taken not to format incorrect drive.
   DesignGateway is not responsible for any trouble or problem caused by such incorrect operation.

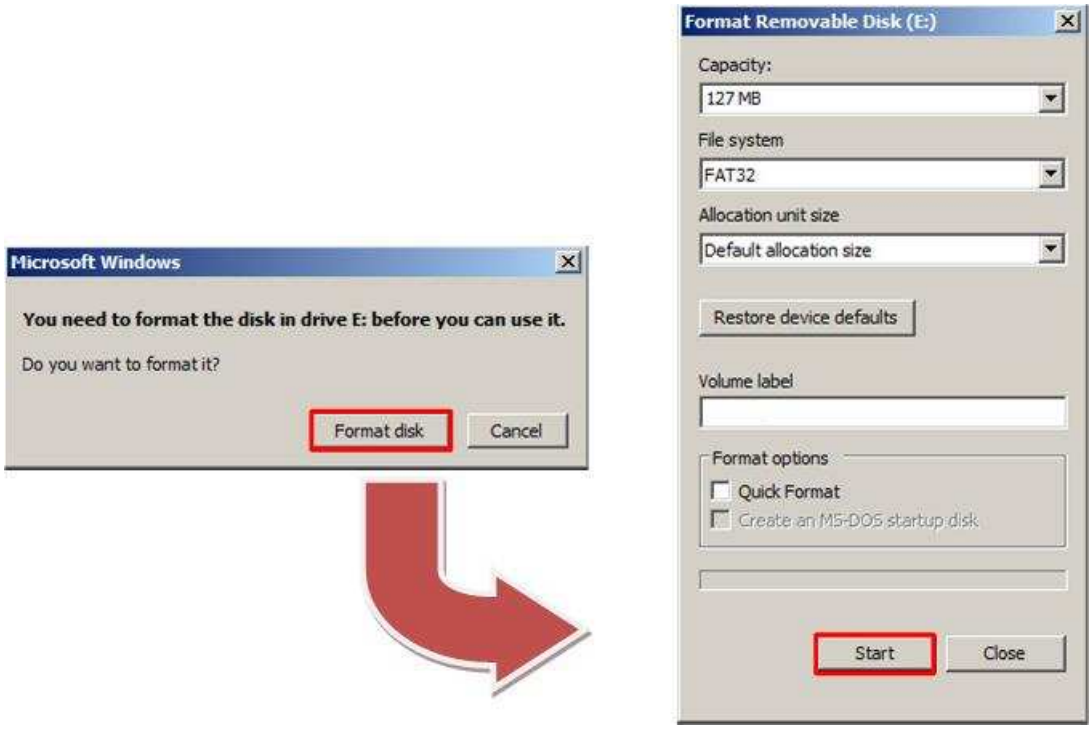

Figure 20: Execute format to the demo drive

2. Device Manager
   User can confirm by the device manager of Windows that demo drive is recognized as an USB mass storage device.

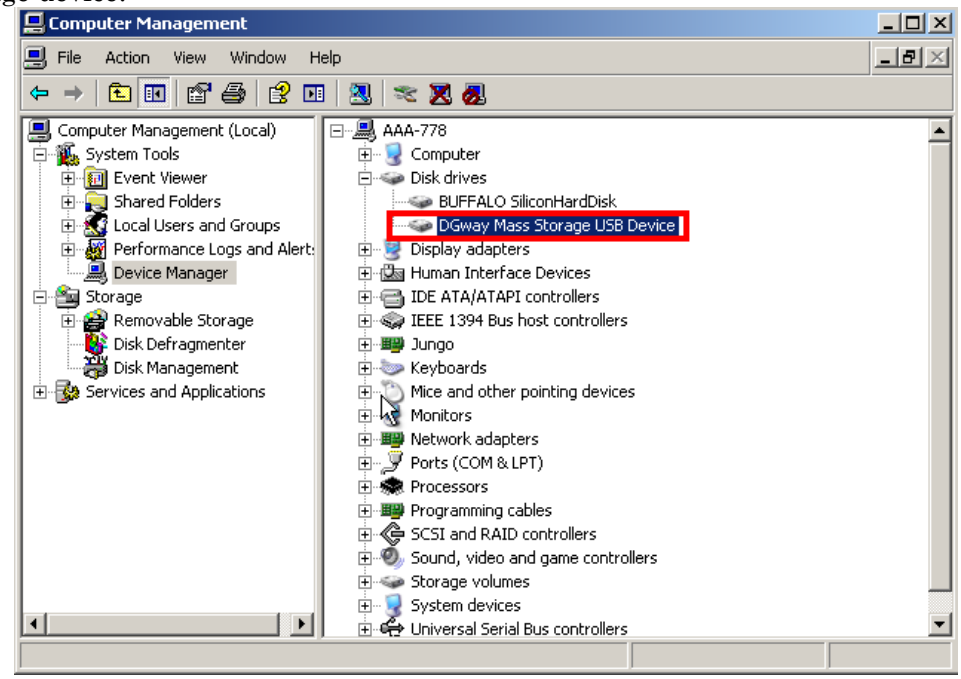

Figure 21: Mass Storage USB Device detected from Device Manager

3. Copy & Paste
   User can execute file or folder Copy&Paste to the demo drive for example.
   Note that drive capacity is limited to 127Mbytes only.

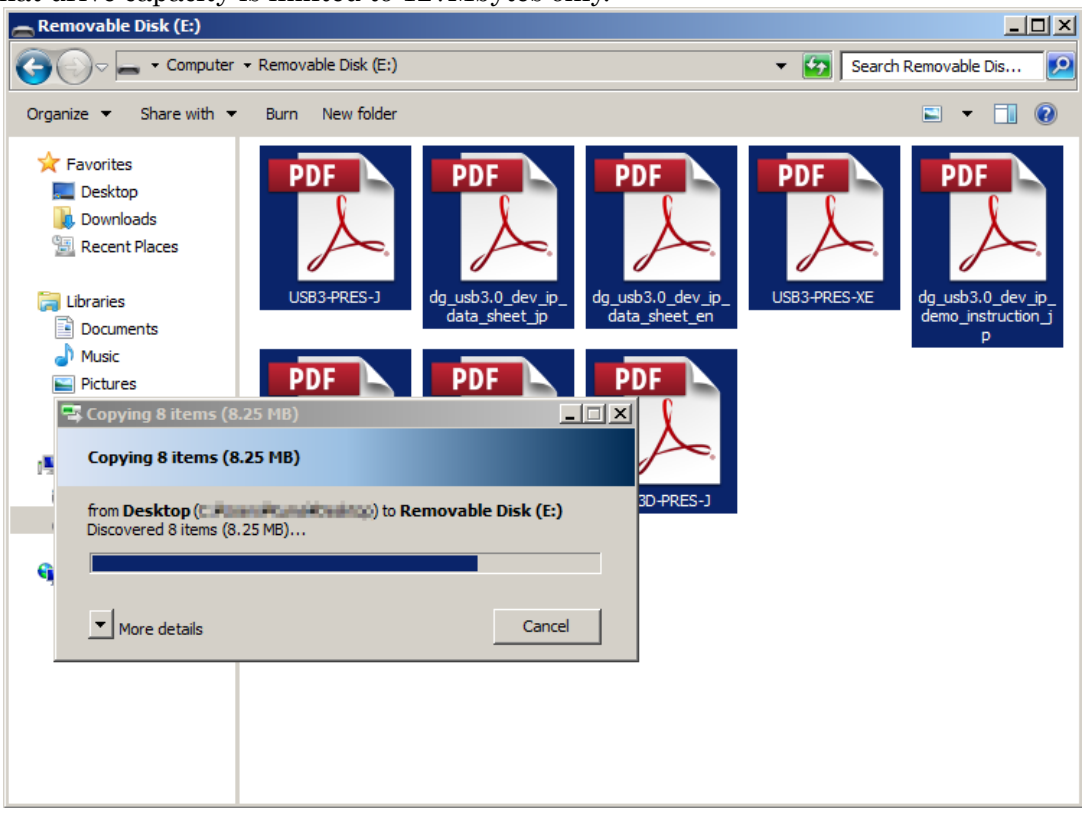

Figure 22: Copy & Paster

4. Benchmark test
   User can execute benchmark test to check performance.
   Note that if HostPC performance is poor (for example of 1-lane PCIe adapter usage or PCIe is GEN1 case), demo drive cannot provide USB3.0 performance. Real transfer performance depends on OS type on the HostPC, CPU performance, and/or PCIe bus speed of the USB3.0 adapter card.

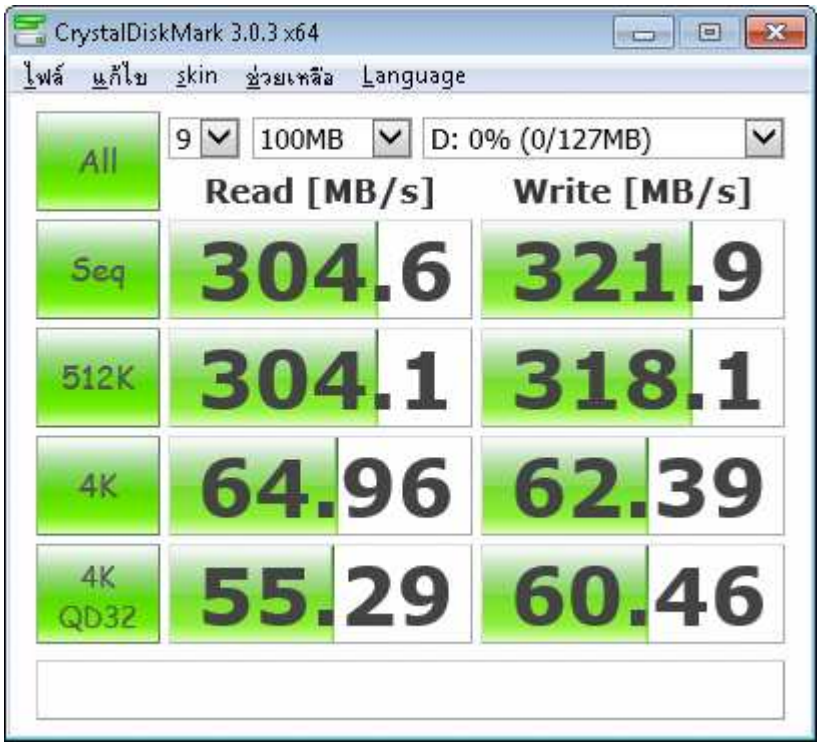

Figure 23: Benchmark test result example

5. Plug-out and Plug-in
   The demo drive can execute plug-out and plug-in operation as a removable disk.
   Take enough intervals between plug-out and plug-in for correct operation.
   If user execute plug-in immediately after plug-out, HostPC may not detect USB3.0 device correctly.

4. Revision History

Revision	Date	Description
1.0	18-Jul-2012	Release English version.
1.1E	04-Mar-2015	Merged both Altera and Xilinx into one document
1.2E	09-Mar-2015	Updated Figure-15 by the latest test result
1.3E	15-May-2015	Add board support