

# tCAM IP Demo Instruction

1	En	ivironment Setup	. 1
2	PC	Setup	. 2
3	FP	PGA board setup	. 4
4	Sig	gnalTap setup.	. 6
	4.1	SignalTap operations	. 6
	4.2	SignalTap trigger condition	. 8
	4.2	2.1 To see Rule Initial Control signals	. 8
	4.2	2.2 To see Rule Memory Interface signals	. 9
	4.2	2.3 To see Input key and Search result signals	10
5	tCA	AMIP demo software	11
	5.1	Demo software interface description	11
	5.2	File format for Rule data and Key Data	12
	5.3	Rule table creation	13
	5.4	Key data table creation	14
	5.5	Initialization rule data to FPGA Development board	15
	5.6	Searching key data	16
	5.7	Compare	18
6	Re	vision History	19



## tCAM IP Demo Instruction

#### Rev1.02 2-Jun-2023

This document describes the instruction to demonstrate the operation of tCAMIP on Arria10SoC development board. This demonstration uses tCAMIP demo software to communicate with development board via 1 Gigabits Ethernet for preparing rule table, initializing tCAMIP, sending keys and reading result data. User is also able to use SignalTap to see the operation of provided signal in FPGA.

## 1 Environment Setup

To operate tCAMIP demo, please prepare following test environment.

- 1) FPGA development boards (Arria10SoC development board)
- 2) Test PC with 1 Gigabits Ethernet connection.
- 3) Micro USB cable for JTAG connection connecting between FPGA development board and PC
- 4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
- 5) Quartus Prime for programming FPGA, installed on Test PC
- 6) File "tCAMIPDemoPack.zip" that included Test Application named "tCAM-IP Demo.exe", configuration file named "tCAMIPTest\_time\_limited.sof" and SignalTap file named "stp1.stp".

(To download this file, please visit our web site at www.design-gateway.com)



Figure 1-1 tCAMIP demo (FPGA<->PC) on Arria10SoC board



## 2 PC Setup

Before running demo, please check the network setting on PC. Ethernet setting is shown as follows.

💺 Network and Sharing Center		
🗧 🔶 👻 🛧 🗱 🤉 Control Pa	nel > Network and Internet > Network a	and Sharing Center
Control Panel Home	View your basic network infor	rmation and set up connections
Change adapter settings	View your active networks	
Change advanced sharing settings	Network Public network	Access type: Internet 2 Connections: <u>Ethernet</u>
	Change your networking settings	
	Figure 2-1 IPv4 settin	<u>la</u>

- 1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
- 2) Click Ethernet icon which is used to connect with FPGA board.

Ethernet Status		× Ethernet Properties
Connection IPv4 Connectivity: IPv6 Connectivity: Media State: Duration:	No Internet access No network access Enabled 01:56:55	Networking         Connect using:       1-Gb LAN connection         Image: Intel(R) Ethemet Connection (7) I219-V         Configure         This connection uses the following items:
Speed: Details Activity Sent	1.0 Gbps	Client for Microsoft Networks  Client for Microsoft Networks  Client for Microsoft Networks  Client for Microsoft Scheduler  Client Protocol Version 4 (TCP/IPv4)  Microsoft Network Adapter Multiplexor Protocol  Microsoft LLDP Protocol Driver  Microsoft LLDP Protocol Version 6 (TCP/IPv6)  Client P
Bytes: 39,299,554	503,073,087	Install Uninstall Properties Description Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks.
	Close	OK Canc

Figure 2-2 Select IP address setting menu

- 3) Click Properties button in Ethernet Status window.
- 4) Select "TCP/IPv4".
- 5) Click Properties button in Ethernet Properties window.



 $\times$ 

tCAM-instruction-intel-en.doc

Internet Protocol Version 4 (TCP/IPv4) Properties

General You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings.					
Obtain an IP address automatical	ly				
• Use the following IP address:	6a				
IP address:	192 . 168 . 11 . 81				
Subnet mask:	255 . 255 . 255 . 0				
Default gateway:					
Obtain DNS server address auton	natically				
Use the following DNS server add	resses:				
Preferred DNS server:					
Alternate DNS server:					
Ualidate settings upon exit	Advanced				
	OK Cancel				

Figure 2-3 Set IP address

6) Set IP address = 192.168.11.81 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.



## 3 FPGA board setup

- 1) Make sure power switch is off and connect power supply to FPGA development board.
- 2) Connect USB cable between FPGA board and PC via micro USB
- 3) Connect CAT5e/CAT6 cable between PC and Ethernet connection of FPGA board. User must use the right port when FPGA board has two 1 Gigabits Ethernet ports.



#### Figure 3-1 Power, Ethernet, and micro USB cable connection

- 4) Power on system.
- 5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
  - a) Click "Hardware Setup..." to select USB-BlasterII [USB-1].
  - b) Click "Auto Detect" and select FPGA device. (10AS066N3).
  - c) Select FPGA device icon.
  - d) Click "Change File" button, select SOF file in pop-up window, and click "open" button
  - e) Check "program"
  - f) Click "Start" button to program FPGA and wait until Progress status is equal to 100%



## Figure 3-2 FPGA Programmer



6) When configuration is completed, Quartus will show popup message of OpenCore Plus as shown in Figure 3-3. Please do not press cancel button, because NiosII in tCAMIP will stop running.



Figure 3-3 OpenCore Plus Status

- 7) When configuration is completed, user can check status LEDs on board as Figure 3-4
  - LED0 is "Ready" status of TOE1G-IP. This LED is on when ethernet connection between PC and board is ready.
  - LED1 is "Connection on" status of TOE1G-IP. This LED is on when software open connection to board.
  - o LED2 is show reset status and relate to hardware reset switch "S10".
  - LED3 is always blink to show clock is working.



Figure 3-4 LEDs status on board



## 4 SignalTap setup

This designed block diagram of this demo is shown as in Figure 4-1. SignalTap is prepared to see all control signals between tCAMIP and user logics design.



Figure 4-1 Demo environment block diagram

#### 4.1 SignalTap operations

Step to use SignalTap II Logic Analyzer is as follows.

- a) Click File -> Open ..., then select file type to SignalTap II Logic Analyzer Files (\*.stp)
- b) Select "stp1.stp", then click Open button as shown in Figure 4-2
- c) As in Figure 4-3, connect FPGA board by select Hardware to USB-BlasterII.
- d) Setup trigger condition to specify signals behavior. Sample of trigger condition and result is shown as in topic 4.2
- e) Click "Run Analysis" button, wait to capture signals from tCAMIP.
- f) The result will be shown, when do SignalTap detect signals same as trigger condition.



#### Figure 4-2 Open file "stp1.stp"



% SignalTap II Logic Analyzer - D:/66.Projects/3	0.ELLM/construction/intel/tCAN	IIPTest - tCAMIPTest - [stp1.stp]*		- 🗆 ×
File Edit View Project Processing Tools Wind	dow Help			Search altera.com
🖷 📒 🤈 ぐ 👫 🏍 🕨 🖏 😮				
Instano 🍡 🔊 🔳 🛅 Ready to acqui	ire			AG Chain Configuration: JTAG readv ×
Instan e Status Enable	ed LEs: 2605 Memory: 19046	Small: 0/18520( Medium: 10/21: Large: 0/0		Hardware: USB-Blasterll [USB-1]
🔝 a 🛛 📶 tap_0 Not running 🗹	2605 cells 190464 bits	0 blocks 10 blocks 0 blocks		
				Device: @1: 10AS066H(1 2 2ES 3 3E2 3  Scan Chain
				>> SOF Manager:
log: Trig @ 2020/08/18 15:45:48 (0:1:2.1 elapsed) #1			click to insert time bar	
Type Alias Name	-8 -7 -6 -	i -4 -3 -2	-1 9 1 2	3 4 5 6 7 8
tCAMIP:u_tCAMIP[keyValid         E-tCAMIP:u_tCAMIP[keyValid         E-tCAMIP:u_tCAMIP[keyData[63_0]	J 0000000b X0100000b	02000000hX0300000hX04000000hX0500000	hX06000000bXFF000000bX00010000bX01010000b	X02010000bX03010000bX04010000bX05010000bX06010000b
tCAMIP:u_tCAMIP resultValid				
E tCAMIP:u_tCAMIP resultData[310]		0000001h	X0000002hX0000003h	X00000004hX00000005hX0000006hX00000007hX0000008hX
	<			
🥦 Data 🛛 🐺 Setup				
Hierarchy Display: × Data Lo	og: 📴			x
✓      ✓      ★ tCAMIPTest     ✓      ★ tCAMIP:u_tCAMIP	o_signaltap_0			
🛃 auto_signaltap_0				0% 00:00:00





#### 4.2 SignalTap trigger condition

On demo running, user is able to use SignalTap to setup trigger condition and check the signal waveform after trigger is detected. The prepared SignalTap signals are separated to 3 parts as (1) Rule Initial control signals, (2) Rule Memory interface signals and (3) Input keys & search result signal respectively.

#### 4.2.1 To see Rule Initial Control signals

Figure 4-4 show trigger condition and Figure 4-5 show sample result from SignalTap when user do initial rule table in topic 5.5

trigg	ger: 20	20/08/18 14:51:37 #1	Lock mode:	子 Allow all ch	anges 👻
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	186	186	1 → Basic AND -
J.			$\checkmark$	$\checkmark$	XXXXh
<b>.</b>			$\checkmark$	$\checkmark$	XXXXXXXXXXh
*•		tCAMIP:u_tCAMIP ruleInit	$\checkmark$	$\checkmark$	1
*•		tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$	
<b>.</b>		tCAMIP:u_tCAMIP ruleAddr[310]	$\checkmark$	$\checkmark$	XXXXXXXXXXh
*•		tCAMIP:u_tCAMIP ruleRdReq	$\checkmark$	$\checkmark$	
*•		tCAMIP:u_tCAMIP ruleRdValid	$\checkmark$	$\checkmark$	
<b>"</b>		tCAMIP:u_tCAMIP ruleData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXXh
<b>_</b>			$\checkmark$	$\checkmark$	Xh
*		tCAMIP:u_tCAMIP keyValid	$\checkmark$	$\checkmark$	
<b>.</b>		tCAMIP:u_tCAMIP keyData[630]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP resultValid	$\checkmark$	$\checkmark$	
-		tCAMIP:u_tCAMIP resultData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXXh

## Figure 4-4 Trigger setup for rule initial control signals

🧚 SignalTap II Logic Analyzer - D:/66.Projects/30.ELLM/construction/intel/tCAMIPTest - [stp1.stp]* - 🗆 X									
Eile Edit View Project Processing Tools Window Help Search altera.com								a.com 🜖	
岡日つで 巻め ト 陰 🛛									
Instance Manager: 🍡 👂 🔳 🔛 Ready to acc	uire					×	JTAG Chain Configuration	n: JTAG ready	×
Instance Status Enal	led LEs: 2605	Memory: 19046 Small: 0/185	20( Medium: 10/2	13 Large: 0/0			Hardwara: LICP Plasta		Cotup
🔝 auto_signaltap_0 Not running 🗸	2605 cells	190464 bits 0 blocks	10 blocks	0 blocks			Hardware. USD-Diaster	ii [030-1] •	Setup
							Device: @1: 10AS00	6H(1 2 2ES 3 3E2 3 -	Scan Chain
							>> SOF Manager:	L ()	
log: Trig @ 2020/08/18 15:54:20 (0:0:10.1 elapsed)				click to	insert time bar				
Type Alias Name	4	948	12 16	20 24	28 32	36	40 44	48 52	56
tCAMIP:u_tCAMIP ruleWidth[150]					0040h				^
E tCAMIP:u_tCAMIP ruleCount[310]				00	001FA3Fh				
tCAMIP:u_tCAMIP/ruleInit									
tCAMIP:u_tCAMIPIruleBusy					0004075				
* CAMIDiu (CAMIDiuleDeDe				UL	JUED IE / N				
tCAMIP:u_tCAMIP/ruleRdReq									
	_			0	0000066				
	<								>
Data Setup									
									~
	Log. 📑								^
V V S tCAMIPTest	o_signaltap_0								
Lauto_signaltap_0									
								0%	00:00:00

#### Figure 4-5 Sample result for rule initial control signals



#### 4.2.2 To see Rule Memory Interface signals

Figure 4-6 show trigger condition and Figure 4-7 show sample result from SignalTap when user do initial rule table in topic 5.5

trigg	ger: 20	20/08/18 15:54:10 #0	Lock mode:	🚽 Allow all ch	anges 👻
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	186	186	1    Basic AND    ▼
6		tCAMIP:u_tCAMIP ruleWidth[150]	$\checkmark$	$\checkmark$	XXXXh
5		tCAMIP:u_tCAMIP ruleCount[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP ruleInit	$\checkmark$	$\checkmark$	
*		tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP ruleAddr[310]	$\checkmark$	$\checkmark$	XXXXXXXXh
×.		tCAMIP:u_tCAMIP ruleRdReq	$\checkmark$	$\checkmark$	1
×.		tCAMIP:u_tCAMIP ruleRdValid	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP ruleData[310]	$\checkmark$	$\checkmark$	XXXXXXXXh
5			$\checkmark$	$\checkmark$	Xh
*		tCAMIP:u_tCAMIP keyValid	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP keyData[630]	$\checkmark$	$\checkmark$	XXXXXXXXh
*		tCAMIP:u_tCAMIP resultValid	$\checkmark$	$\checkmark$	
-		tCAMIP:u_tCAMIP resultData[310]	$\checkmark$	$\checkmark$	XXXXXXXXh

### Figure 4-6 Trigger setup for rule memory signals

📌 SignalTap II Logic Analyzer - D:/66.Projects/30.ELLM/construction/intel/tCAMIPTest - tCAMIPTest - [stp1.stp]* – 🗆 🗙						
Eile Edit View Project Processing Iools Window Help						
瞬  日   つ で   巻 66   ▶ 協  (2)						
Instance Manager: 🍡 🔊 🔳 🔛 Ready to acquire	× JTAG Chain Configuration: JTAG ready ×					
Instance Status Enabled LEs: 2605 Memory: 19046 Small: 0/18520( Medium: 10/21: Large						
🔝 auto_signaltap_0 Not running 🗹 2605 cells 190464 bits 0 blocks 10 blocks 0 bloc	cks					
	Device: @1: 10AS066H(1 2 2ES 3 3E2 3 - Scan Chain					
	SOE Managar					
	U U Wanagel					
log: Ing @ 2020/08/18 15:56:56 (0:0:9:6 elapsed)	Click to insert time bar					
E tokum u cokum pilotvidu [15:0]     E tokum u cokum pilotvidu [15:0]     E tokum u cokum pilotvidu [15:0]	0001FA3Fh					
tcAMIP:u tCAMIP/ruleInit						
LCAMIP.u tCAMIP/ruleBusy						
	0000008h					
tCAMIP:u_tCAMIP/ruleRdReq						
tCAMIP:u_tCAMIP/ruleRdValid						
B-tCAMIP:u_tCAMIP[ruleData[31.0]	0000000h					
B-tCAMIP:u_tCAMIP[ruleStatusCode[3.0]	1h					
tCAMIP:u_tCAMIP[keyValid						
B tCAMIP:u_tCAMIP[keyData[63.0]	0101FF02h					
tCAMIP:u_tCAMIPresultValid						
H - tCAMIP:u_tCAMIP/resultData[310]	0000000h					
<	>					
ጆ Data 🐺 Setup						
Hierarchy Display: × Data Log: 🖻	×					
✓ ✓ ► tCAMIPTest     ✓ ➤ tCAMIP.u_tCAMIP						
B auto_signaltap_0	0% 00:00:00					

### Figure 4-7 Sample result for rule memory signals



#### 4.2.3 To see Input key and Search result signals

Figure 4-8 show trigger condition and Figure 4-9 show sample result from SignalTap when user do initial rule table in topic 5.6

trigg	ger: 20	20/08/18 15:58:58 #0	Lock mode:	🚽 Allow all ch	anges 👻
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	186	186	1 → Basic AND
6		tCAMIP:u_tCAMIP ruleWidth[150]	$\checkmark$	$\checkmark$	XXXXh
1		tCAMIP:u_tCAMIP ruleCount[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP ruleInit	$\checkmark$	$\checkmark$	
*		tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$	
- 😓		tCAMIP:u_tCAMIP ruleAddr[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP ruleRdReq	$\checkmark$	$\checkmark$	
*		tCAMIP:u_tCAMIP ruleRdValid	$\checkmark$	$\checkmark$	
6		tCAMIP:u_tCAMIP ruleData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
6			$\checkmark$	$\checkmark$	Xh
*		tCAMIP:u_tCAMIP keyValid	$\checkmark$	$\checkmark$	1
6			$\checkmark$	$\checkmark$	XXXXXXXXXXh
*		tCAMIP:u_tCAMIP resultValid	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP resultData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh

## Figure 4-8 Trigger setup for input key and searching result

🥕 SignalTap II Logic Analyzer - D:/66.Projects/30.ELLM/construction/intel/tCAMIPTest - tCAMIPTest - [stp1.stp]* - 🗆 X							
Eile Edit View Project Processing Tools Window Help							
Instance Manager: 📉 🔊 🔳 Ready to acquire 🗙 JTAG Chain Configuration:	TAG ready ×						
Instance Status Enabled LEs: 2605 Memory: 19046 Small: 0/18520( Medium: 10/21: Large: 0/0							
R auto signaltad 0 Not running 2505 cells 190464 bits 0 blocks 10 blocks 0 blocks	3B-1] • Setup						
Device: @1: 10AS066	2 2ES 3 3E2 3 - Scan Chain						
	a [						
Sor wanager.							
	1						
log: Ing @ 2020/08/18 15:59-32 (0:0:7.2 elapsed) click to insert time bar	12 14 15						
	1,2 1,4 15						
Commit Comm							
t CAMIP:u CAMIPIruleInit							
LCAMIP.u tCAMIP/ruleBusy							
B - tCAMIP:u tCAMIPIruleAddr[31.0]     000FD1F7h							
LCAMIP:u tCAMIP/ruleRdReg							
LCAMIP:u_tCAMIP(ruleRdValid							
Image: Bet CAMIP:u_CAM							
tCAMIP:u_tCAMIP[keyValid							
■ tCAMIP.u_tCAMIP[keyData[63.0]          0101FF02h%0000000h/01000000h/01000000h/02000000h/030000000h/05000000h/050000000h/050000000h/050000000h/050000000h/050000000h/050000000h/050000000h/0500000h/050000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/05000000h/050000000h/050000000h/0500000000	/10000hX05010000hX06010000h						
tCAMIP:u_tCAMIPIresultValid							
E - tCAMIP:u_tCAMIP:u_tCAMIP:resultData[31.0]     00002CDAh     00000001h/00000002h/00000003h/00000004h/00000005h/(	<u>,00006h</u> X0000007hX0000008h						
<	>						
🗾 Data 🐺 Setup							
nieratory uspay. A Data Log	^						
✓     ✓     CAMIP-lest       ✓     →     tCAMIP:u_tCAMIP							
🔝 auto_signalap_0							

#### Figure 4-9 Sample result for input key and searching result



## 5 tCAMIP demo software

tCAMIP demo software is used for preparing and sending rule and key pattern data to A10SoC board via 1 Gigabits Ethernet connection and getting the result of searching from tCAMIP.

The main features of tCAMIP demo software are as following.

- 1) Rule creation.
- 2) Key creation.
- 3) Initialization rule data table to FPGA development board.
- 4) Search key data and display result.
- 5) Compare expect data of key data searching to result data of key data searching.

#### 5.1 Demo software interface description

-IP Demo		
Rule table	b Key data	Rule width C tCAM-IP version : 1.01
No. A+0 A+1 A+2 A+3 A+4 A+5 A+6 A+7	No. A+0 A+1 A+2 A+3 A+4 A+5 A+6 A+7 Expect Result	Rule width         CAMP vestor         Camp vestor
		Generate from Rule     Stop     Shuffle Key       File     In\software\dataTest\test0001.txt     From File       Hardware Connection     Inital Status: 0     Disconnect       Disconnect     Rule init     Search       Compare     rLatencyCount : 7     f

Figure 5-1 Software interface

Figure 5-1 shows tCAMIP demo software and the description is shown as below.

- a) Rule table is the user rule data display.
- b) Key data table is the user key data display.
- c) Rule width, Users can select data size modes.
- d) Rule Creation, Users can generate rule data table pattern or load rule data table pattern from the file.
- e) Key Creation, Users can generate key data from rule table or load key data table pattern from the file.
- f) Hardware Connection, Users can communicate with FPGA development board in this part. Which consists of connection with board, rule Initialize, key data search, result compare.



#### 5.2 File format for Rule data and Key Data

User can prepare Rule data or Key data file for this demo. The file format is shown as Figure 5-2 and Figure 5-3 for rule width 32-bit and 64-bit respectively.

- 1) The first line is header of file for specific number of byte data in this file like "A+0, A+1, A+2, A+3" for 32-bit file format.
- 2) Next lines are data. The valid range of data is 0-255, others number and 'x' is defined to don't care value.



#### Figure 5-2 Example of load rule file 32-bit

🗯 test0001 8byte 2 tyt - Notenad		····			Rule	table			
	No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7
File Edit Format View Help	1	192	168	11	5	6	7	8	9
A+0, A+1, A+2, A+3, A+4, A+5, A+6, A+7	2	192	168	11	6	6	7	8	10
192, 108, 11, 5, 6, 7, 8, 9 192, 168, 11, 6, 6, 7, 8, 10	3	192	168	11	7	6	7	8	11
192, 168, 11, 7, 6, 7, 8, 11	4	192	168	11	x	6	7	8	12
192, 168, 11, x, 6, 7, 8, 12 193, 168, 10, 4, 6, 7, 8, 12	5	192	168	10	4	6	7	8	13
192, 168, 10, 4, 6, 7, 8, 13 LOAUTUR LADIE HOITTINE	6	192	168	10	3	6	7	8	14
192, 168, 10, x, 6, 7, 8, 15	7	192	168	10	x	6	7	8	15
192, 168, 9, 4, 6, 7, 8, 16 192 168 9 x 6 7 8 17	8	192	168	9	4	6	7	8	16
192, 168, x, 3, 6, 7, x, x	9	192	168	9	v.	6	7	8	17
192, 168, x, x, 6, x, x, x	10	102	100	~	2	6	7	~	~
192, X, X, X, X, X, X, X	11	102	100	<u>^</u>	5	с С		<u>^</u>	<u>^</u>
x, x, x, 1, x, x, x	10	192	100	x	x	0	x	x	x
· · · · · · · · · · · · · · · · · · ·	12	192	x	x	x	x	x	x	x
	13	10	x	x	x	x	x	x	x
	14	x	x	x	1	x	x	x	x

Figure 5-3 Example of load rule file 64-bit



#### 5.3 Rule table creation

To create the rule table, the step is shown as in Figure 5-4.

🖷 tCAM-IP Demo	~
Rule table 3 Key data Rule width 1 tCAM-IP version	n : 1.01
Rule table       3       Key data         No.       A+0       A+1       A+2       A+3       A+4       A+5       A+6       A+7       Expect       Reat       Reat	i :1.01 i tttem File

#### Figure 5-4 Rule creation process

- 1) Select Rule width mode for setup data size.
- 2) Create rule table, the user can select 2 modes as follows.
  - i) Generate rule data table from pattern as show in Figure 5-5.
    - a) Fill out valid range (0-256) of each byte in "Pattern". Byte of pattern position starts "A+0" left to right.
    - b) Click "From Pattern" to start generate rule table.

					Rule	table			
	No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7
	1	0	0	0	0	0	0	0	0
Conorato	rulo toblo 2	0	0	0	0	0	0	0	x
Pattem		0	0	0	0	0	0	x	0
A0 A2 1 5 10 256 [From Dottern]	4	0	0	0	0	0	0	x	x
AU-AS I S IU 230 From Pattern	5	0	0	0	0	0	x	0	0
A4-A7 1 1 1 1	6	0	0	0	0	0	x	0	x
	7	0	0	0	0	0	x	x	0
	8	0	0	0	0	0	x	x	x
	9	0	0	0	0	x	0	0	0
	10	0	0	0	0	x	0	0	x
	11	0	0	0	0	x	0	x	0
	12	0	0	0	0	x	0	x	x
	13	0	0	0	0	x	x	0	0
	14	0	0	0	0	x	x	0	x
	15	0	0	0	0	x	x	x	0





- ii) Load rule data table from the file by click "From File" button to browse and load rule data file.
- 3) When rule is created, rule data show in rule table as shown in Figure 5-5.

#### 5.4 Key data table creation

To create key table, the step is shown as in Figure 5-6.

🚽 tCAM	-IP De	mo																			-	×
				Rule	table				^						Key	data					7 2	Bule width tCAM-IP version : 1.0
No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7			No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7	Expect	Result	
1	x	x	0	0	x	x	0	0			1	255	255	0	0	255	255	0	0	1		64-bit V
2	x	x	0	0	x	x	0	1			2	255	255	0	0	255	255	0	1	2		Rule Creation
3	x	x	0	0	x	x	0	x			3	255	255	0	0	255	255	0	255	3		Pattern
4	x	x	0	0	x	x	x	0			4	255	255	0	0	255	255	255	0	4		A0 - A3 0 0 1 2 From Pattern
5	x	x	0	0	x	x	x	1			5	255	255	0	0	255	255	255	1	5		A4 - A7 0 0 1 2
6	x	x	0	0	x	x	x	x			6	255	255	0	0	255	255	255	255	6		
7	x	x	0	1	x	x	0	0			7	255	255	0	1	255	255	0	0	7		
8	x	x	0	1	x	x	0	1			8	255	255	0	1	255	255	0	1	8	_( i	Key Creation 3
9	x	x	0	1	x	x	0	x			9	255	255	0	1	255	255	0	255	9		Number of key: 36 / 36
10	x	x	0	1	x	x	x	0			10	255	255	0	1	255	255	255	0	10		Generate from Rule Stop Shuffle Key
11	x	x	0	1	x	x	x	1			11	255	255	0	1	255	255	255	1	11		
12	x	x	0	1	x	x	x	x			12	255	255	0	1	255	255	255	255	12		File Tisonware toata test test 000 fort
13	x	x	0	x	x	x	0	0			13	255	255	0	255	255	255	0	0	13		(ii
14	x	x	0	x	x	x	0	1			14	255	255	0	255	255	255	0	1	14		Hardware Connection
15	x	x	0	x	x	x	0	x			15	255	255	0	255	255	255	0	255	15		
16	x	x	0	x	x	x	x	0			16	255	255	0	255	255	255	255	0	16		Disconnect Rule init
17	x	x	0	x	x	x	x	1			17	255	255	0	255	255	255	255	1	17		Search Compare
18	x	x	0	x	x	x	x	x			18	255	255	0	255	255	255	255	255	18		rLatencyCount : 7
19	x	x	x	0	x	x	0	0			19	255	255	255	0	255	255	0	0	19		
20	x	x	x	0	x	x	0	1			20	255	255	255	0	255	255	0	1	20		
21	x	x	x	0	x	x	0	x			21	255	255	255	0	255	255	0	255	21		
22	x	x	x	0	x	x	x	0			22	255	255	255	0	255	255	255	0	22		
23	x	x	x	0	x	x	x	1			23	255	255	255	0	255	255	255	1	23		
24	x	x	x	0	x	x	x	x			24	255	255	255	0	255	255	255	255	24		
25	x	x	x	1	x	x	0	0			25	255	255	255	1	255	255	0	0	25		
26	x	x	x	1	x	x	0	1			26	255	255	255	1	255	255	0	1	26		
27	x	x	x	1	x	x	0	x			27	255	255	255	1	255	255	0	255	27		
							-		$\sim$	-		_	_	_	-	_		-		-		

#### Figure 5-6 Key creation

- 1) Create Key data, the user can select 2 modes as follows
  - i) Generate key data from rule table.
    - a) Click "Generate from Rule" to start generate key data.
    - b) "Number of key: X / Y" is progress status by X is progress number of key and Y is total number of keys from all combination of rules. (generating time depends on the amount of key data)
    - c) "Stop" button is used for stop key generating.
  - ii) Load key data from the file by click "From File" button to browse and load rule data file.
- 2) When key data is created, the expect value will be generated automatically.
- 3) "Shuffle Key" button is used to shuffle each key in key table randomly.



#### 5.5 Initialization rule data to FPGA Development board

The step to initialize rule data is following as below and Figure 5-7.

- 1) Please make sure that LED0 (TOE1G ready) is on (please refer LEDs on board in Figure 3-4), before click "Connect" button.
- When connection is completed, the text of the button will change to "Disconnect" and LED1 (open connection status) is turn on. The button "Rule init", "Search" and "Compare" will enable.
- 3) On SignalTap, setup trigger condition when ruleInit = '1' and other signals are don't care. Then press "Run Analysis" button.
- 4) Click "Rule init" button to initialize data of rule table. Initialization duration time depends on the amount of key data.

"Initial Status: X" is active status for Rule transfer, Rule verify, Rule initial and Status code. By X is running number of rule table, time count of Rule initial status and status code which shows that process is still running)

- When ruleInit signal = '1', SignalTap will show all interface signals of tCAMIP.
- In case to see the difference trigger point, user can change trigger condition in SignalTap on step 3).
- 5) When initialization is completed, the message box will popup "Rule initial completed". In case initialization is incomplete, "Initial Status:" is shown error message of status code.

				Rule	table				^					Key	data						^	Dute with tCAM-IP versio
No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7		No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7	Expect	Result		Rule width
1	x	x	0	0	x	x	0	0		1	255	255	0	0	255	255	0	0	1			64-bit 🗸
2	x	x	0	0	x	x	0	1		2	255	255	0	0	255	255	0	1	2			Pula Crastian
3	x	x	0	0	x	x	0	x		3	255	255	0	0	255	255	0	255	3			Pattern
4	x	x	0	0	x	x	x	0		4	255	255	0	0	255	255	255	0	4			A0 - A3 0 0 1 2 From Pa
5	x	x	0	0	x	x	x	1		5	255	255	0	0	255	255	255	1	5			A4 - A7 0 0 1 2
6	x	x	0	0	x	x	x	x		6	255	255	0	0	255	255	255	255	6			
7	x	x	0	1	x	x	0	0		7	255	255	0	1	255	255	0	0	7			File 1\software\dataTest\test0001.txt From F
8	x	x	0	1	x	x	0	1		8	255	255	0	1	255	255	0	1	8			Key Creation
9	x	x	0	1	x	x	0	x		9	255	255	0	1	255	255	0	255	9			Number of key : 36 / 36
10	x	x	0	1	x	x	x	0		10	255	255	0	1	255	255	255	0	10			Generate from Rule Stop Shuffle
11	x	x	0	1	x	x	x	1		11	255	255	0	1	255	255	255	1	11			
12	x	x	0	1	x	x	x	x		12	255	255	0	1	255	255	255	255	12			File <u>n\software\dataTest\testUUUT.txt</u> From
13	x	x	0	x	x	x	0	0		13	255	255	0	255	255	255	0	0	13			
14	x	x	0	x	x	x	0	1		14	255	255	0	255	255	255	0	1	14	1		Hardware Connection
15	x	x	0	x	x	x	0	x		15	255	255	0	255	255	255	0	255	15		1	Inital Status: 0
16	x	x	0	x	x	x	x	0		16	255	255	0	255	255	255	255	0	16			Disconnect Rule init
17	x	x	0	x	x	x	x	1		17	255	255	0	255	255	255	255	1	17			Search Compare
18	x	x	0	x	x	x	x	x		18	255	255	0	255	255	255	255	255	18			rLatencyCount : 7
19	x	x	x	0	x	x	0	0		19	255	255	255	0	255	255	0	0	19			
20	x	x	x	0	x	x	0	1		20	255	255	255	0	255	255	0	1	20			
21	x	x	x	0	x	x	0	x		21	255	255	255	0	255	255	0	255	21			
22	x	x	x	0	x	x	x	0		22	255	255	255	0	255	255	255	0	22			
23	x	x	x	0	x	x	x	1		23	255	255	255	0	255	255	255	1	23			
24	x	x	x	0	x	x	x	x		24	255	255	255	0	255	255	255	255	24			
25	x	x	x	1	x	x	0	0		25	255	255	255	1	255	255	0	0	25			
26	x	x	x	1	x	x	0	1		26	255	255	255	1	255	255	0	1	26			
27	x	x	x	1	x	x	0	x		27	255	255	255	1	255	255	0	255	27			

Figure 5-7 Rule initialization



#### 5.6 Searching key data

To search key data by the hardware of tCAMIP demo, the step is following as below and Figure 5-8.

- 1) On SignalTap, setup trigger condition when keyValid = '1' and other signals are don't care. Then press "Run Analysis" button.
- 2) Click "Search" button to run key data searching.
- 3) When search is completed, the message box will popup "Search completed"
  - SignalTap will show all signals interface of tCAMIP as shown in Figure 5-9
  - In case to see the different trigger point, user can change trigger condition in SignalTap on step 1).
- 4) Result of key search will be displayed to 'Result' column. "rLantencyCount: X" show number of clocks between first key data to first result data.

🖷 tCAM	I-IP De	mo																			×
				Rule	e table				^					Key	data					$\square$	4 tCAM-IP version : 1.01
No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7		No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7	Expect	Result	Color Color
1	x	x	0	0	x	x	0	0		1	255	255	0	0	255	255	0	0	1	1	64-bit V
2	x	x	0	0	x	x	0	1		2	255	255	0	0	255	255	0	1	2	2	Rule Creation
3	x	x	0	0	x	x	0	x		3	255	255	0	0	255	255	0	255	3	3	Pattern
4	x	x	0	0	x	x	x	0		4	255	255	0	0	255	255	255	0	4	4	A0 - A3 0 0 1 2 From Pattern
5	x	x	0	0	x	x	x	1		5	255	255	0	0	255	255	255	1	5	5	A4 - A7 0 0 1 2
6	x	x	0	0	x	x	x	x		6	255	255	0	0	255	255	255	255	6	6	
7	x	x	0	1	x	x	0	0		7	255	255	0	1	255	255	0	0	7	7	File 1\software\dataTest\test000T.txt From File
8	x	x	0	1	x	x	0	1		8	255	255	0	1	255	255	0	1	8	8	Key Creation
9	x	x	0	1	x	x	0	x		9	255	255	0	1	255	255	0	255	9	9	Number of key: 36 / 36
10	x	x	0	1	x	x	x	0		10	255	255	0	1	255	255	255	0	10	10	Generate from Rule Stop Shuffle Key
11	x	x	0	1	x	x	x	1		11	255	255	0	1	255	255	255	1	11	11	
12	x	x	0	1	x	x	x	x		12	255	255	0	1	255	255	255	255	12	12	File n\software\dataTest\test0001.txt From File
13	x	x	0	x	x	x	0	0		13	255	255	0	255	255	255	0	0	13	13	
14	x	x	0	x	x	x	0	1		14	255	255	0	255	255	255	0	1	14	14	Hardware Connection
15	x	x	0	x	x	x	0	x		15	255	255	0	255	255	255	0	255	15	15	Status code mpleted)
16	x	x	0	x	x	x	x	0		16	255	255	0	255	255	255	255	0	16	16	Disconne Rule init
17	x	x	0	x	x	x	x	1		17	255	255	0	255	255	255	255	1	17	17	Search Compare
18	x	x	0	x	x	x	x	x		18	255	255	0	255	255	255	255	255	18	18	rLatencyCount : 7
19	x	x	x	0	x	x	0	0		19	255	255	255	0	255	255	0	0	19	19	
20	x	x	x	0	x	x	0	1		20	255	255	255	0	255	255	0	1	20	20	
21	x	x	x	0	x	x	0	x		21	255	255	255	0	255	255	0	255	21	21	
22	x	x	x	0	x	x	x	0		22	255	255	255	0	255	255	255	0	22	22	
23	x	x	x	0	x	x	x	1		23	255	255	255	0	255	255	255	1	23	23	
24	x	x	x	0	x	x	x	x		24	255	255	255	0	255	255	255	255	24	24	
25	x	x	x	1	x	x	0	0		25	255	255	255	1	255	255	0	0	25	25	
26	x	x	x	1	x	x	0	1		26	255	255	255	1	255	255	0	1	26	26	
27	x	x	x	1	x	x	0	x		27	255	255	255	1	255	255	0	255	27	27	
		-		-			-		~	-							-				

Figure 5-8 Search key data



% SignalTap II Logic Ana File Edit View Project	lyzer - D:/66.Pro Processing Too	jects/30.ELL ols Window	M/constructio	n/intel/tCAMIPT	est - tCAMIPTes	t - [stp1.stp]*						Search al	L tera.com	×
🖼   つ で   👫 🐽	Þ 🖏 😗													
Instance Manager: 🍡 🔊	a 🔛 Read	dy to acquire							×	JTAG CH	nain Configuratio	on: JTAG ready		×
Instance	Status	Enabled	LEs: 1183	Memory: 16896	Small: 0/185200	Medium: 2/2131	Large: 0/0			Hardwar	e: USB-Blaste	rll (USB-11	- Se	tup
🔝 auto_signaltap_0	Not running		1183 cells	16896 bits	0 blocks	2 blocks	0 blocks			Device:	@1: 10AS0	56H(1 2 2ES 3 3E2 3	• Scar	1 Chain
log: Trig @ 2020/05/26 14:	23:43 (0:0:4.7 elap	psed) #1					cli	ck to insert time bar						
Type Alias	Name IIDIko A (alid	-2	-1	9 1	2	3 4	ş	Ģ	7 8	9	1 <u>0</u>	1,1 1,2	13	14
E tCAMIP:u_tC	AMIP[keyData[31]	.0]	0006310Ah	X00000000hXFF	000000hX0001000	00h/FF010000h/(	00020000h)(FFI	020000hX00030000H	XFF030000hX000400	00h)(FF040	000h\00050000	hXFF050000hX000600	00hXFF06	;0000h)
tCAMIP:u_tCAM	11P resultValid AMIP resultData[3	310]			0000526	SDh				02h)(00000)	003h)(00000004	hX00000005hX000000	06h)(0000	0007h
		<												>
🧯 Data 🛛 🐺 Setup														
Hierarchy Display:	×	Data Log:	<b>P</b>											×
<ul> <li>✓ ✓ ➤ tCAMIPTest</li> <li>✓ ➤ tCAMIP:u_tCA</li> </ul>	MIP	🛃 auto_sig	gnaltap_0											
🕄 auto_signaltap_0													0% 0	0:00:00 .:

Figure 5-9 Sample of SignalTap result



#### 5.7 Compare

To compare between the expected value (from software) and result from hardware searching, the step is as shown in Figure 5-10.

- 1) Click "Compare" button to compare expect data and result data of key data.
- 2) When comparing is completed, if compare have mismatch. The message box will popup "Completed with X mismatch found", By X is number of mismatches found.

	-IF De	mo																				- L ^
				Rule	table				^					Key	data						^	Rule width tCAM-IP version : 1.01
No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7		No.	A+0	A+1	A+2	A+3	A+4	A+5	A+6	A+7	Expect	Result		C4 ha
1	x	x	0	0	x	x	0	0		1	255	255	0	0	255	255	0	0	1	1		0410it V
2	x	x	0	0	x	x	0	1		2	255	255	0	0	255	255	0	1	2	2		Rule Creation
3	x	x	0	0	x	x	0	x		3	255	255	0	0	255	255	0	255	3	3		Pattem
4	x	x	0	0	x	x	x	0		4	255	255	0	0	255	255	255	0	4	4		A0 - A3 0 0 1 2 From Pattern
5	x	x	0	0	x	x	x	1		5	255	255	0	0	255	255	255	1	5	5		A4 - A7 0 0 1 2
6	x	x	0	0	x	x	x	x		6	255	255	0	0	255	255	255	255	6	6		
7	x	x	0	1	x	x	0	0		7	255	255	0	1	255	255	0	0	7	7		
8	x	x	0	1	x	x	0	1		8	255	255	0	1	255	255	0	1	8	8		Key Creation
9	x	x	0	1	x	x	0	x		9	255	255	0	1	255	255	0	255	9	9		Number of key : 36 / 36
10	x	x	0	1	x	x	x	0		10	255	255	0	1	255	255	255	0	10	10		Generate from Rule Stop Shuffle Key
11	x	x	0	1	x	x	x	1		11	255	255	0	1	255	255	255	1	11	11		File
12	x	x	0	1	x	x	x	x		12	255	255	0	1	255	255	255	255	12	12		
13	x	x	0	x	x	x	0	0		13	255	255	0	255	255	255	0	0	13	13		
14	x	x	0	x	x	x	0	1		14	255	255	0	255	255	255	0	1	14	14		Hardware Connection
15	x	x	0	x	x	x	0	x		15	255	255	0	255	255	255	0	255	15	15		
16	x	x	0	x	x	x	x	0		16	255	255	0	255	255	255	255	0	16	16		Disconnect Rule init
17	x	x	0	x	x	x	x	1		17	255	255	0	255	255	255	255	1	17	17		Search Compare
18	x	x	0	x	x	x	x	x		18	255	255	0	255	255	255	255	255	18	18		rLatencyCount : 7
19	x	x	x	0	x	x	0	0		19	255	255	255	0	255	255	0	0	19	19		
20	x	x	x	0	x	x	0	1		20	255	255	255	0	255	255	0	1	20	20		
21	x	x	x	0	x	x	0	x		21	255	255	255	0	255	255	0	255	21	21		
22	x	x	x	0	x	x	x	0		22	255	255	255	0	255	255	255	0	22	22		
23	x	x	x	0	x	x	x	1		23	255	255	255	0	255	255	255	1	23	23		
24	x	x	x	0	x	x	x	x		24	255	255	255	0	255	255	255	255	24	24		
25	x	x	x	1	x	x	0	0		25	255	255	255	1	255	255	0	0	25	25		
26	x	x	x	1	x	x	0	1		26	255	255	255	1	255	255	0	1	26	26		
27	x	x	x	1	x	x	0	x	$\checkmark$	27	255	255	255	1	255	255	0	255	27	27	~	

Figure 5-10 Step to compare data.



## 6 Revision History

Revision	Date	Description
1.02	5-Mar-2021	Revise
1.01	25-Aug-2020	Support up to 64-bit width of rule
1.00	4-Jun-2020	Initial version release