

tCAM IP Search Replace Demo Instruction

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tCAM IP Search Replace Demo Instruction

Rev1.00 1-Sep-2023

This document describes the instruction to demonstrate the operation of tCAMIP on Agilex7 I-series development kit. This demonstration shows search/replace text function by using tCAMIP. User is also able to use SignalTap to see the operation of provided signals in FPGA.

1 Environment Setup

To operate tCAMIP demo, please prepare following test environment.

- 1) FPGA development boards (Agilex7 I-series development kit)
- 2) Test PC.
- 3) Micro USB cable for JTAG connection between FPGA development board and Test PC
- 4) Quartus programmer for programming FPGA, installed on Test PC
- 5) SOF file named "tCAMIP.sof" (To download these files, please visit our web site at www.design-gateway.com)



Figure 1-1 tCAMIP demo on Agilex7 I-series board



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2 FPGA development board setup

- 1) Make sure power switch is off and connect power supply to FPGA development board.
- 2) Connect USB cables between FPGA board and PC via micro-USB ports.
- 3) Turn on power switch for FPGA board.
- 4) Open Quartus Programmer to program FPGA through USB-1 by following step.
 - i) Click "Hardware Setup..." to select
 - AGI FPGA Development Kit [USB-1] for Agilex7 I-series
 - ii) Click "Auto Detect" and select FPGA number.
 - iii) Select FPGA device icon (Agilex or A10SoC).
 - iv) Click "Change File" button, select SOF file in pop-up window and click "open" button.
 - v) Check "program".
 - vi) Click "Start" button to program FPGA.
 - vii) Wait until Progress status is equal to 100%.

🖖 Programmer - C:/Users/taksa/Desktop/tCAM/NoSTP/AGIB027/intel/tCAMIPTest - tCAMIPTest - [tCAMIPTest.cdf]* — 🗌 🗙										
Eile Window Help i) Click Hardware Setup -> USB-1 FPGA FPGA										
Hardware Setup										
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vi ▶™Start	File	Device	Checksum	Usercode	Program/ Configure	Verify Blank-	Examine	Security Bit	Erase	ISP CLAMP
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ii <none></none>		1_BIT_TAP VTAP10	000000000000000000000000000000000000000	<none> <none></none></none>	Ч	v) Check "Progr	am"			
× Delete										
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Add Device	itel.	intel	_							
t [™] Up										
Down ↓ TDAGIB02	7R29AR3 1_BIT_	TAP VTAP10								

Figure 2-1 FPGA Programmer for Agilex



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- 5) When configuration is completed, user can check status LEDs on board as Figure 2-2.
 - LED0 is show reset status, This LED is on when the reset signal is not active.
 - LED1 is show "Ready" status of Search Replace Module.
 - LED2 is show Error status, This LED is on when an error is detected.
 - LED3 is always blink to show dataInValid is working.



Figure 2-2 LED[3:0] status on board



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3 SignalTap Logic Analyzer

Block diagram of the tCAMIP demonstration is shown as in Figure 3-1. SignalTap is prepared to show waveform of input and output of tCAMIP in FPGA. User can set trigger condition to show the desired waveform.



Figure 3-1 tCAMIP Demo block diagram

3.1 SignalTap operations

Step to use Signal Tap Logic Analyzer is as follows.

- a) Click File -> Open ..., then select file type to Signal Tap Logic Analyzer Files (*.stp)
- b) Select "stp1.stp", then click Open button as shown in Figure 3-2
- c) As in Figure 3-3, select Hardware to AGI FPGA Development Kit.
- d) Setup trigger condition to specify signals behavior. Sample of trigger condition and result is shown as in topic 3.2
- e) Click "Run Analysis" button, wait to capture signals from tCAMIP.
- f) The result will be shown, when do SignalTap detect signals same as trigger condition.



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Open File					×		
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File <u>n</u> ar	Add file to current project	Open as:	Auto	Output Fil Power and Design As All Files (*. cignal Tap	tes (*.qmsg *.vo *.vho *.tdo *.sc d Thermal Calculator Files (*.ptc, sistant Waiver Files (*.dawf) *) Logic Analyzer Files (*.stp)		

Figure 3-2 Open file "stp1.stp"

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Elle Edit View Project Processing Tools Window Help					
	A 2				
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Instance Status Enabled		C ardware: AGLERGA Development Kit [USP-1]	* Cotup		
auto_signaltap Not running 🗸			T Gran Chain		
		Bridge index: None detected	Scan chain		
		SOE Managerr + Son/tCAM/Data//alid/ACIP027/intel/outp	ut files/tCAMIPTest sof		
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log-Trig @ 2023/07/10 13:42:20 (0:0:0:1 clapsed) #1	-64 -32 0 32 64	Click to insert time bar 96 128 160 192 224 256 299 220	352 384		
Pre-Syn c SRIu tCAMIPIkeValid	345				
Pre-Syn * C SR[u tCAMIP[keyData]630]					
Pre-Syn C SR resultData[310] Pre-Syn C SR u tCAMIP ruleAddr[310]		0000165Fh			
Pre-Syn c SRIu tCAMIPIruleRdReg					
Pre-Syn C SR[u tCAMIP[ruleData[80]		100h 0040b			
Pre-Syn © c SR(u tCAMP) rule would 13.0]		000002CCh			
Pre-Syn c SR u tCAMIP ruleInit Pre-Syn c SR u tCAMIP ruleBusy					
Pre-Syn		1h	(f		
🔁 Data 🚾 Setup					
Hierarchy Display: X Data Log: V V tCAMIP V CAMIP			X		
🔜 auto_signaltap_0					
Run the Signal Tap Logic Analyzer in continuous acquisition and up	date mode				

Figure 3-3 SignalTap II Logic Analyzer



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3.2 SignalTap trigger condition

On demo running, user is able to use SignalTap to setup trigger condition and check the signal waveform after trigger is detected. The provided SignalTap signals can be triggered based on Input keys & search result signal.

3.2.1 To see Input key and Search result signals

Figure 3-4 show trigger condition and Figure 3-5 show sample result from SignalTap when user search key data.

Node Data Enable Trigger Enable Trigger Conc						
Type Alias Tap 💡			Name	195	195	1 V Basic AND
C -		Pre-Syn	c SR u tCAMIP keyValid	✓	✓	<u>_</u>
_		Pre-Syn	■ c SR u tCAMIP keyData[630]	✓	\checkmark	XXXXXXXXXXXXXXXX
C		Pre-Syn	c SR resultValid	✓	\checkmark	×
_		Pre-Syn		✓	\checkmark	XXXXXXXh
_		Pre-Syn	■ c SR u tCAMIP ruleAddr[310]	✓	✓	XXXXXXXh
C _		Pre-Syn	c SR u tCAMIP ruleRdReg	✓	✓	×
C		Pre-Syn	c SR u tCAMIP ruleRdValid	✓	\checkmark	×
C and a second s		Pre-Syn		✓	✓	XXXh
_		Pre-Syn	■ c SR u tCAMIP ruleWidth[150]	✓	✓	XXXXh
_		Pre-Syn		✓	✓	XXXXXXXh
C		Pre-Syn	c SR u tCAMIP ruleInit	✓	✓	×
C -		Pre-Syn	c SR u tCAMIP ruleBusy	✓	✓	X
		Pre-Syn	■ c SR u tCAMIP ruleStatusCode[30]	✓	✓	Xh

Figure 3-4 Trigger setup for input key and searching result



Figure 3-5 Sample result for input key and searching result



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4 Revision History

Revision	Date	Description
1.00	21-Jun-2023	Initial version release