

# IP Lock User's Manual

Design Gateway Co.,Ltd.

*Rev 1.6*

*(PD0601-6-01-06E)*

\*\*\* Please read this manual carefully before using IP Lock \*\*\*



## Revision History

Revision	Date	Detail of change
1.0	10 May 2006	Initial Release
1.1	1 August 2006	Adding IP lock core for Altera FPGA.
1.2	14 November 2006	Update detail of setting internal pull-up on ISE Update detail of SC0 signal
1.3	8 November 2007	Support Xilinx Virtex5 Adding Troubleshooting
1.4	30 December 2009	Update resource usage on Xilinx
1.5	6 August 2010	Update Figure 4-1 and 4-8
1.6	15 October 2010	Update Device support

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## 1. Introduction

Thank you very much for purchasing IP Lock. Please check that all the following items are in the box. If anything is missing or damaged, contact your distributor or Design Gateway Co.,Ltd.

1. IP Lock writer
2. User's manual
3. IP Lock device 3 pcs.
4. USB cable
5. CD ROM contains :
  - IP Lock software
  - IP Lock user's manual
  - IP Lock core for Xilinx (TopIPLock.vhd, iplock.ngc and iplockex.ngo)
  - IP Lock core for Altera (TopIPLock.vhd, iplock.vhd)
  - Example VHDL design source codes ( Counter.vhd, Counter32Bits.vhd)
  - Device driver (dgmchpusb.inf and dgmchpusb.sys)

### 1.1. Specifications

1. 128-bit AES encryption
2. Resource : about 400 slices / 2 Block RAM on Xilinx FPGA, about 1200LE/ about 24,500 memory bit on Altera FPGA
3. IP Lock core and IP Lock device sent and receive data for checking every 200 msec.
4. Xilinx FPGA support only Spartan2, Spartan2E, Spartan3, Spartan3E, Spartan6, Virtex, Virtex2, Virtex2Pro, Virtex4, Virtex5 and Virtex6
5. Altera FPGA support only Stratix, Stratix2, Stratix3, Stratix4, ArriaGX, Arria2GX, Cyclone Cyclone2 and Cyclone3

## 1.2. Minimum System Requirement

1. Pentium III or compatible processor
2. RAM 256 MB
3. Windows XP
4. Xilinx ISE 7.1 or over for Xilinx FPGA designer
5. Quartus II 4.1 or over for Altera FPGA designer
6. 1 Port USB

## 1.3. Caution

Please be careful this information when using IP Lock.

1. Please write user's ID to IP Lock devices by IP Lock writer because user's ID was not written from shipment
2. Please use IP Lock core and IP Lock writer from same package because IP Lock writer has unique writer's ID. So if user writes same user's ID from different IP Lock writer, ID on IP Lock device will mismatch from IP Lock core.
3. Please be careful mounting direction of IP Lock device.
4. Please be careful static electricity when mounting IP Lock device to board.
5. Voltage range of IP Lock device is +2.5V or +3.3V. Please be careful to supply voltage to it.
6. For Altera FPGA, user must register to Design Gateway Co.,Ltd for request license file.

## 1.4. Qualifications

1. Design Gateway Co.,Ltd do not guarantee quality of IP Lock If user re-model by your self
2. Design Gateway Co.,Ltd recommend user to evaluate IP Lock by using IP Lock Laboratories pack and evaluation board before using IP Lock in mass production.

### 1.5. Warranty Policy

1. Product warranty is valid for 1 year from purchasing date.
2. Warranty is void if any modification has been made to this product and any incorrect operation from this manual or warranty sticker is torn or damaged.
3. In order to claim for product exchange or technical support within warranty period, official receipt is required for unregistered customer as an evidence of purchasing whereas official receipt is unnecessary for registered customer (please fill up registration card attached herewith the product and send back to Design Gateway Co.,Ltd).

### 1.6. Customer Support

Customer can contact to [support@design-gateway.com](mailto:support@design-gateway.com) for support of any problem about IP Lock or visit our website at [www.design-gateway.com](http://www.design-gateway.com).

Your Personal information will be restricted with high confidentiality.

## 2. IP Lock System

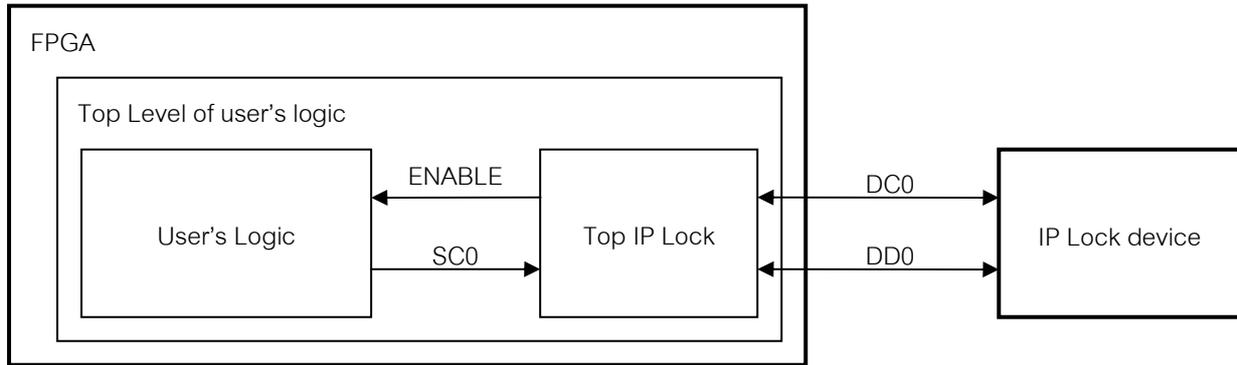


Figure 2-1 IP Lock System

From above block diagram, it is shown IP Lock system. IP Lock core communicate with IP Lock device for check user's ID. If user's ID is correct, ENABLE signal is logic '1' (enable). On the other hand, if user's ID is not correct, ENABLE signal is logic '0' (disable). User can use ENABLE signal from IP Lock core to enable user's logic. In IP Lock core, user can set user's ID (USERID) in HDL code. In IP Lock device, user can set user's ID to IP Lock device via IP Lock software. Both of them must be same value.

IP Lock core use 3 signals for active. That is SC0, DC0 and DD0. SC0 signal is system clock for IP Lock core. It use internal clock from user's logic but *SC0 must have frequency range between 1-25 MHz*. DC0 and DD0 signal is data signal. It use for communicate between IP Lock core and IP Lock device.

Because ENABLE signal from Top IP Lock does not synchronous with user's clock so user should be add a D Flip-Flop in user's logic as show in Figure 2-2 ENABLE signal that out from D Flip-Flop is synchronous with user's clock in user's logic.

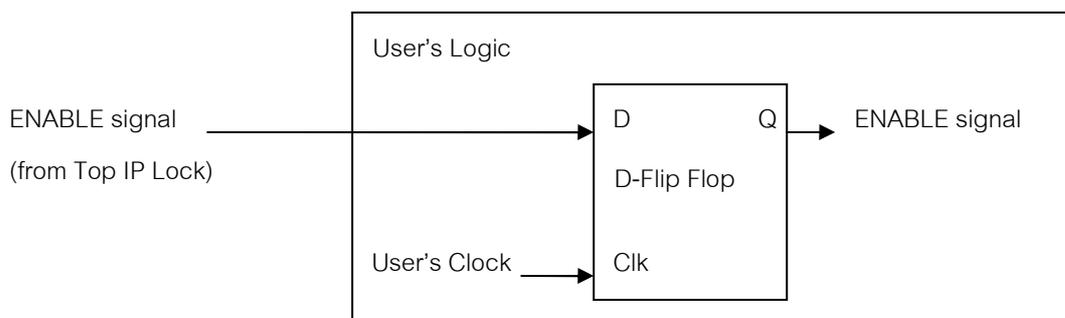


Figure 2-2 Recommend logic on ENABLE signal

### 3. IP Lock core

#### 3.1. IP Lock core for Xilinx FPGA

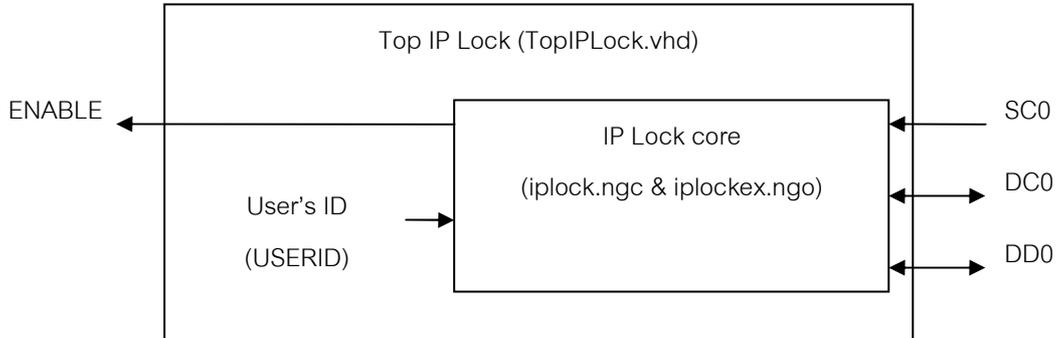


Figure 3-1 Top level of IP Lock for Xilinx FPGA

Figure 3-1 shows block diagram of top level IP Lock for Xilinx FPGA.

- Xilinx IP Lock core (iplock.ngc and iplockex.ngo): IP Lock core communicate with IP Lock device for check user's ID before enable ENABLE signal. If communication between IP Lock core and IP Lock device failed or user's ID is not same value, IP Lock will disable ENABLE signal.
- User must copy iplock.ngc and iplockex.ngo to Xilinx project folder before start synthesis and implement HDL code
- User's ID value (USERID) can set in HDL code and it must be same value with user's ID in IP Lock device.

#### 3.2. IP Lock core for Altera FPGA

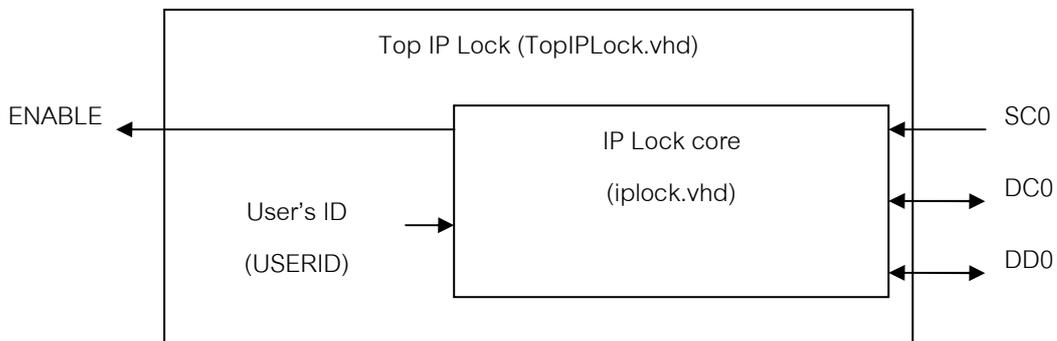


Figure 3-2 Top level of IP Lock for Altera FPGA

Figure 3-2 shows block diagram of top level IP Lock for Altera FPGA.

- Altera IP Lock core (iplock.vhd): IP Lock core communicate with IP Lock device for check user's ID before enable ENABLE signal. If communication between IP Lock core and IP Lock device failed or user's ID is not same value, IP Lock will disable ENABLE signal.
- User's ID value (USERID) can set in HDL code and it must be same value with user's ID in IP Lock device.
- User must add IP Lock license into Quartus II license as show in Figure 3-3 before start synthesis and implement HDL code, If user does not have IP Lock license, User can not synthesis and implement IP Lock core.
- IP Lock license file: user must send email to [iplock@design-gateway.com](mailto:iplock@design-gateway.com) for request IP Lock license and Design Gateway Co.,Ltd request some information for register as shown in Figure 3-4. Please fill this information in email.
- User can check Volume Serial Number by run DOS prompt and use command "dir" on window drive as shown in Figure 3-5 .

```

license.dat - Notepad
File Edit Format View Help
# QuartusII license

# Start QuartusII license
.....

.....

.....

.....

.....

.....

# End QuartusII license

# Start IPLock license

INCREMENT 7D50_0001 alterad 9999.12 permanent uncounted 31B7BA09499F \

VENDOR_STRING="Jdjgic1884kNhsZK42qPqJwV3SaZDt0EcGUk8RtGWTQhctNYgcSOLyIuj62EN1GfQmQOZcYE1us0cBNoXZ9JPFaZI
KQm9TDFQP4utVOGJzHpg8QHdQBESFy8WVGjZAQwU$J8vz88cRyl$6" \
  HOSTID=DISK_SERIAL_NUM=8c27bac5 SIGN="1416 E439 BF41 68BC 9C8F \
  DDD6 4842 399B CF56 6728 0B92 99B5 B9A1 D69D E933 0910 C269 \
  0260 C32F 0583 E6CB C962 C50F 4812 CB0F 489C 2D30 B9F7 532A \
  5240"

# End IPLock license
  
```

Figure 3-3 IP Lock license in Quartus II license

Name / Company: .....
IP Lock Serial Number: .....
Volume Serial Number: .....
Address: .....
Tel: .....
Fax: .....

Figure 3-4 Information for register

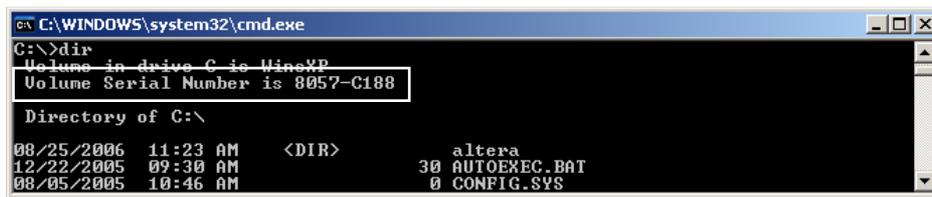


Figure 3-5 Volume Serial Number

### 3.3. How to change user's ID in user's logic

User can change user's ID in source code by using constant value. This constant value is 32-bit binary. Figure 3-6 shows user's ID in source code.

```

-- IP Lock core
Component TopIPLock is
Port (
  USERKEY      : in  std_logic_vector(31 downto 0);
  SCO          : in  std_logic;
  DCO          : inout std_logic;
  DDO          : inout std_logic;
  ENABLE       : out std_logic
);
End Component TopIPLock;

-- User's Logic
Component Counter32Bits Is
Port (
  SysClk      : in  std_logic;
  SysRstB     : in  std_logic;
  Enable      : in  std_logic;
  LED         : out std_logic_vector(3 downto 0)
);
End Component Counter32Bits;

----- Constant Declareation -----
-- User's Key
constant cUSERKEY      : std_logic_vector(31 downto 0) := x"00000000";

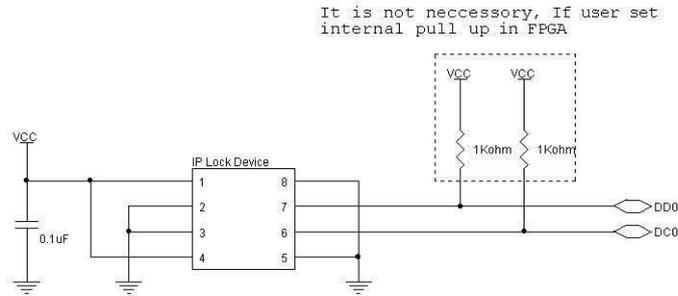
----- Signal Declareation -----
signal rEnable         : std_logic;

Begin
----- Component Mapping -----
    
```

Figure 3-6 User's ID in source code

#### 4. IP Lock Device

IP Lock device is device, which communicates with IP Lock core, for protect FPGA core. IP Lock device must connect to FPGA (IP Lock core) all time. Figure 4-1 shows recommend schematic of IP Lock device. Voltage I/O of FPGA that connects to IP Lock device should be connecting to +3.3 - +5 V.



Note : VCC support voltage 3.3 – 5 Volt

Figure 4-1 Schematic of IP Lock Device

For Xilinx FPGA, user can use internal pull up in FPGA by

- Setting in Design Object List. Create Area Constraints menu on ISE as show in Figure 4-2
- or
- Adding text in ucf file (pin assignment file) of user’s logic as shown in Figure 4-3.

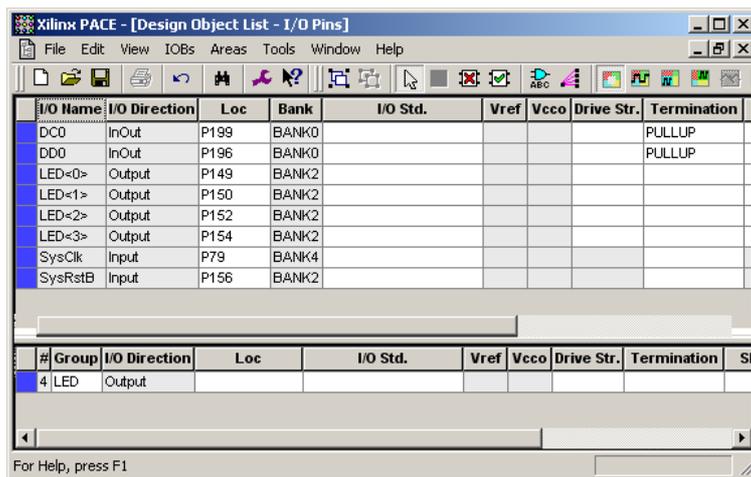


Figure 4-2 Setting internal pull up on ISE

```
NET "DD0" LOC = "P196" | PULLUP ;
NET "DC0" LOC = "P199" | PULLUP ;
```

Figure 4-3 Setting internal pull up on ucf file

For Altera FPGA, user can use internal pull up in FPGA by

- Setting in Assignment Editor on Quartus II as shown in Figure 4-4

or

- Adding text in qsf file (Quartus II Setting File) as shown in Figure 4-5

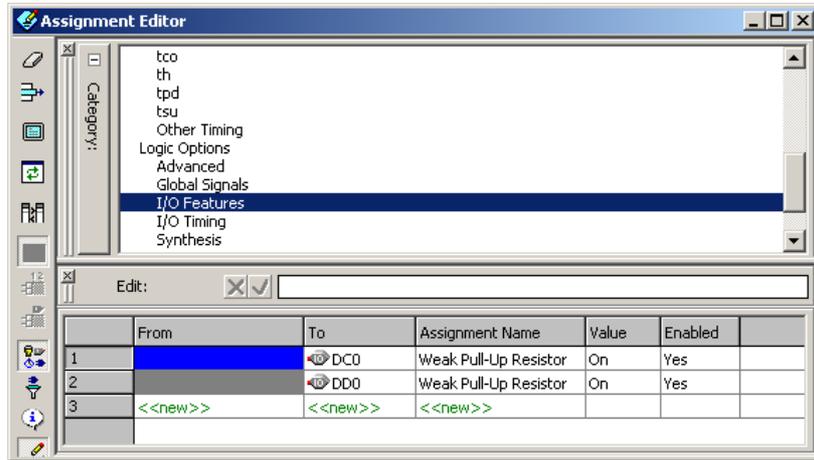
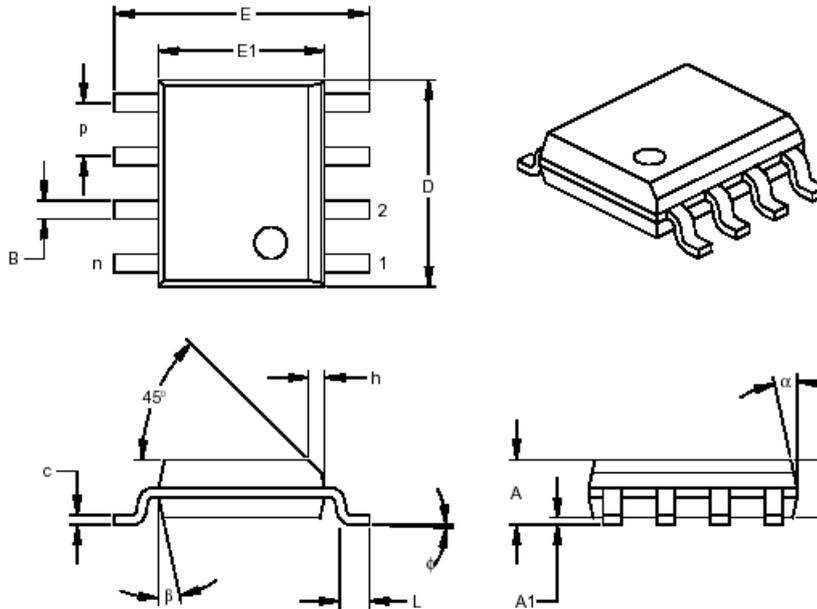


Figure 4-4 Setting internal pull up on Quartus II

```
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to DC0
```

```
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to DD0
```

Figure 4-5 Setting internal pull up on qsf file



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	P		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter  
§ Significant Characteristic

Figure 4-6 Package dimensions of IP Lock device

Figure 4-6 shows package dimensions of IP Lock device. Figure 4-7 shows footprint dimensions of IP Lock device. Figure 4-8 shows typical circuit of IP Lock device.

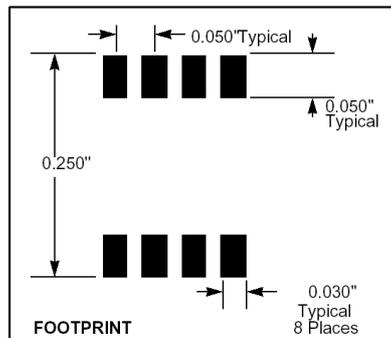


Figure 4-7 Footprint of IP Lock device (All dimensions in inch)

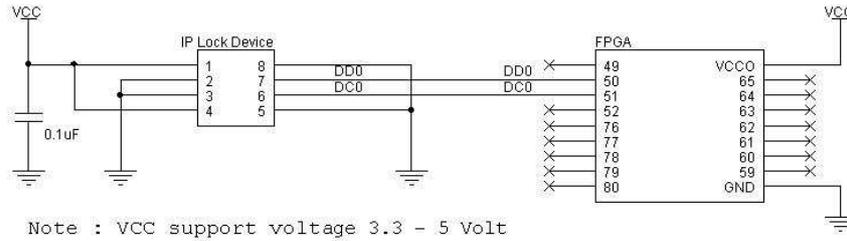


Figure 4-8 Typical circuit of IP Lock device

## 5. IP Lock Writer



Figure 5-1 IP Lock writer

IP Lock writer is shown in Figure 5-1. IP Lock writer use for write user's ID to IP Lock device via IP Lock software. IP Lock writer use USB bus power so it does not need external power to supply it. User can insert IP Lock device into socket on IP Lock writer for write user ID and pin1 of IP Lock device is as same as LED status position.

## 6. IP Lock Software

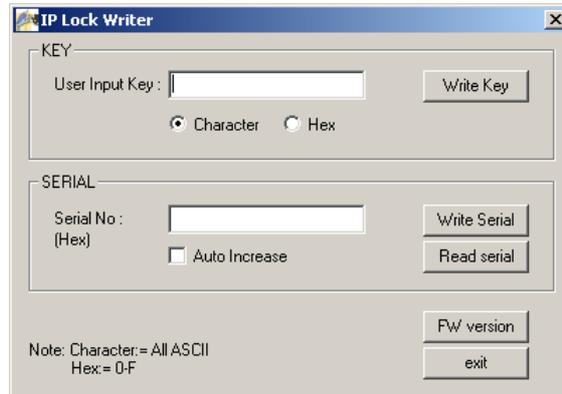


Figure 6-1 IP Lock Writer software

IP Lock writer software is software to access IP Lock writer. Users can use this software to write user's ID and serial number to IP Lock device.

IP Lock writer software has 2 main controls

1. ID: This main control use for write user's ID to IP Lock device. User can choice user's ID format, Character or HEX.
  - Character format: Software write user's ID to IP Lock device in HEX value using ASCII value of each character.
  - HEX format: software write user's ID to IP Lock device in HEX value.
2. Serial: This main control use for write serial number to IP Lock device. If user do not write serial number to IP Lock device. Default serial number value is "FFFFFFFFFFFFFFFF".
  - Auto Increase is increase serial number value by 1

FW version button show version of firmware on IP Lock writer.

Note:

- Default user's ID in IP Lock device is "00000000" until user writes new user's ID to IP lock device.
- User must write user's ID to IP Lock device at least one time before use it. Although user's ID, which is written to IP Lock device, is "00000000".

## 7. How to install device driver

Please follow these steps to install IP Lock device driver:

1. After plug in IP Lock writer to PC, “Found New Hardware Wizard” dialog (Figure 7-1) will be occurs. Select “Install from a list or specific location (Advanced)” and click “Next”.



Figure 7-1 “Found New Hardware Wizard” dialog

2. Select “Search for the best driver in these locations.” and browse to device driver location (Figure 7-2) then click next.

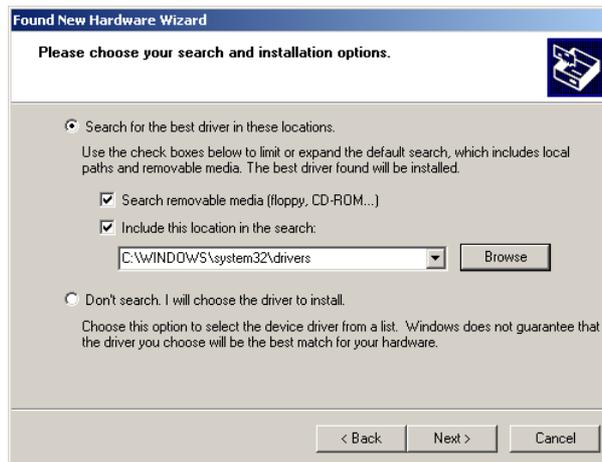


Figure 7-2 Select location of device driver

3. In warning dialog (Figure 7-3), click at “Continue Anyway”.



Figure 7-3 Warning dialog

4. In finish dialog (Figure 7-4), click "Finish" to complete install device driver process.



Figure 7-4 Finish dialog

## 8. Example VHDL design

The example source codes compose of Counter.vhd and Counter32bits.vhd. Counter.vhd is example code that shows how to connect between user's logic and Top IP Lock. Counter32Bits.vhd is example code that shows how to use ENABLE signal in user's logic. The block diagram of example VHDL design as shown in Figure 8-1

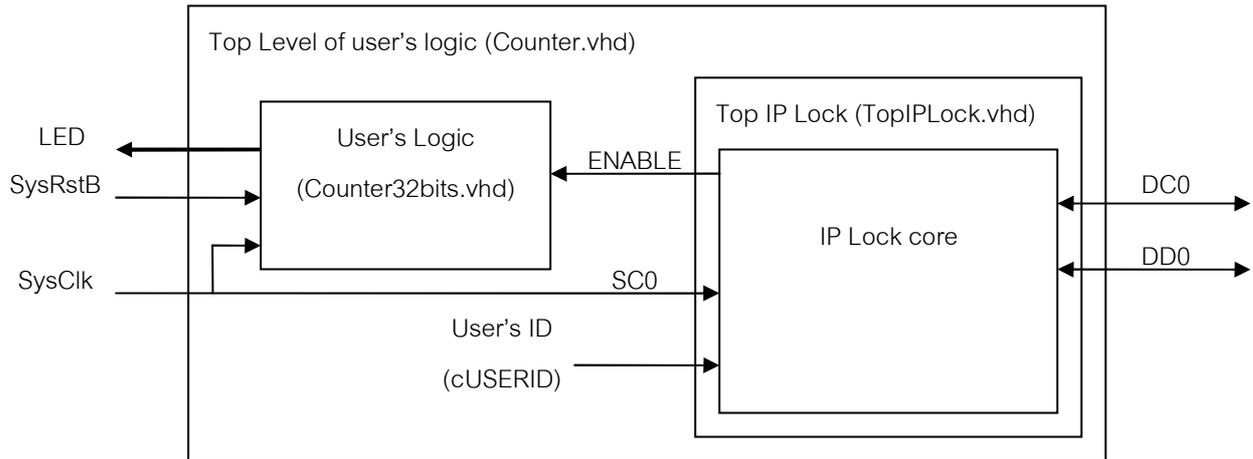


Figure 8-1 Example VHDL design block diagram

Using Xilinx, the structure of source file for implement example design as shown in Figure 8-2

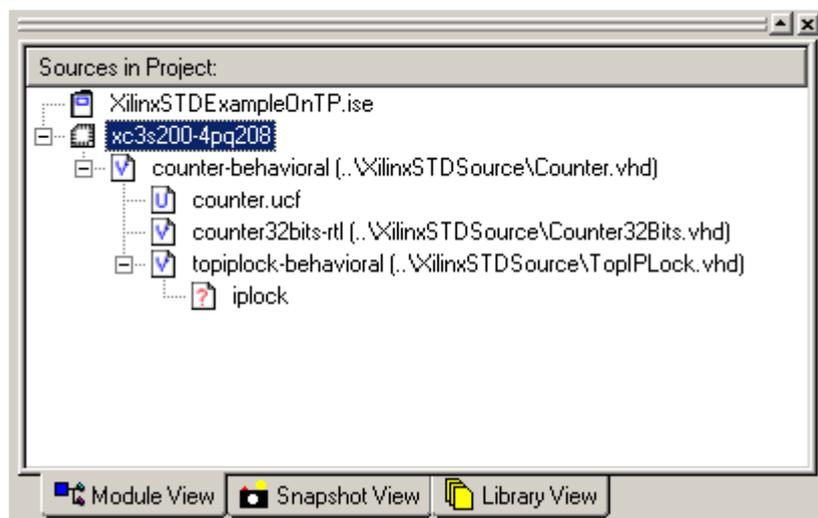


Figure 8-2 Structure of source file in example HDL design project for Xilinx ISE

Using Altera, the structure of source file for implement example design as shown in Figure 8-3

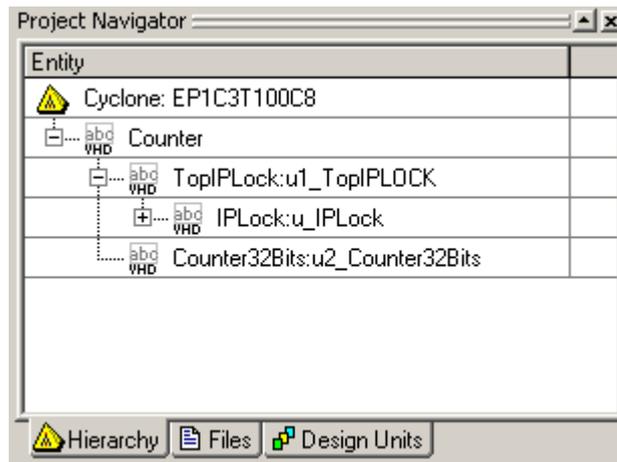


Figure 8-3 Structure of source file in example HDL design project for Quartus II

## 9. Troubleshooting

Following information may help user determine the problem and provides some plausible solution when IP Lock do not operated on user's board

Q: Enable signal from IP Lock is logic '0' (disable)?

A: Please check IP Lock device direction is mounted correctly or assign pin in FPGA correctly or set user's key in IP Lock device and IP Lock core correctly.

Q: Power supply voltage for IP Lock device is correct?

A: Please supply voltage as same as level with FPGA I/O pin

Q: DD0 and DC0 of IP Lock device pull up?

A: If they do not have external pull up, it can use internal pull up in FPGA

Q: Do you use IP Lock core same package with IP Lock writer?

A: Because IP Lock writer has unique writer's ID. So if user writes same user's ID from different IP Lock writer, ID on IP Lock device will mismatch from IP Lock core.

If user already check all item but IP Lock still do not work, Please contact us [iplock@design-gateway.com](mailto:iplock@design-gateway.com).

Note

Note





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