IP Lock (standard pack)

User's Manual

Design Gateway Co.,Ltd.

Rev 1.5

(PD0602-6-01-05E)

*** Please read this manual carefully before using IP Lock (standard pack)***

Revision History

Revision	Date	Detail of change
1.0	10 May 2006	Initial Release
1.1	18 July 2006	Adding IP lock core for Altera FPGA.
1.2	19 October 2006	Update detail of setting internal pull-up on ISE Update detail of SC0 signal
1.3	8 November 2007	Support Xilinx Virtex5 Adding Troubleshooting
1.4	6 August 2010	Update Figure 4-1 and 4-8
1.5	15 October 2010	Update Device support

Table of Contents

1. Introduction

Thank you very much for purchasing IP Lock. Please check that all the following items are in the box. If anything is missing or damaged, contact your distributor or Design Gateway Co.,Ltd.

1. IP Lock device 10 or 50 pcs.
2. User's manual
3. CD ROM contains :
   - IP Lock user's manual (IPL_UserManual1_1_E.pdf)
   - IP Lock core for Xilinx (TopIPLock.vhd, iplock.ngc and iplockex.ngo)
   - IP Lock core for Altera (TopIPLock.vhd, iplock.vhd)
   - Example VHDL design source codes (Counter.vhd, Counter32Bits.vhd)

1.1. Summary Feature

1. 128-bit AES encryption
2. IP Lock core and IP Lock device sent and receive data for checking every 200 msec
3. Xilinx FPGA support only Spartan2, Spartan2E, Spartan3, Spartan3E, Spartan6, Virtex, Virtex2, Virtex2Pro, Virtex4, Virtex5 and Virtex6
4. Altera FPGA support only Stratix, Stratix2, Stratix3, Stratix4, ArriaGX, Arria2GX, Cyclone Cyclone2 and Cyclone3

1.2. Minimum System Requirement

1. Pentium III or compatible processor
2. RAM 256 MB
3. Windows XP
4. Xilinx ISE 7.1 or over for Xilinx FPGA designer
5. Quartus II 4.1 or over for Altera FPGA designer

1.3. Warranty Policy

1. Product warranty is valid for 1 year from purchasing date.
2. Warranty is void if any modification has been made to this product and any incorrect operation from this manual or warranty sticker is torn or damaged.
3. In order to claim for product exchange or technical support within warranty period, official receipt is required for unregistered customer as an evidence of purchasing whereas official receipt is unnecessary for registered customer (please fill up registration card attached herewith the product and send back to Design Gateway Co.,Ltd).

1.4. Customer Support

Customer can contact to support@design-gateway.com for support of any problem about IP Lock or visit our website at www.design-gateway.com.

Your Personal information will be restricted with high confidentiality.

2. IP Lock System

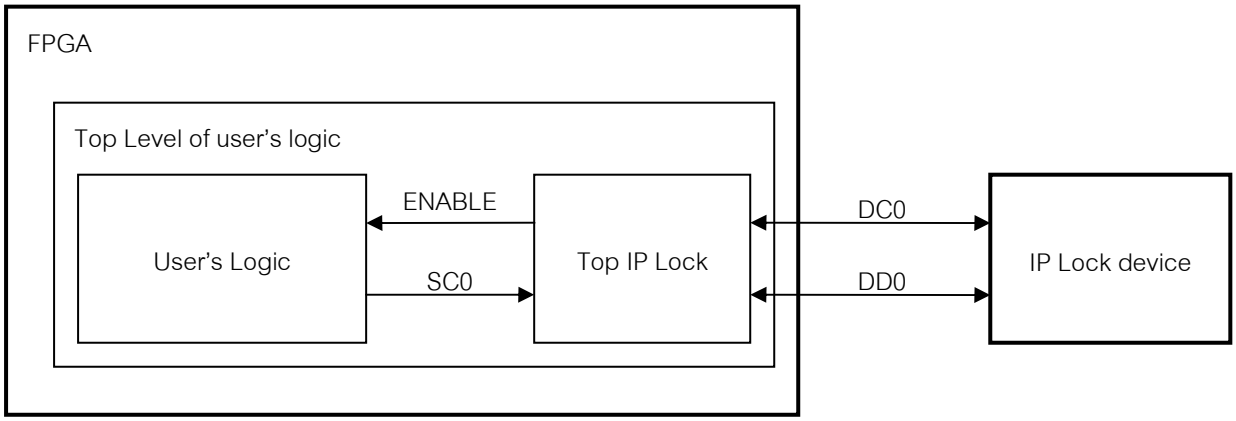


Figure 2-1 IP Lock System

From above block diagram, it is shown IP Lock system. IP Lock core communicate with IP Lock device for check user's key. If user's key is correct, ENABLE signal is logic '1' (enable). On the other hand, if user's key is not correct, ENABLE signal is logic '0' (disable). User can use ENABLE signal from IP Lock core to enable user's logic. For IP Lock (standard pack) *Design Gateway Co.,Ltd fix user's key in IP Lock core and IP Lock device so user can not change user's key value*. And each IP Lock (standard pack) user's key value is not same value so user can not use IP Lock core and IP Lock device from different standard pack.

IP Lock core use 3 signals for active. That is SC0, DC0 and DD0. SC0 signal is system clock for IP Lock core. It use internal clock from user's logic but *SC0 must have frequency range between 1-25 MHz*. DC0 and DD0 signal is data signal. It use for communicate between IP Lock core and IP Lock device.

Because ENABLE signal from Top IP Lock does not synchronous with user's clock so user should be add a D Flip-Flop in user's logic as show in Figure 2-2. ENABLE signal that out from D Flip-Flop is synchronous with user's clock in user's logic.

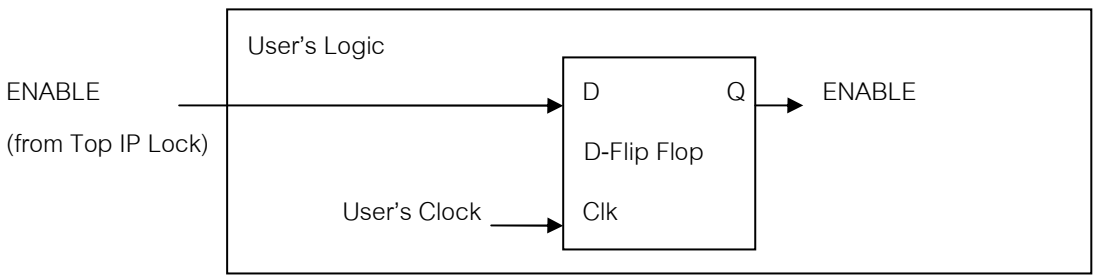


Figure 2-2 Recommend logic on ENABLE signal

3. IP Lock core

3.1. IP Lock core for Xilinx FPGA

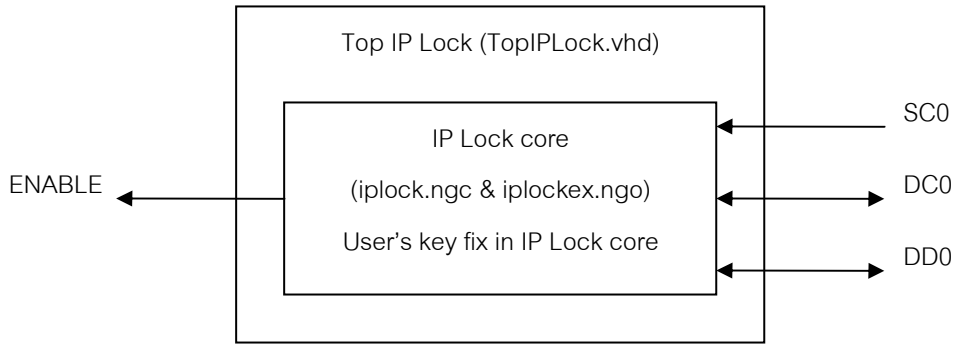


Figure 3-1 Top level of IP Lock for Xilinx FPGA

Figure 3-1 shows block diagram of top level IP Lock for Xilinx FPGA.

- Xilinx IP Lock core (iplock.ngc and iplockex.ngo): IP Lock core communicate with IP Lock device for check user's key before enable ENABLE signal. If communication between IP Lock core and IP Lock device failed or user's key is not same value, IP Lock will disable ENABLE signal.
- User must copy iplock.ngc and iplockex.ngo to Xilinx project folder before start synthesis and implement HDL code.
- User's key value already fix in IP Lock core.

3.2. IP Lock core for Altera FPGA

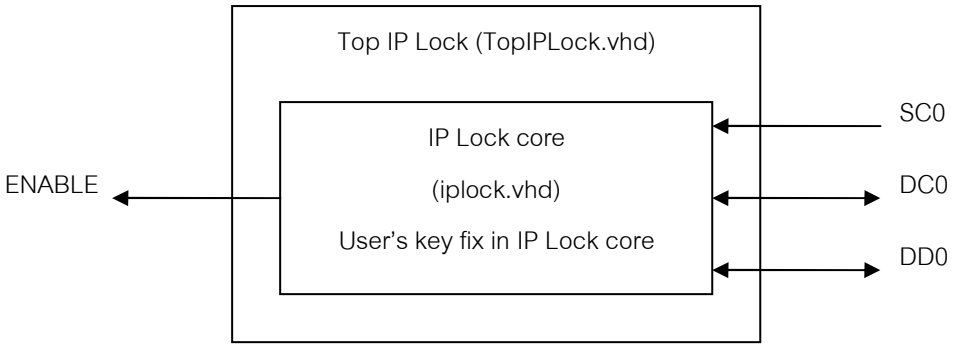


Figure 3-2 Top level of IP Lock for Altera FPGA

Figure 3-2 shows block diagram of top level IP Lock for Altera FPGA.

- Altera IP Lock core (iplock.vhd): IP Lock core communicate with IP Lock device for check user's key before enable ENABLE signal. If communication between IP Lock core and IP Lock device failed or user's key is not same value, IP Lock will disable ENABLE signal.
- User's key value already fix in IP Lock core.
- User must add IP Lock license into Quartus II license as shown in Figure 3-3 before start synthesis and implement HDL code. If user does not have IP Lock license, User can not synthesis and implement IP Lock core.
- IP Lock license file: User must send email to iplock@design-gateway.com for request IP Lock license and Design Gateway Co.,Ltd require some information for register as shown in Figure 3-4. Please fill this information in email.
- User can check Volume Serial Number by run DOS prompt and use command "dir" on window drive as shown in Figure 3-5 .

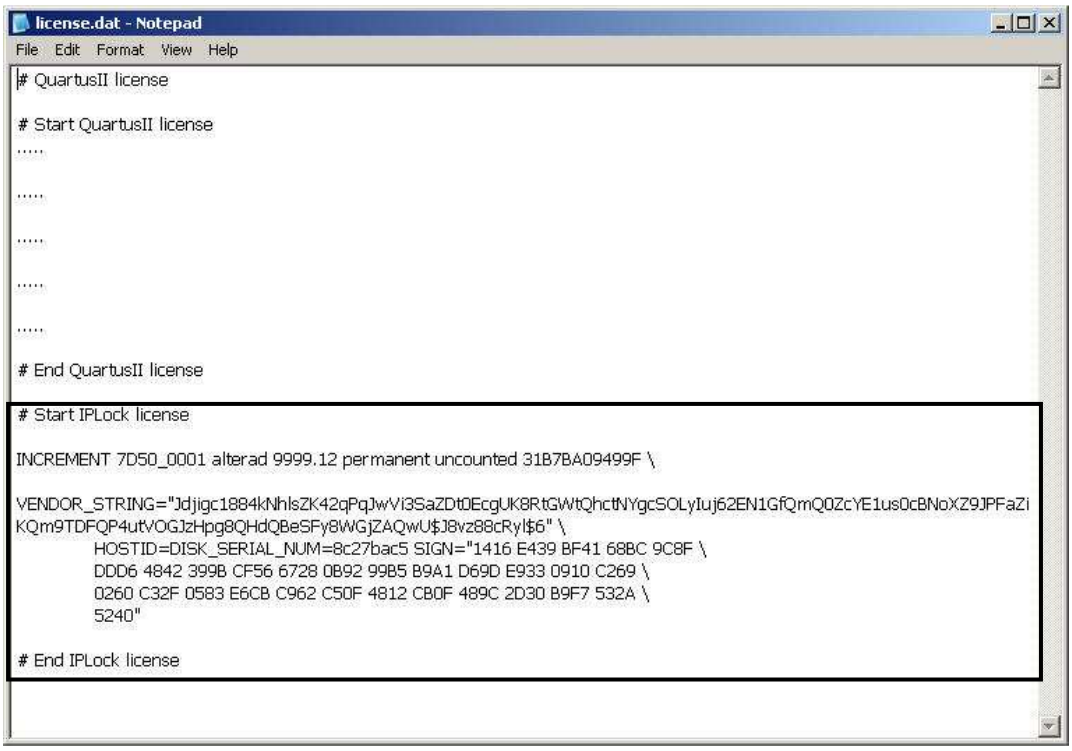


Figure 3-3 IP Lock license in Quartus II license

Name / Company: ……..

IP Lock Serial Number: ……

Volume Serial Number: ……

Address: ……

Tel: ……

Fax: ……

Figure 3-4 Information for register

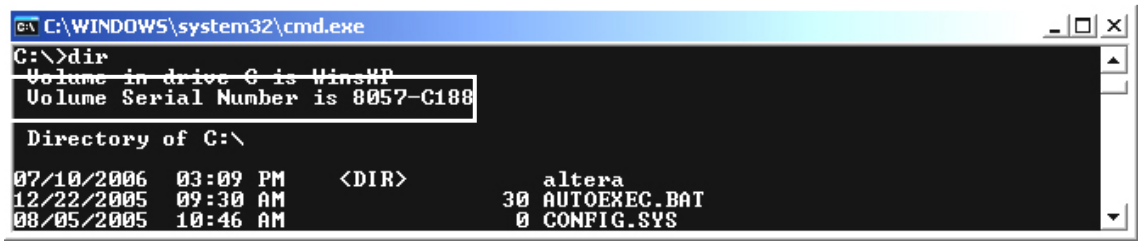


Figure 3-5 Volume Serial Number

4. IP Lock Device

IP Lock device is device, which communicates with IP Lock core, for protect FPGA core. IP Lock device must connect to FPGA (IP Lock core) all time. Figure 4-1 shows recommend schematic of IP Lock device. Voltage I/O of FPGA that connects to IP Lock device should be connecting to +3.3 - +5 V.

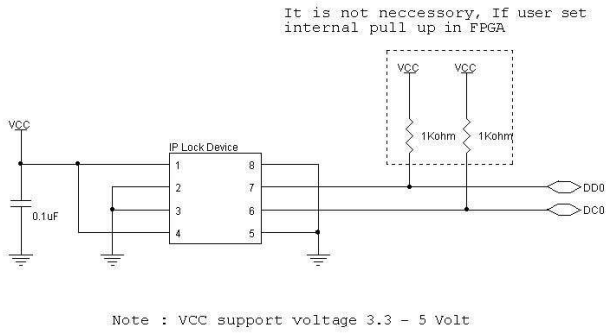


Figure 4-1 Schematic of IP Lock Device

For Xilinx FPGA, user can use internal pull up in FPGA by

- setting in Design Object List –I/O Pins on ISE as shown in Figure 4-2

or

- edit ucf file (User Constraint File) of user's logic as shown in Figure 4-3.

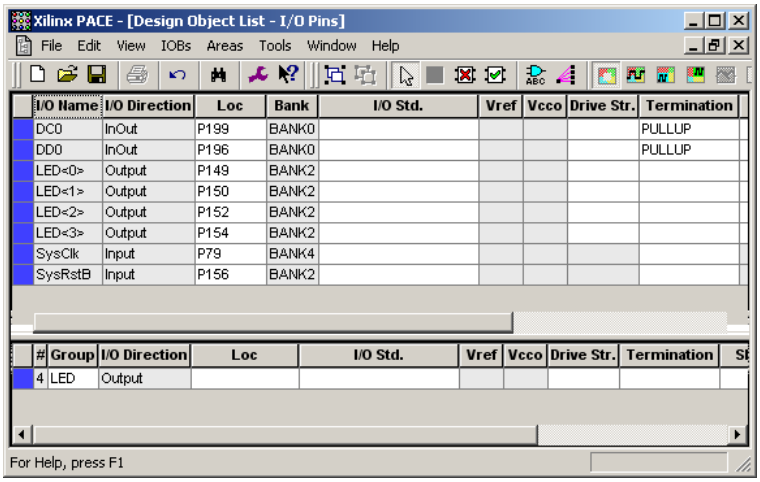


Figure 4-2 Setting internal pull up on ISE file

```
NET "DD0"  LOC = "P196" | PULLUP ;
NET "DC0"  LOC = "P199" | PULLUP ;
```

Figure 4-3 Setting internal pull up on ucf file

For Altera FPGA, user can use internal pull up in FPGA by

- setting in Assignment Editor on Quartus II as shown in Figure 4-4

or

- adding in qsf file (Quartus II Setting File) as shown in Figure 4-5

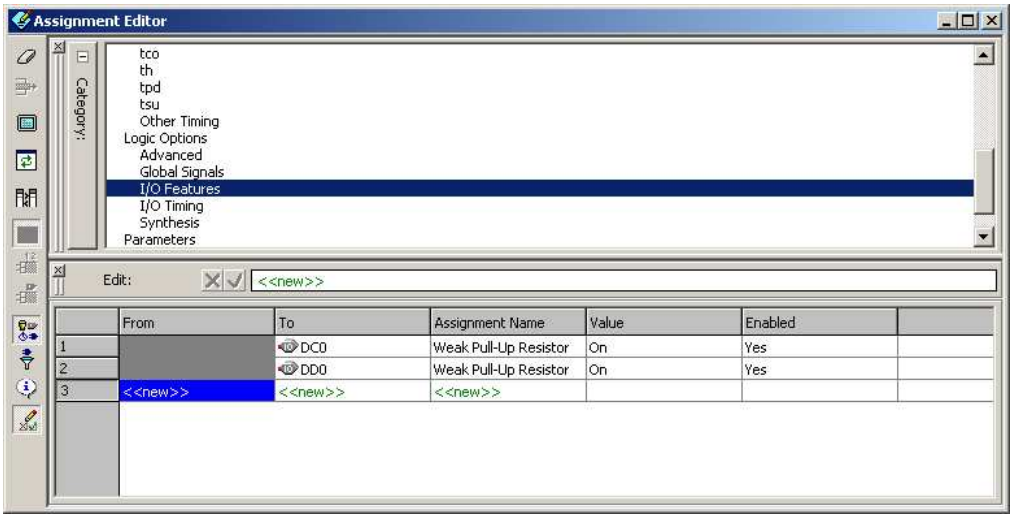
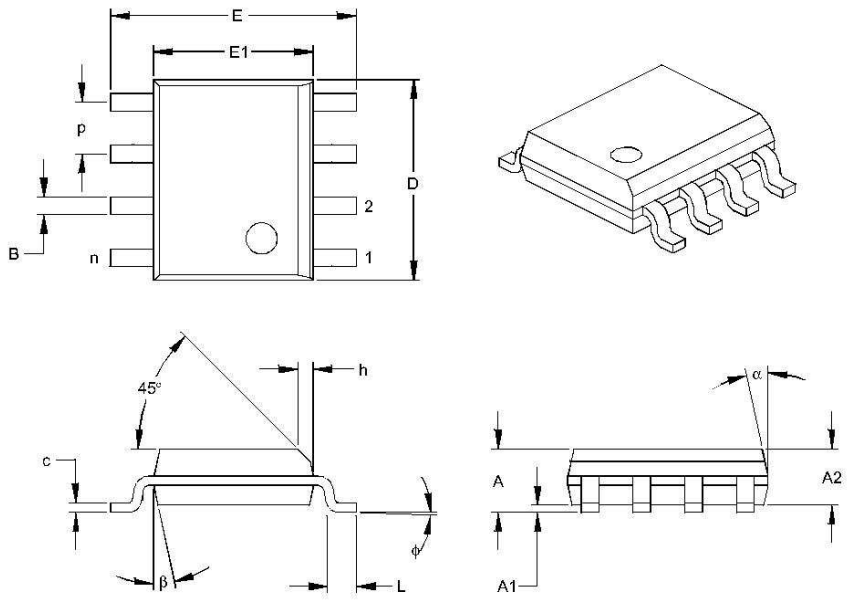


Figure 4-4 Setting internal pull up on Quartus II

```
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to DC0
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to DD0
```

Figure 4-5 Setting internal pull up on qsf file



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Figure 4-6 Package dimensions of IP Lock device

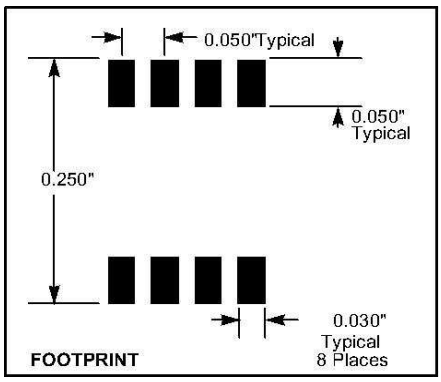


Figure 4-7 Footprint of IP Lock device (All dimensions in inch)

Figure 4-6 shows package dimensions of IP Lock device. Figure 4-7 shows footprint dimensions of IP Lock device. Figure 4-8 shows typical circuit of IP Lock device.

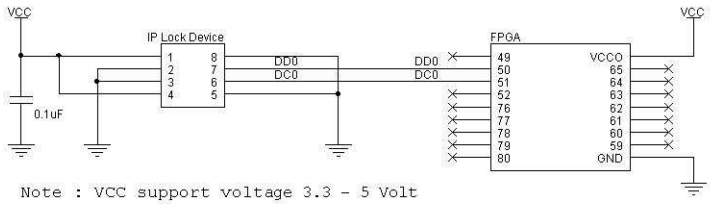


Figure 4-8 Typical circuit of IP Lock device

5. Example VHDL design

The example source codes compose of Counter.vhd and Counter32bits.vhd. Counter.vhd is example code that shows how to connect between user's logic and Top IP Lock. Counter32Bits.vhd is example code that shows how to use ENABLE signal in user's logic. The block diagram of example VHDL design as shown in Figure 5-1

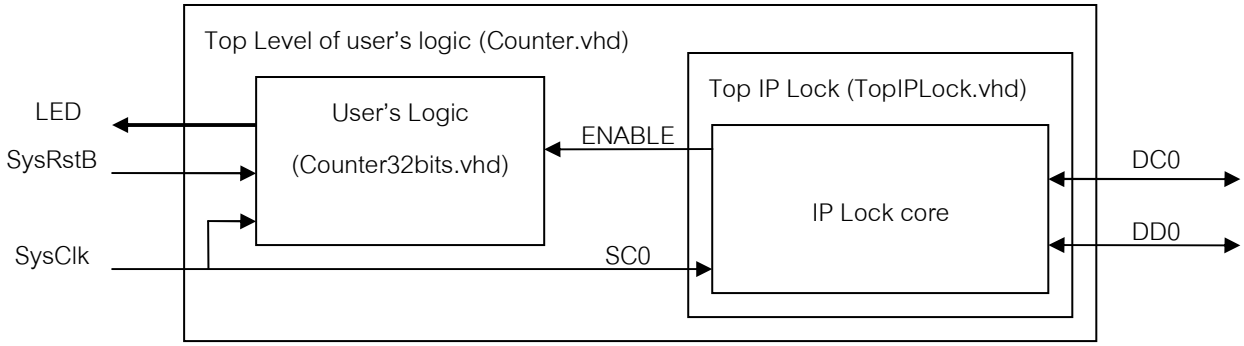


Figure 5-1 Example VHDL design block diagram

Using Xilinx, the structure of source file for implement example design as shown in Figure 5-2

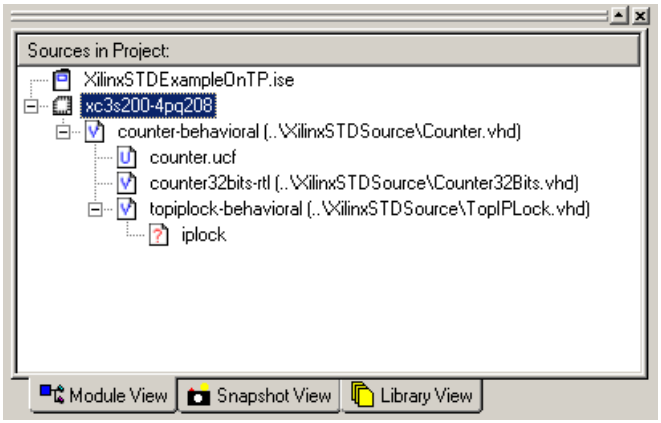


Figure 5-2 Structure of source file in example HDL design project for Xilinx ISE

Using Altera, the structure of source file for implement example design as shown in Figure 5-3

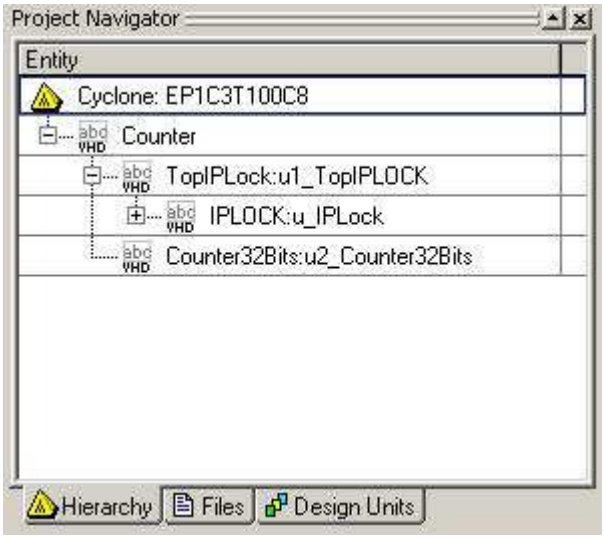


Figure 5-3 Structure of source file in example HDL design project for Quartus II

6. Troubleshooting

Following information may help user determine the problem and provides some plausible solution when IP Lock do not operated on user's board

Q: Enable signal from IP Lock is logic '0' (disable)?

A: Please check IP Lock device direction is mounted correctly or assign pin in FPGA correctly.

Q: Power supply voltage for IP Lock device is correct?

A: Please supply voltage as same as level with FPGA I/O pin.

Q: DD0 and DC0 of IP Lock device pull up?

A: If they do not have external pull up, it can use internal pull up in FPGA.

Q: Do you use IP Lock core and IP Lock device from same package?

A: Because user's ID in IP Lock core and user's ID IP Lock device are same and fix, so if user use IP Lock core and IP Lock device from different package, IP Lock does not enable (disable).

If user already check all item but IP Lock still do not work, Please contact us iplock@design-gateway.com

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