VC-AN01E

Guideline for clock implementation

Ver1.0

This application note explains guidelines for clock implementation on the user's board with using "VariClock".

[Contents]

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1: VariClock output specification

VariClock generates clock output by LVTTL-level. Table1 shows general output specification.

Item	Specification	Remark
Output level	High level over2.4V Low level below 0.4V	LVTTL level
Output current	+24mA / -24mA	
Guaranteed frequency	25MHz - 250MHz	Output load 20pF

[Table 1] VariClock general output specification

Though the guaranteed maximum frequency of VariClock is 250MHz, actual upper limit of clock frequency in the user board coupled with VariClock depends on the clock line implementation on the board. The potential of VariClock can be fully extracted when enough consideration for clock line implementation is done to the user board. On the other hand, VariClock cannot play its high capability if the clock line of user board is not implemented adequately.

To bring out the maximum performance of VariClock, please consider the following point.

[1] Clock Line has proper termination

[2] Board pattern of clock line is optimized

[3] Load of clock line is kept in proper range

The following pages explain guidelines of each topic. This application note premises that VariClock is used for clock source, however, it can be applied not only VariClock but also all clock system.

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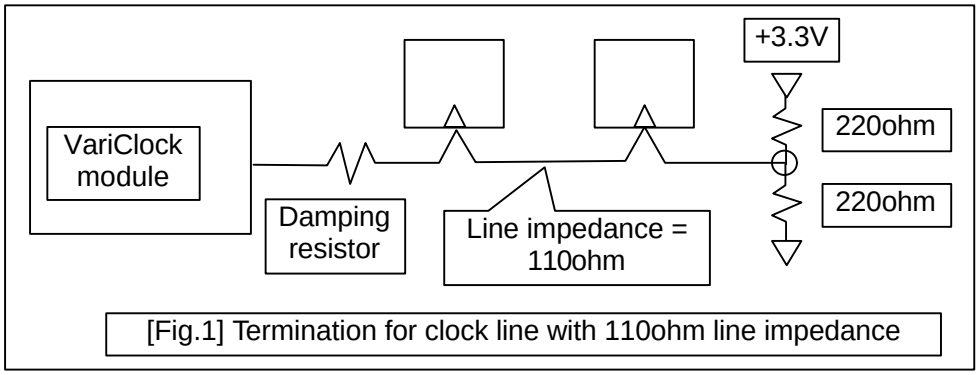
2: Termination of clock line

High-speed user board requires an optimized termination that matches with line independence of clock line. For example, Thevenin termination with 110ohm of synthesized resistor value is effective on the clock line with 110ohm line impedance. In this case, please implement the board circuit as figure1 shown below.



[Fig.1] Termination for clock line with 110ohm line impedance

Value of the termination resistor should be determined so that output current value of VariClock will not exceed the maximum output current of +24mA/-24mA. Each of 220ohm pull-up and pull-down Thevenin resistors is implemented in the figure1 for clock line with 110ohm line impedance. In this case, even the damping resistor value is 0ohm, VariClock can drive the clock signal to High or Low level because its drive current is 3.3[V] / 220[ohm] = 15mA as allowable range as below 24mA.

Generally, line impedance of clock line is required to keep low value by wide board pattern. This is because clock line must have enough tolerance against the external noise and must keep minimum of amplitude reduction by minimizing series resistor value of the line.

But simultaneously, line impedance is required not to exceed the maximum drive current of VariClock. For example, if the line impedance is 50ohm, Thevenin resistor value must be 100ohm so that 33mA drive current is required, but this current value exceeds maximum output current specification of VariClock.

With the consideration of VariClock current drive capability, it is one of the best implementation that clock line impedance is adjusted to 75ohm and set the Thevenin termination resistor value to 150ohm. In this case, drive current would be 22mA as allowable range of VariClock specification.

On the other hand, recommendable damping register value is between 22 - 39ohm in general. When the value of damping resistor is increased, overshoot of signal wave will decrease but rising and falling time of clock line will be slower and clock signal amplitude will decrease, and vice versa. Because of this trade-off relationship, damping resistor value must be optimized so that the clock waveform will be the best one.

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3: Board pattern of clock line

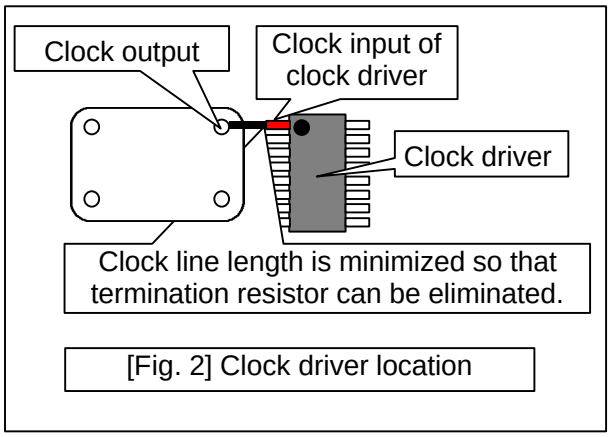
The consideration below must be taken to build the best clock line implementation.

- Keep the clock pattern length as short as possible.
- Build the clock pattern as a simple stroke line, and do never build stab on the pattern.
- Keep minimum number of Via on the pattern.
- Build the GND guard pattern of low impedance around the clock line.
- Build the board so that adjacent layer of clock line layer should be GND or VCC layer of low impedance.
- Another signal pattern should not be set parallel with clock line for protection from cross talk noise.

Moreover, user should consider following point when multiple clock channel of identical clock source exists on the user board. In this case user must prepare some clock driver because clock output of VariClock is single channel.

- Both the line impedance value and termination resistor value must be the same among all clock channels.
- Board pattern trace length must be the same among all clock channels.
- Equalize device count on each pattern so that line load value must be the same among all clock channels.
- Keep the same Via count of each pattern among all clock channels.

When the clock driver is used on user board, locate the clock driver close to the VariClock so that the clock input pin of clock driver could be as close as the clock output pin (pin#8) of VariClock. With this consideration, termination resistor of this clock line can be eliminated because this signal pattern length is minimized.



[Fig. 2] Clock driver location

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4: Load of clock line

The guaranteed maximum frequency of VariClock is 250MHz on condition that output load is 20pF. The actual frequency will decrease according to the load connected to the clock line. Therefore, clock driver is required to reduce load of each clock channel in case many clock supply devices might exist on the user board.

In the general printed board, the approximate load can be calculated as below.

[1] Board pattern 1cm = 1pF

[2] Board Via 1 point = 1pF(*)

(*) Keep effort for board design so that no Via could exist on the clock line. When the Via exists on the clock line, the signal reflection will occur because line impedance will change at Via point, thus signal quality will decrease.

So the load explained above will be added beside the total load by clock input pin of connected device. Maximum acceptable load will depend on the clock frequency. For example, when the 250MHz frequency clock is required by VariClock, total load should not exceed 20pF. Assume that the load of device clock input pin is 15pF, only one device can be connected to the clock line. And VariClock output pin (pin#8) itself is through-hole, so if its load is assumed to be 1pF, clock line length should be less than 4cm. Needless to say, the clock line length should be as short as possible.

5: Conclusion

Optimized design for clock line on user board can extract the maximum capability of VariClock.

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