VariClock low voltage support

Ver1.0

This application note describes how to apply VariClock to low voltage signal clock such as 2.5V-LVTTL or LVDS.

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1: Output level of VariClock

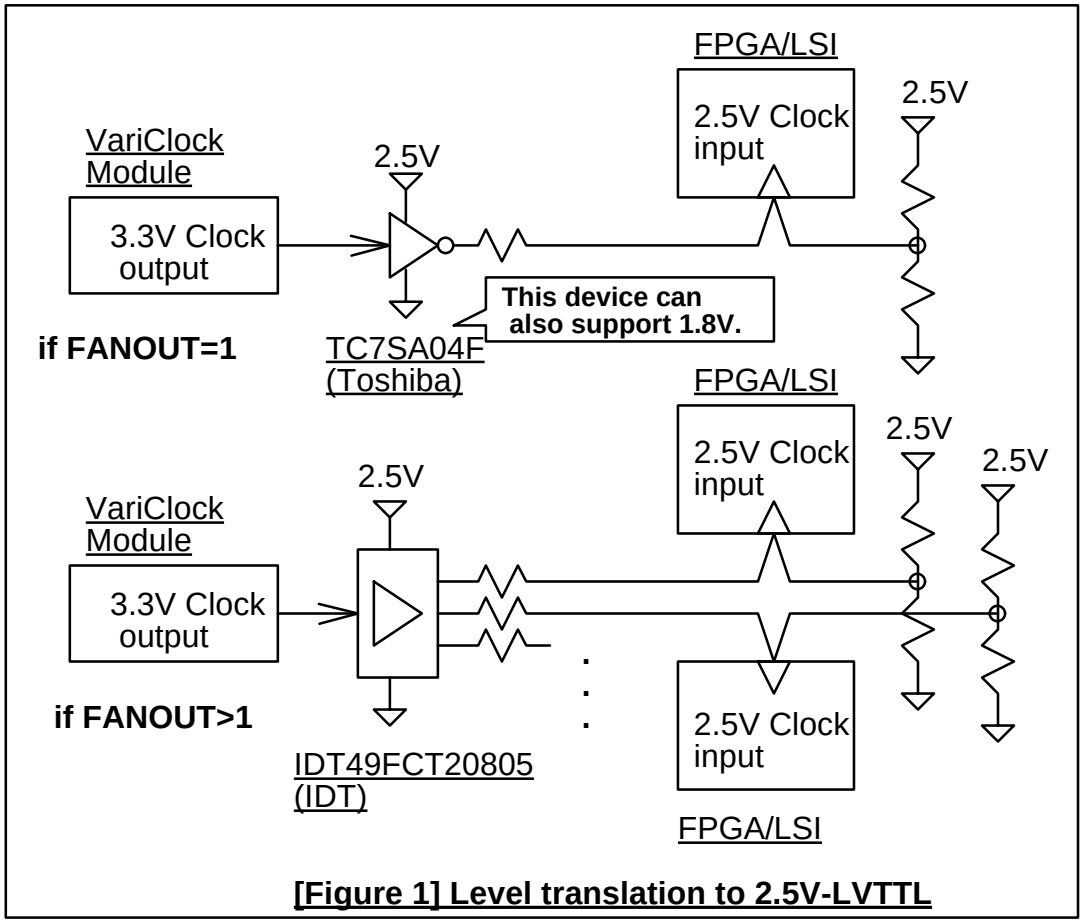
Some latest LSI or FPGA with very low voltage power supply cannot accept 3.3V-LVTTL level clock input. Unfortunately, because clock output signal from VariClock is 3.3V-LVTTL level, it is possible that the high level of output clock from VariClock may reach to 3.3V at maximum. Thus direct connection between VariClock and LSI/FPGA without 3.3V-tolerant is inhibited. Moreover, clock signal should be translated into differential signal when clock input must be LVDS standard.

Also, when clock must be supplied to multiple devices, not only level conversion but also clock driver insertion for increased fan-out is required. In this case, it is recommendable to use such clock driver that can accept 3.3V-LVTTL input and can support multiple clock output of required signal standard.

A single clock driver of both level conversion and fan-out support will minimize jitter increase by the additional device insertion.

2: 2.5V-LVTTL Support

To support LSI/FPGA that requires 2.5V-LVTTL level clock input, level translation device from 3.3V-LVTTL to 2.5V-LVTTL must be inserted as following figure 1.



[Figure 1] Level translation to 2.5V-LVTTL

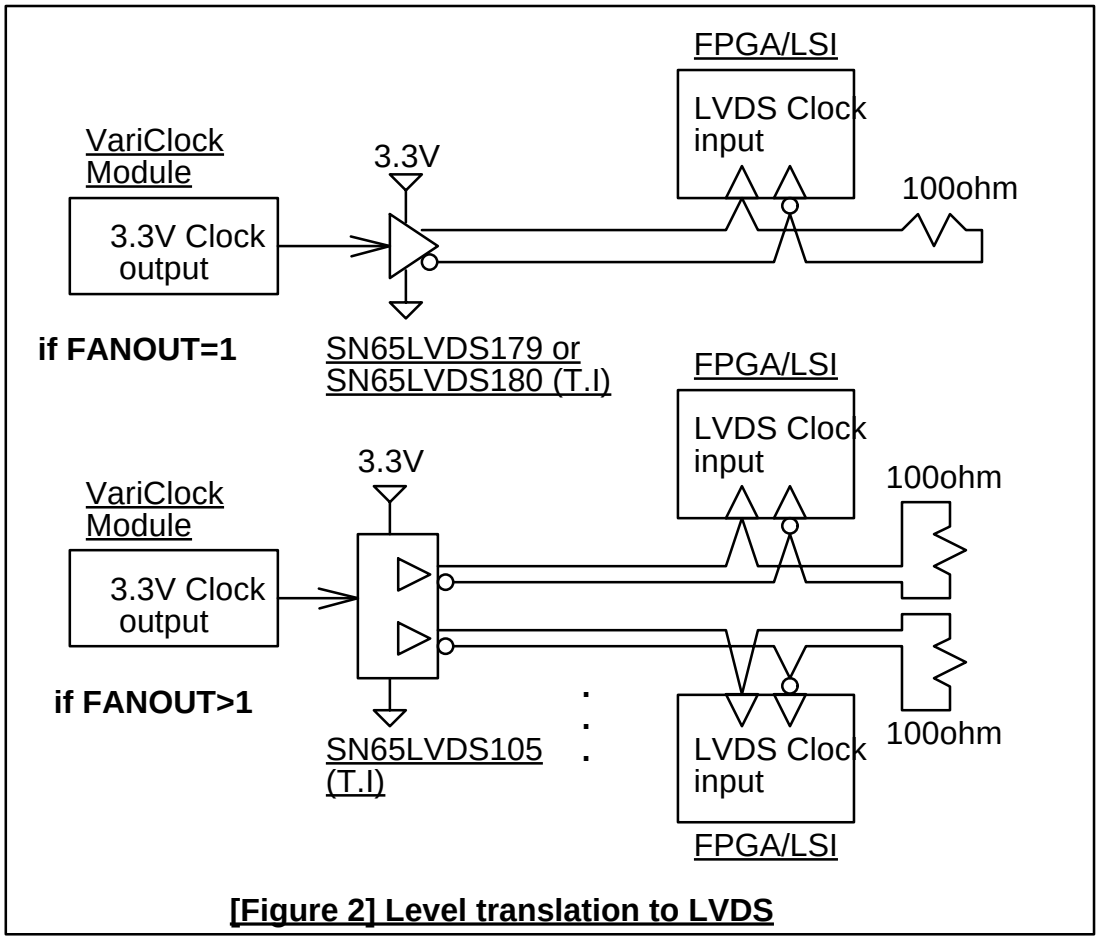
When clock should be supplied to only one device (FANOUT=1), single level translation of one-input to one-output is enough. In this case high-speed one-gate logic such as TC7SA04F from Toshiba is suitable because of the board area. Though the output clock phase shifts 180 degree from input clock because of the inverter buffer, it is not the problem unless direct clock output from VariClock is supplied to another part of the circuit. This TC7SA04F also supports 1.8V power supply voltage.

When clock must be distributed to multiple devices (FANOUT>1), it is effective to use clock driver (with minimum channel skew) that also can translate signal level. IDT49F20805 from IDT, that can accept 3.3V level input and can supply 2.5V level output, is recommendable in this case.

Clock driver device with PLL application such as ZeroDelay buffer is not recommended because PLL will degrade jitter characteristics. Always use pure fan-out type buffer that does not adjust clock phase by internal PLL.

3: LVDS Support

To support LSI/FPGA that requires LVDS differential clock input, signal translation device from 3.3V-LVTTL to LVDS must be inserted as following figure 2.



[Figure 2] Level translation to LVDS

When clock should be supplied to only one device (FANOUT=1), user can use single channel translator such as SN65LVDS179 or SN65LVDS180 from Texas-Instruments. If more than two devices require LVDS clock input (FANOUT>1), it is recommendable to use clock driver that can translate 3.3V-LVTTL to LVDS and also can increase clock channel such as SN65LVDS105 from Texas-Instruments

It is also recommendable for LVDS not to use clock driver with internal PLL because of the jitter characteristic.

4: Conclusion

VariClock can be applied as a clock source that is not the 3.3V-LVTTL level by adequate signal translator or clock driver insertion.