# NVMe PCIe Gen3 Host Controller Core: Breaking the barrier of limited number of PCIe Harden IP on Intel® FPGA Arria® 10 / Stratix® 10 device.

By Design Gateway Co., Ltd.

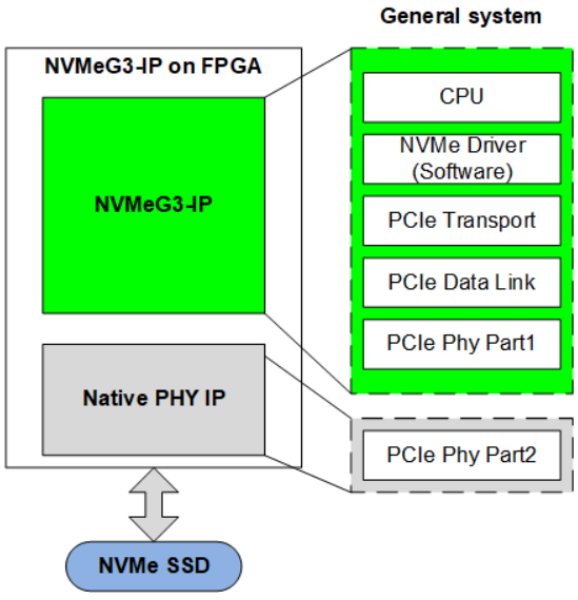
The Intel® FPGA Arria® 10 and Stratix® 10 family has limited number of PCIe Harden IP Block but features rich with Transceiver which has the capability of supporting a PCI Express® Gen3 interface.

**Example number of PCIe Harden IP block & Transceivers on Arria® 10 & Stratix® 10**

| | **Arria® 10 GX/SX** 270/320/480/570/660 | **Stratix® 10 GX/SX** 400/650/850/1100 |
|---|---|---|
| PCIe Hardened IP blocks | 2(PCIe Gen3x8) | 1/1/2/2(PCIe Gen3x16) |
| Total Transceiver count | 24/24/36/48/48 | 24/24/48/48 |

Design Gateway's NVMe PCIe Gen3 Host Controller IP core (NVMeG3-IP) is designed to leverage Intel® FPGA's Transceivers to support the NVMe SSD drive PCIe Gen3 technology. The IP core has been proven on Intel® Arria® 10 GX Development Kit and able to achieve incredibly fast performance: >2GB/s write speed and >3GB/s read speed.

## Implementation of NVMe Host Controller on Intel® FPGA's transceiver




*NVMe Implementation. (Image source: Design Gateway)*

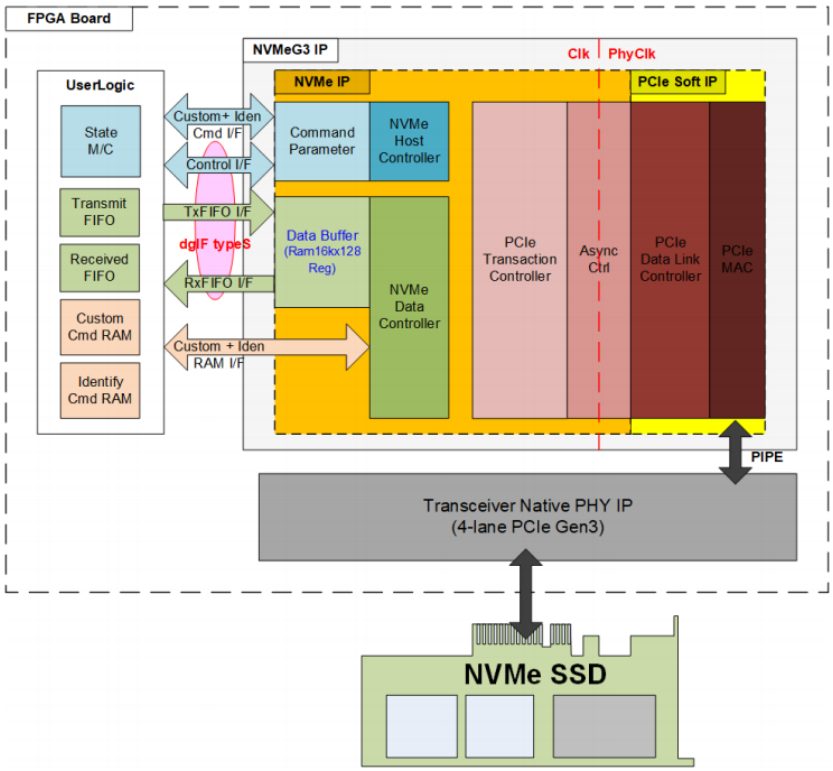
Conventionally, the NVMe host is implemented by using a Host Processor operating with a PCIe Controller for transferring data to and from the NVMe SSD. NVMe protocol is implemented for device

driver communications with the PCIe controller hardware CPU peripheral connected through a very high-speed bus. External DDR memory is required for data buffering and command queue to transfer the data between the PCIe controller and SSD.

Since Intel® Arria® 10 / Stratix® 10 FPGA features with 17.4Gbps ~ 28.3Gbps transceiver which capable of PCIe Gen3 interface support but has limited number of PCIe Gen3 Harden IP on some device.

Design Gateway solved this problem by developing the NVMeG3-IP core that able to run as a standalone NVMe host controller with bult-in PCIe soft IP and PCIe bridge logic in single core. Enabling NVMe PCIe Gen3 SSD access with simplify user interface and standard features are designed for ease of usage without needing knowledge of the NVMe protocol.

## Overview of NVMeG3-IP




*NVMeG3-IP block diagram. (Image source: Design Gateway)*

## Key features

- Implement application layer, transaction layer, data link layer, and some parts of the physical layer to access the NVMe SSD without CPU and external DDR memory required
- Operate with Intel® PCIe PHY IP (PIPE) configured as a 4-lane PCIe Gen3 (128-bit bus interface)
- Includes 256 Kbyte RAM data buffer
- Supports six commands, i.e. Identify, Shutdown, Write, Read, SMART, and Flush (support additional command as optional)

- User clock frequency must be more than or equal to PCIe clock (250MHz for Gen3)
- Available reference design:
  - Intel® Arria® 10 GX Development Kit with AB18-PCIeX16/AB16-PCIeXOVR adapter board.
  - Intel® Stratix® 10 GX Development Kit with AB18-PCIeX16/AB16-PCIeXOVR adapter board.

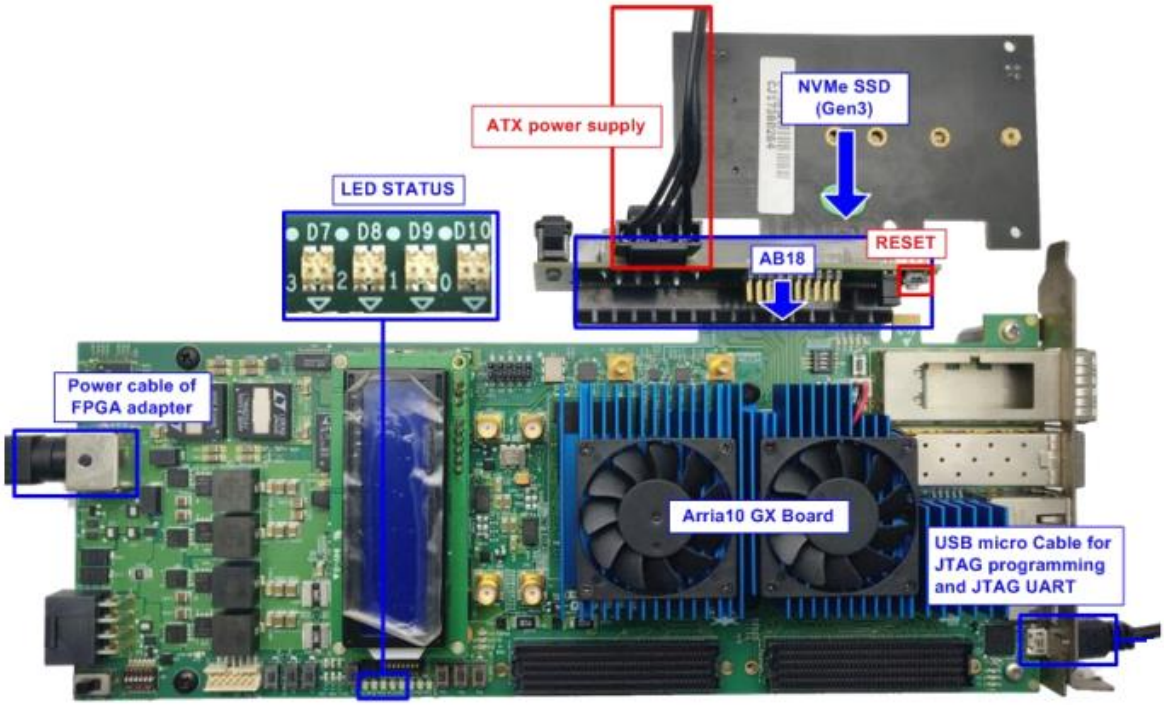
Example Implementation Statistics for Intel® Arria 10 GX device

| Family | Example Device | Fmax (MHz) | Logic utilization (ALMs) | Registers | Pin | Block Memory | Design Tools |
|---|---|---|---|---|---|---|---|
| Arria10 GX | 10AX115S2F45I1SG | 300 | 8560 | 10984 | - | 140 M20Ks | QuartusII 18.0 |

FPGA resource usages on the Arria® 10 GX : 10AX115S2F45I1SG FPGA device are shown in Table

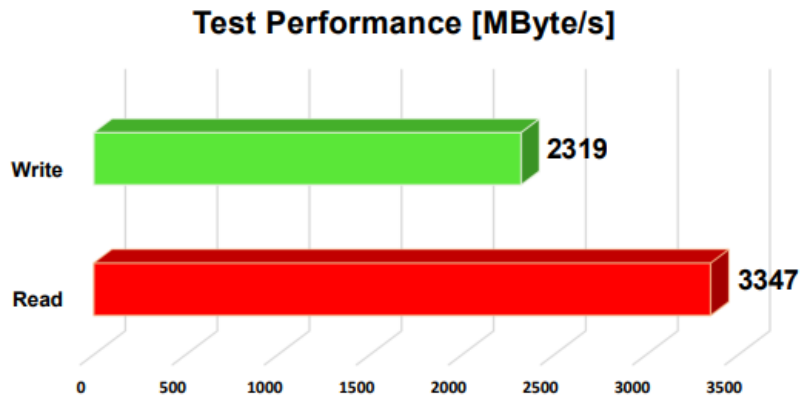
Because of very low FPGA resource usages, NVMeG3-IP core is also suitable for building of a multi-channel RAID system with very high performance and the lowest possible FPGA resource consumption.

## Implementation and performance result on Intel® Arria® 10 GX Development Kit




*NVMeG3-IP demo environment set up on Arria® 10 GX Dev. Kit. (Image source: Design Gateway)*

The example test result when running the demo system on the Arria® 10 GX Dev. Kit while using the Samsung 970 PRO NVMe PCIe Gen3 SSD is shown in figure below.




*NVMe SSD read/write performance on Intel® Arria® 10 GX by using* Samsung 970 PRO NVMe PCIe Gen3 SSD *SSD. (Image source: Design Gateway)*

## Conclusion

NVMeG3-IP Core provides a solution to enable NVMe PCIe Gen3 SSD interface on the Arria® 10 GX Development kit and also the solution for Intel® FPGA device family features with 17.4Gbps ~ 28.3Gbps transceiver but a PCIe Gen3 Harden IP doesn't available or has limited number. NVMeG3-IP is designed with the goal of achieving the highest possible performance with the lowest possible FPGA resource usage for NVMe SSD access without requiring a CPU. It's very suitable for high performance NVMe storage without CPU invention and able to implement multiple NVMe SSD interfaces by utilizing Intel® FPGA's transceivers with no limitations from the number of available PCIe integrated blocks on the FPGA device.

For more detail of NVMeG3-IP and available reference design, please visit Design Gateway's website at https://dgway.com/NVMeG3-IP_A_E.html.