10GEMAC IP Core (for Xilinx) introduction

Super low-latency 10GbE MAC core

DG-10GEMAC-IP Core Overview

- 10GEMAC inserted between DG IP Core and 10G PHY.

DG-10GEMAC-IP Core Block Diagram
Advantage of DG-10GEMAC-IP Core

- Dedicated MAC IP Core for TOE10G-IP/UDP10G-IP.
- Highly compatible with Xilinx MAC (EF-DI-25GEMAC).
- Super low-latency, Tx=19.2nsec, Rx=44.8nsec.
- Minimized resource usage, ½ of Xilinx MAC Core.
- Very low price, 1/5 of Xilinx MAC Core.

MAC function and Interface

- Provided MAC function
  - Implement necessary MAC feature for DG IP Core.
  - FCS (CRC-32) calculation.
  - Preamble, SFD, and FCS insertion to Tx packet.
  - SFD detection and FCS check from Rx packet.
- Interface
  - PHY side interface is 64bit XGMII (156.25MHz).
  - Controller side interface is AXI4-Stream.
DG-10GEMAC-IP Core Advantage 1

- Dedicated MAC core for TOE10G-IP/UDP10G-IP
  - Reference design using real Xilinx board available with combination of TOE10G-IP or UDP10G-IP Core.
  - Highly compatible with Xilinx MAC (EF-DI-25GEMAC).
    (Can swap with Xilinx 10GEMAC with minimal additional circuit.)
  - Very low cost with necessary feature only for DG IP Core.

DG-10GEMAC-IP Core Advantage 2

- Super low-latency
  - Optimized by limitation to the combination with DG IP Core.
  - Especially Rx latency is less than half of Xilinx MAC Core.

<table>
<thead>
<tr>
<th></th>
<th>Tx latency</th>
<th>Rx latency</th>
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<tbody>
<tr>
<td>Xilinx 10GEMAC</td>
<td>19.2ns (3clk)</td>
<td>115.2ns (18clk)</td>
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<tr>
<td>DG-10GEMAC-IP</td>
<td>19.2ns (3clk)</td>
<td>44.8ns (7clk)</td>
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10GEMAC latency comparison (clk freq.=156.25MHz)
DG-10GEMAC-IP Core Advantage 3

- Minimum resource usage
  - About half the resource consumption of Xilinx MAC by omitting MAC function that is not used in DG IP Core.

<table>
<thead>
<tr>
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<th>CLB LUTs</th>
<th>CLB Registers</th>
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<tr>
<td>Xilinx 10GEMAC</td>
<td>3498</td>
<td>3291</td>
<td>694</td>
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<td>DG-10GEMAC-IP</td>
<td>1873</td>
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10GEMAC resource usage comparison (Kintex-Ultrascale)

- Use only with 10GbE Core from DesignGateway
  - Cannot connect with 3rd party network IP Core.

- Some restrictions
  - Not provide zero-padding insertion or removal.
    (Needs to insert/remove zero-padding at user circuit if necessary.)
  - Top byte of Rx packet must position to byte lane0 or 4.
    (It is not the problem in normal use)
Conclusion

- Best match with TOE10G-IP/UDP10G-IP Core
  - Minimum latency, resource usage, and cost.
  - Maximum performance
  - Easy to swap with Xilinx MAC core
    (Immediately can swap when Xilinx EMAC feature become necessary.)
- Reference design for real operation available
  - Vivado Project for Xilinx evaluation board
  - Can check real performance

For more detail

- Detailed documents available on the web site.
- Contact
  - Design Gateway Co., Ltd.
  - E-mail: ip-sales@design-gateway.com
  - FAX: +66-2-261-2290
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