USB3.0-PCIe conversion adapter board [AB13-USB3PCIE] Manual [Ver1.1E]

Introduction

Thank you for choosing USB3.0-PCIe conversion adapter board [Part Number：AB13-USB3PCIE] (“adapter board” in this manual).

The adapter board converts USB3.0 A-type connector interface into PCE-Express socket connector interface, and connects USB3.0 SuperSpeed signal with PCIe transceiver channel of FPGA on Altera/Xilinx evaluation board. The adapter board can be applicable to evaluate USB3.0-IP external PHY-less (SuperSpeed direct connection) version provided from DesignGateway.

The adapter board mounts 8-lane PCE-Express socket connector and 6 USB3.0 A-type connectors, so that it can provide 6 channels USB3.0 SuperSpeed connection resource. 2 channels (CN1 and CN2) have USB3.0 re-driver device (SN65LVPE502CP from T.I) so it can connect with external device by USB3.0 standard compliant signal. Another 4 channels (CN3-CN6) are direct connection with transceiver of FPGA so SuperSpeed signal characteristic will depend on the connected transciver.

Note that both Altera and Xilinx do not officially support USB3.0 SuperSpeed by their transceiver, so that FPGA vendor cannot guarantee SuperSpeed operation.

The feature of the adapter board is as follows.

- Connects with PCI-Express 8-lane (4-lane/1-lane are also possible) of FPGA evaluation board.
- Converts USB3.0 SuperSpeed signal into PCIe transceiver signal.
- Total 6 SuperSpeed channels available, 2 channels have re-driver device and the other 4 channels are direct connection.
- Jumper header for re-driver device parameter setting.
- GPIO connection to general FPGA I/O via 14-core ribbon cable and LCD I/F on FPGA board.
- +5V Vbus power supply in Host-mode from 4-pin ATX power supply.
- In Host-mode, FPGA I/O can control each USB channel Vbus On/Off individually.
- In Device-mode, FPGA I/O can detect each USB channel Vbus status individually.
- Vbus status display LED for each USB channels individually.
- 125MHz low-jitter LVDS clock for SuperSpeed reference clock supply.

Because the adapter board is designed for DesignGateway USB3.0-IP evaluation only, DP/DM signal is left open and not connected to any part. So it cannot use for Legacy USB evaluation such as USB2.0/1.1.

USB3.0 SuperSpeed requires 5Gbps bandwidth, so this adapter board is not useful if FPGA transceiver speed is less than 5Gbps.

Package List

The adapter board includes following items in its product.

- AB13-USB3PCIE adapter baord: 1pcs
- 14-core ribbon cable to connect with LCD connector on the FPGA evaluation board: 1pcs
- Jumper socket for Vbus connection settings and re-driver parameter settings: 18pcs

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Board Outline

The adapter board size is 50mm width and 95mm length.
Following figure-1 shows board outline.

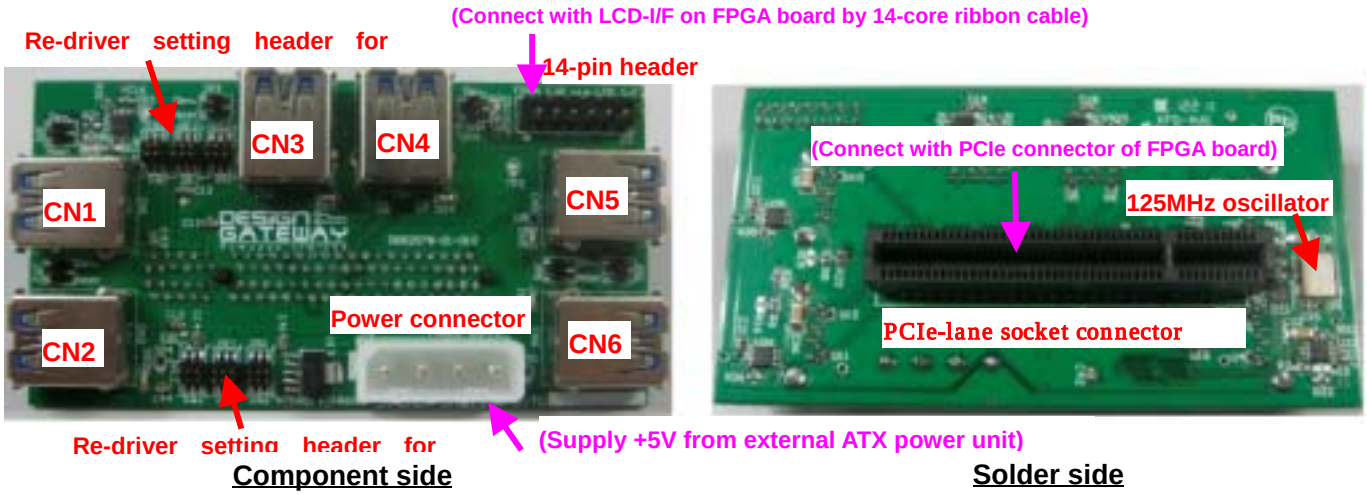

Figure 1: AB13-USB3PCIE board outline

Board Connection

[1] Connection to the PCIe connector on the FPGA board

Connect the adapter board with PCIe 8-lane card-edge connector on the FPGA board. It also can connect with 4-lane or 1-lane conector, however in this case, USB channel count is limited to 4 or 1 respectively.

[2] Connection to the ATX power supply unit

To evaluate USB3.0 SuperSpeed operation, the adapter board requires +5V power supply from external ATX power unit. Use 4-pin power connector for power supply. (+12V is not used in this board.) Without +5V power supply, the adapter board cannot operate because 125MHz oscillator, re-driver device, and power switch (to control Vusb supply in Host-mode) needs +5V.

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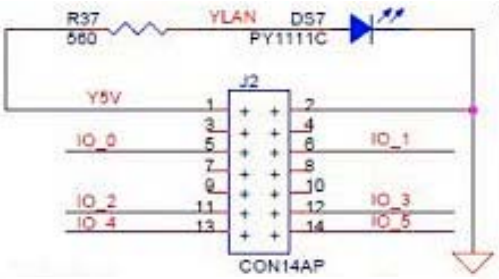
[3] Connection to the LCD connector on the FPGA board by ribbon cable

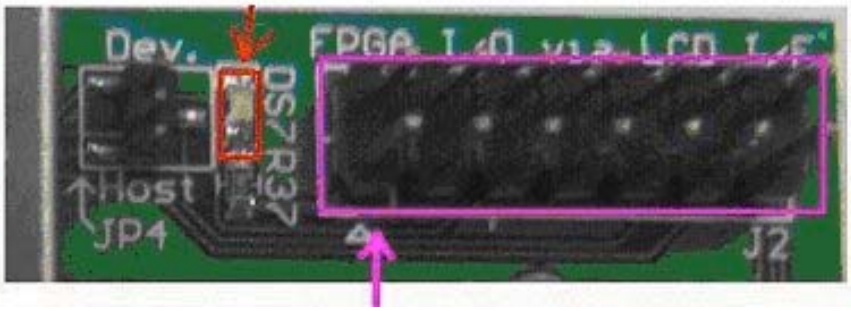
It is necessary to control Vbus (in Host-mode) or monitor Vbus (in Device-mode) by GPIO of FPGA. Use attached 14-core ribbon cable to connect LCD connector on the FPGA board and 14-pin header on the adapter board.

When connection via 14-core ribbon cable is correct, DS7 LED on the adapter board will be ON when FPGA board is powered up. If DS7 does not emit light, cut off FPGA board power immediately and check connection.



When connection to LCD connector on the FPGA board is correct, pin#1 is +5V and pin#2 is GND so DS7 LED will be ON.

DS7 will be ON if connection via ribbon cable is correct



pin#1 position of 14-pin header

Figure 2: Cable connection check by DS7

As explained in the following section, ribbon cable connection direction is different between Altera FPGA board (StratixIV GX board in this description) and Xilinx FPGA board (KC-705 in this description).

[3-1] Connection to the LCD connnector on Altera StratixIV GX board

Following figure 3 shows LCD connector schematic of StratixIV GX board.

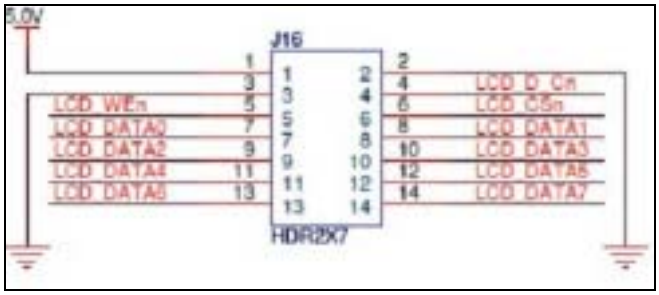


Figure 3: LCD connector schematic of StratixIV GX board

To connect with LCD connector on the StratixIV GX board, connect pin#1 of 14pin-header on this adapter board with pin#1 of LCD connector. So same pin number at both connectors connects each other to make straight connection.

Following table 1 shows correct connection.

The adapter board		StratixIV GX board	
Pin #	Signal	Pin #	Signal
1	High side of DS7	1	5.0V
2	GND(Low side of DS7)	2	GND
5	GPIO for CN1	5	LCD_Wen
6	GPIO for CN2	6	LCD_CSn
11	GPIO for CN3	11	LCD_DATA4
12	GPIO for CN4	12	LCD_DATA5
13	GPIO for CN5	13	LCD_DATA6
14	GPIO for CN6	14	LCD_DATA7

Table 1: Connection for StratixIV GX board

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[3-2] Connection to the LCD connnector on Xilinx KC-705 board

Following figure 4 shows LCD connector schematic of KC-705 board.

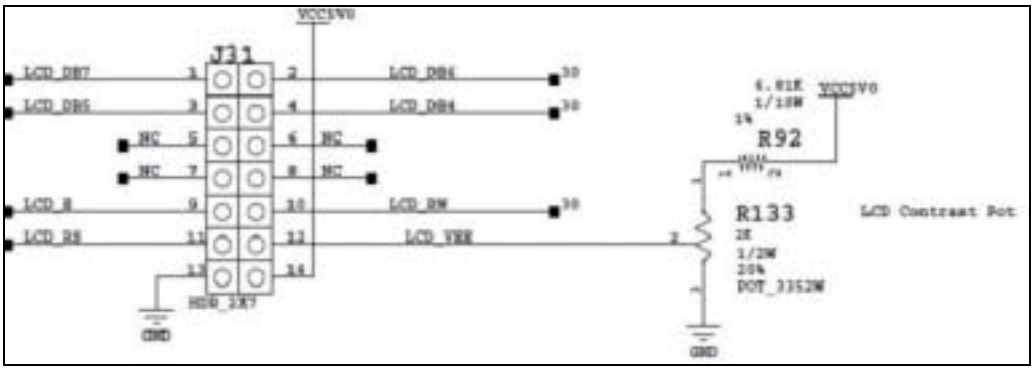

Figure 4: LCD connector schematic of KC-705 board

To connect with LCD connector on the KC-705 board, connect pin#1 of 14pin-header on this adapter board with pin#14 of LCD connector. So pin number connection at each connector is reversed to make cross connection.

Following table 2 shows correct connection.

The adapter board		StratixIV GX board	
Pin #	Signal	Pin #	Signal
1	High side of DS7	14	VCC5V0
2	GND(Low side of DS7)	13	GND
5	GPIO for CN1	10	LCD_RW
6	GPIO for CN2	9	LCD_E
11	GPIO for CN3	4	LCD_DB4
12	GPIO for CN4	3	LCD_DB5
13	GPIO for CN5	2	LCD_DB6
14	GPIO for CN6	1	LCD_DB7

Table 2: Connection for KC-705 board

Connection between PCIe and USB

Following table 3 shows connection between each PCI-Express lane and USB3.0 connector.

PCIe lane#	USB connector	Remark
lane#0	CN1	Connect via U15 re-driver device.
lane#1	CN2	Connect via U16 re-driver device.
lane#2	CN3	Direct connection between PCIe and USB3.0
lane#3	CN4	Direct connection between PCIe and USB3.0
lane#4		Loop back connection of TX-RX in PCIe
lane#5		Loop back connection of TX-RX in PCIe
lane#6	CN5	Direct connection between PCIe and USB3.0
lane#7	CN6	Direct connection between PCIe and USB3.0

Table 3: Connection between PCIe and USB connector

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Jumper Settings

The adapter board mounts 8 jumper headers in total. Use jumper socket attached to the product.

[1] Vbus settings

In each USB connector (CN1-CN6), Vbus setting is selectable between Host-mode or Device-mode. Use JP1-JP6 for CN1-CN6 setting respectively.

When jumper socket is set to [1-2], it can supply +5V to Vbus for Host-mode. Moreover, Vbus On/Off control by power switch (AP2411MP-13.) is possible by GPIO control from FPGA.

(Refer to http://www.diodes.com/datasheets/AP24x1.pdf for power switch specification.)

When jumper socket is set to [2-3], GPIO of FPGA can monitor power supply status of Vbus.

Follow [Host] [Dev] label near by jumper header for socket position.

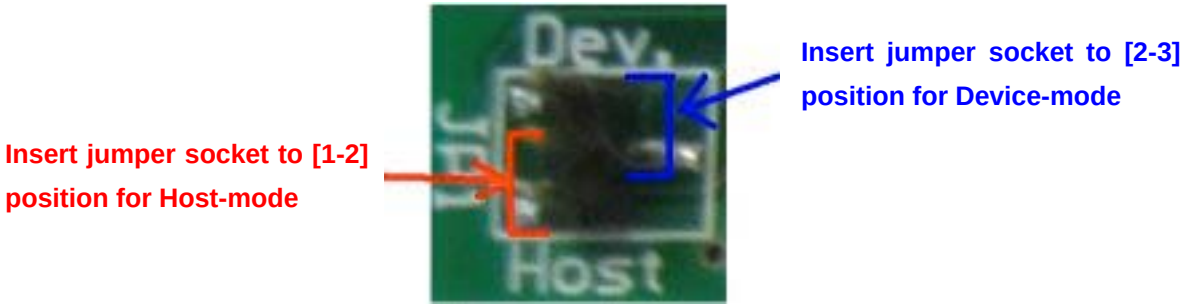

Figure 5: Vbus settings by jumper socket

[2] Re-driver parameter settings

USB3.0 SuperSpeed signal of CN1 and CN2 is transferred through re-driver device U15 and U16 respectively. User can select de-emphasis (DE), equalization (EQ), and output swing(OS) parameter by JP11 and JP12 jumper setting.

In each parameter, value is set to high if socket is inserted into center pin and [+] (plus) pin. Value is set to low if socket is inserted into center pin and [-] (minus) pin. Value is set to default if socket is not set.

Refer to SN65LVPE502CP datasheet (http://www.ti.com/product/sn65lvpe502cp) for more detailed parameter description.

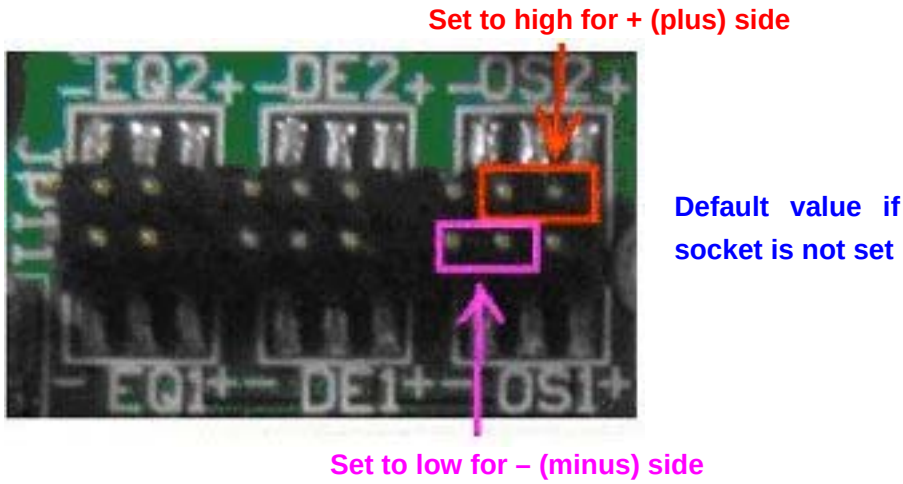

Figure 6: Re-driver parameter setting by jumper

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Disclaimer

The manufacturer of the product limits liability in following situation or use.

- Any damage to the connected USB device via USB interface of the adapter board.
- Any damage to the FPGA evaluation board connected with the adapter board.
- DesignGateway does not guarantee USB3.0 super-speed operation.

[Contact]
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Revision History

Revision	Date	Description
1.1E	07-May-2013	Initial English manual

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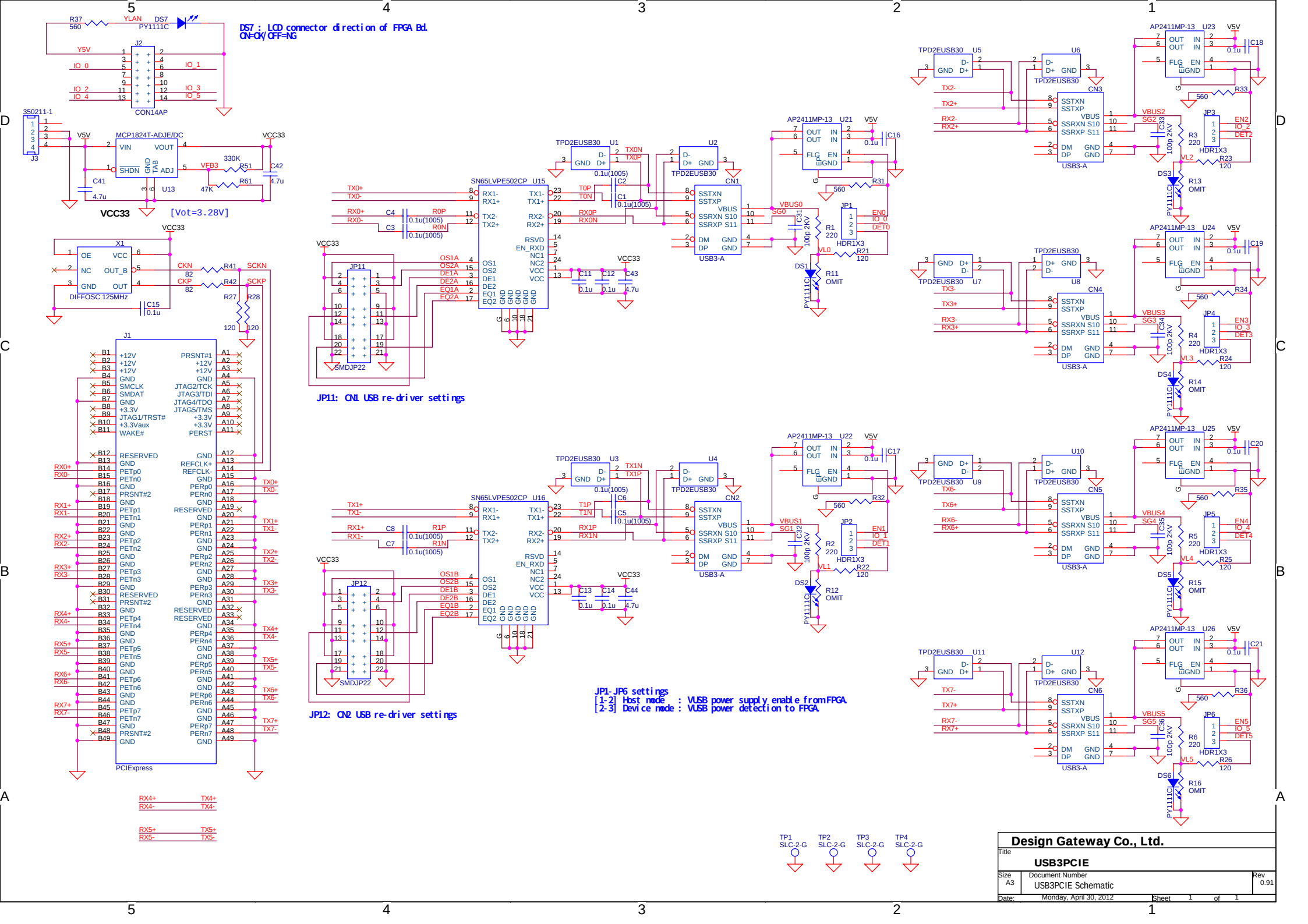
DS7 : LCD connector direction of FPGA Bd.
CN=OK/OFF=NG
JP11: CN1 USB re-driver settings
JP12: CN2 USB re-driver settings
JP1-JP6 settings
[1-2] Host mode : VUSB power supply enable from FPGA
[2-3] Device mode : VUSB power detection to FPGA
VCC33
[Vot=3.28V]
PCIExpress
Design Gateway Co., Ltd.
USB3PCIE
USB3PCIE Schematic
Monday, April 30, 2012