PCIe Crossover adapter board [AB16-PCIeXOVR] Manual [Ver1.0E]

Introduction

Thank you for choosing PCIe Crossover adapter board [Part Number: AB16-PCIeXOVR] ("adapter board" in this manual).

This adapter board supports 1/4/8-lane PCIe (PC-Express) and converts between PCIe host and PCIe device, and can apply to FPGA evaluation board from Altera or Xililnx. The adapter board mounts two 8-lane PCIe socket connectors on both of component and solders side, and connects between TX pair and RX pair in each connector.

Generally, PCIe card-edge connector on FPGA evaluation board is assigned as device function and can insert into PCIe socket of general PC so that FPGA can operate as a PCIe device. However, when FPGA evaluation board is connected to the component side socket of this adapter board and some PCIe device is connected to the solder side socket, FPGA with PCIe host function in its logic can communicate with connected PCIe device. So this board is ideal for PCIe host application development using FPGA evaluation board.

This adapter board is also necessary when user evaluates APS-IP core from DesignGateway.

The feature of the adapter board is as follows.

- Host side socket can accept general FPGA evaluation board with PCI-Express 8/4/1-lane.
- Device side socket can accept PCIe 8/4/1-lane device such as SSD.
- Mounts PCIe Low-jitter reference clock (HSCL differential signal, 100MHz default) source.
- Same PCIe clock is supplied to both host and device side.
- Side-band signal between host and device connection is configurable by jumper socket.
- 2.5V/3.3V power supply for side-band pin header for user original daughter board on the header.
- Flexible hardware reset with manual reset function for host and device reset usage.
- On-board On-Off power supply switch.
- Accessory power distribution cable assembly for standard Altera/Xilinx DC P.S (power supply).

Package List

The adapter board includes following items in its product.

- AB16-PCIeXOVR adapter board: 1pcs
- Cable assembly with LDO for Altera DC P.S.: 1pcs.
- Cable assembly for Xilinx DC P.S.: 1pcs

Board Outline

The adapter board size is 40mm width and 75mm length.
Following figure-1 and 2 shows component side and solder side respectively.

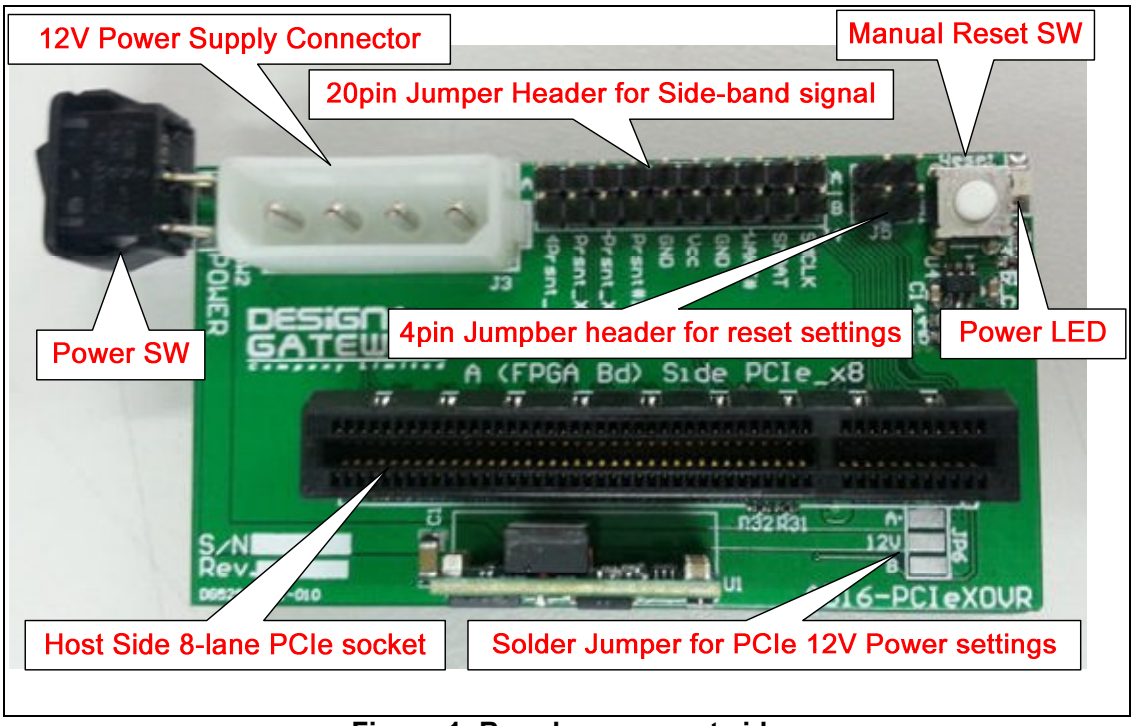


Figure-1: Board component side

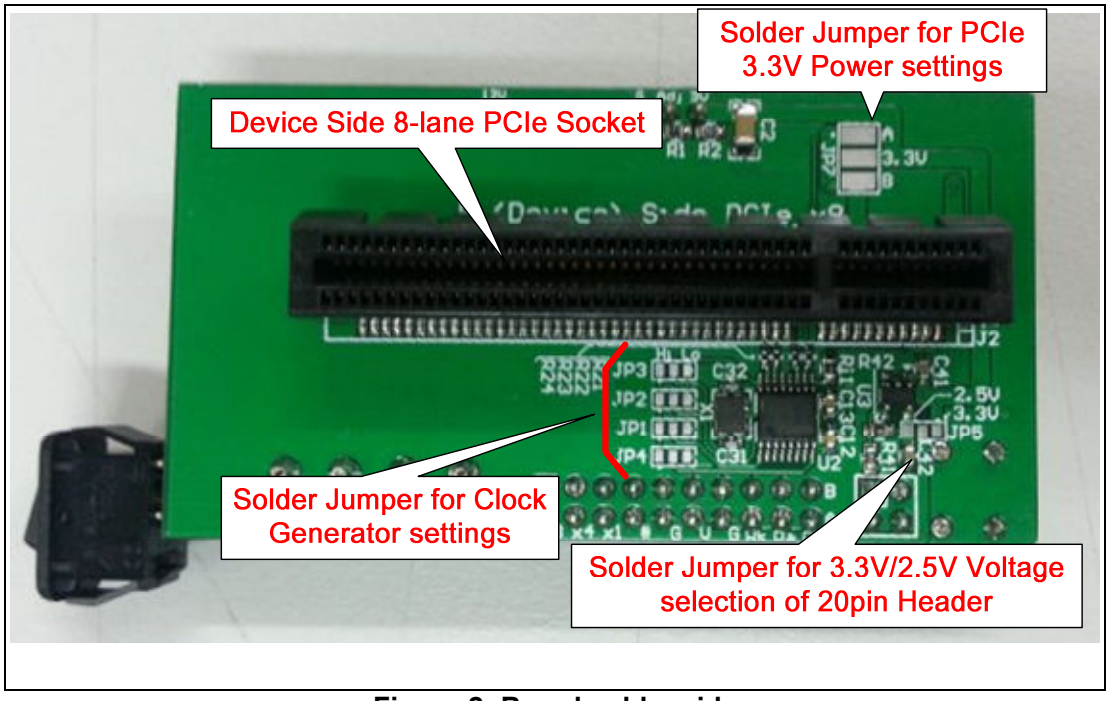


Figure-2: Board solder side

This product also includes power distribution cable assembly for both Altera and Xilinx. By using this cable, Altera/Xilinx DC P.S. can supply power to both FPGA evaluation board and this adapter board concurrently. Because Altera standard DC P.S. is not regulated power supply, 12V LDO is used for Altera cable assembly. Figure-3 and 4 shows power distribution cable assembly for Altera and Xilinx respectively.

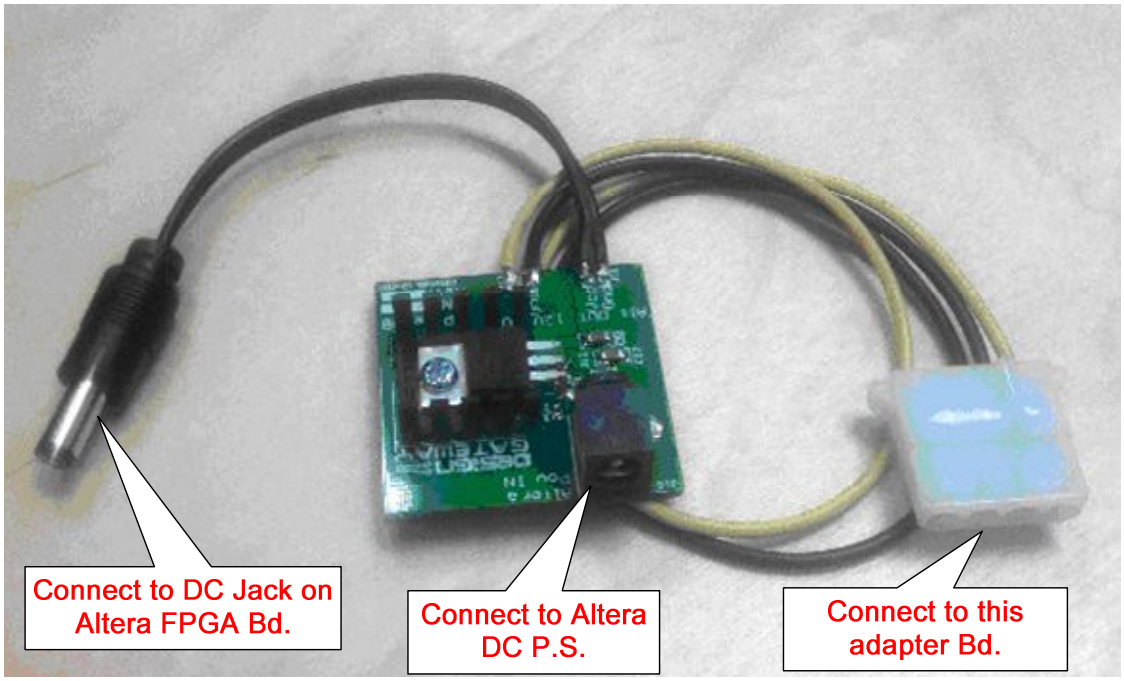


Figure-3: Power distribution cable for Altera

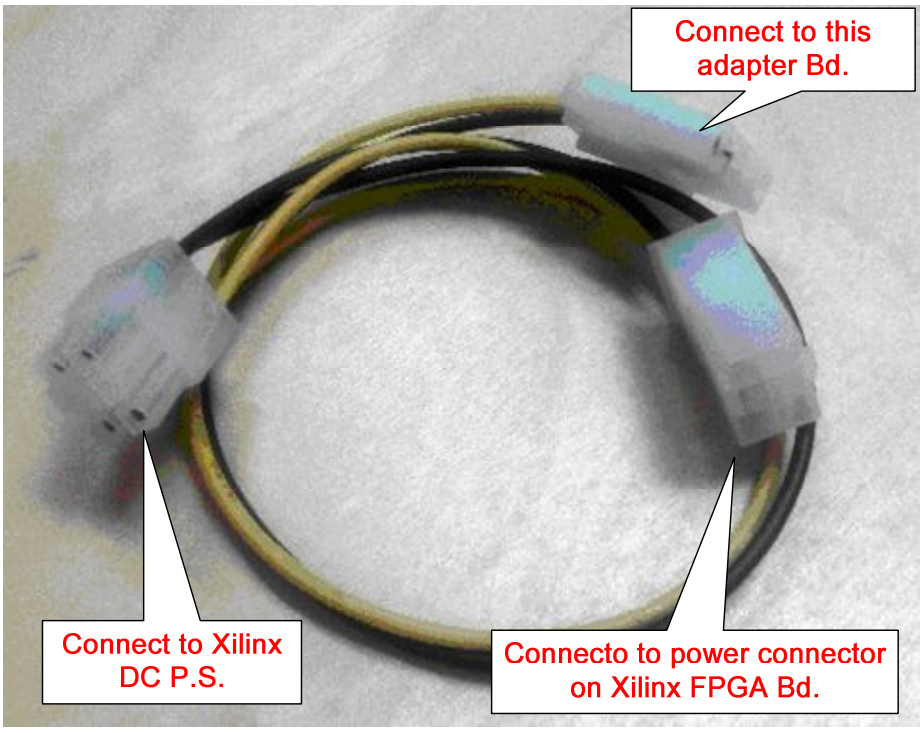


Figure-4: Power distribution cable for Xilinx

Jumper Setting

This adapter board mounts two pin headers of J4 (20pin) and J5 (4pin), and also has 7 solder patterns of JP1-JP7 so that they can be set by the user. Each pin header, solder pattern and related circuit block are described below.

[1] J4 (20pin header)

J4 is 2x10 pin header shown in figure-5 below, and connects PCIe side-band signals of host side and device side. It also prepares Vcc power supply pin (Pin#11, #12) which is selectable between 3.3V and 2.5V, so user can build original daughter board on this pin header using this power supply. Figure-5 shows pin number definition, even number pin at outer side is for host (A) side, and odd number pin at inner side is for device (B) side. When user set 2.54mm-pitch short plug on the same row of J4, it can directly connect same PCIe side-band signal between host and device. For more detailed J4 pin assignment, refer to the schematic in the later part of this document.

Figure-5: J4 pin header for PCIe side-band signal

[2] J5 (4pin header)

J5 is 2x2 pin header shown in figure-6 below, and selects PCIe reset signal. Figure-6 also shows pin number definition. By using 2.54mm-pitch short plug, user can select following reset configuration. This adapter board mounts following reset IC (U4) which monitors 3.0V threshold at 3.3V power supply, and reset delay time is 100msec. When user press reset switch (SW1), it can manually generate reset signal.

IC Vendor: T.I Part Number: TPS3808G01DBV

J5 settings:

1-2 Short: Directly connect reset signal between host and device.
1-3 Short: Connect reset output from Reset IC (U4) to reset signal of PCIe device side.
2-4 Short: Connect reset output from Reset IC (U4) to reset signal of PCIe host side.

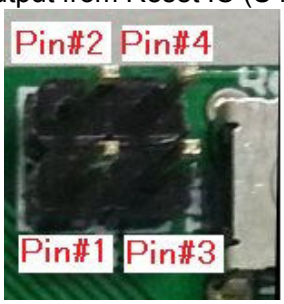


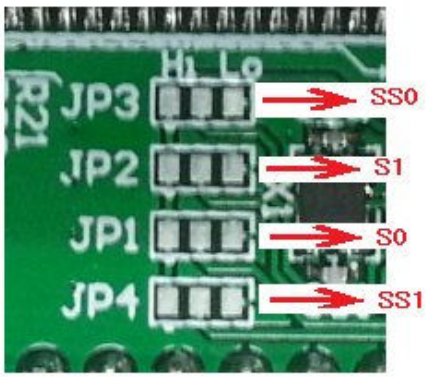
Figure-6: J5 pin header for PCIe reset

[3] JP1-JP4 (Solder pattern)

JP1-JP4 is solder pattern for clock parameter settings of PCIe clock generator IC, and setting description is shown at figure-7 below. This adapter board mounts following clock generator IC.

Vendor: IDT Part Number: IDT5V41235PGG

At JP1-JP4 pattern of figure-7, center pad is connected to S0, S1, SS0, and SS1 pin of the clock generator respectively, and can set parameter by solder short to left side pad (Hi = Vcc) or right side pad (Lo=GND). Factory default setting is that only JP1 is set Hi and JP2-JP4 are set Lo, so that PCIe clock frequency is 100MHz and no SSC.



Output Select Table 1 (MHz) - TSSOP Only

S1	S0	CLK(1:0), $\overline{CLK(1:0)}$	
0	0	25M	← Default setting
0	1	100M	
1	0	125M	
1	1	200M	

Spread Selection Table 2 - TSSOP Only

SS1	SS0	Spread%	
0	0	No Spread	← Default setting
0	1	Down -0.5	
1	0	Down -0.75	
1	1	No Spread	

Figure-7: JP1-JP4 solder pattern for PCIe clock generator setting

[4] JP5 (Solder pattern)

JP5 selects Vcc power supply voltage for pin11-12 of J1 pin header, and shown at figure-8 below. When user builds original daughter board to mount on J1, Vcc (pin11-12) supply power is available with 3.3V or 2.5V set by this JP5. In figure-8, center pad is connected to pin11-12 of J1, so 2.5V is selected when short with left side pad and 3.3V is selected when short with right side pad. Factory default setting is 3.3V.

Caution: Do never short all three pads of JP5, otherwise, adapter board shall be damaged!

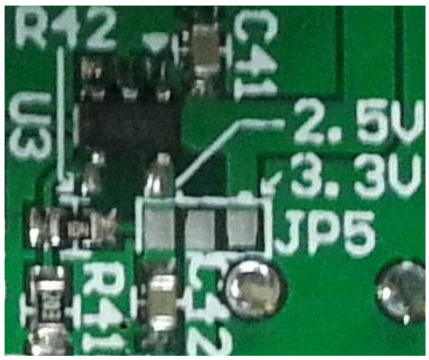


Figure-8: JP5 solder pattern for Vcc voltage setting

[5] JP6 (Solder pattern)

JP6 on the component side selects 12V power supply to PCIe host side and device side. In the figure-9, center pad is connected to 12V power supply source of this adapter board. And short to the upper pad by solder can supply 12V to the host (A) side PCIe power supply, while short to the lower pad can supply 12V to the device (B) side PCIe power supply. Factory default setting is short between center and lower pad, so 12V is supplied to PCIe device side only.

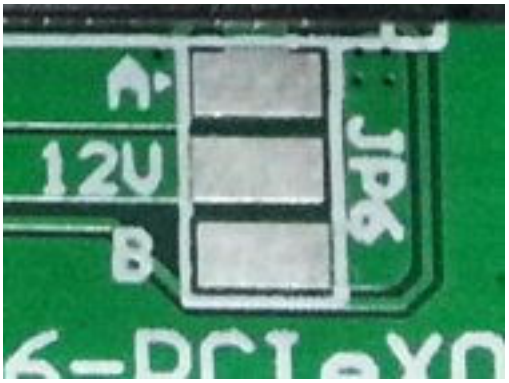


Figure9:: JP6 soldering can select 12V PCIe power supply to host/device side

[6] JP7 (Solder pattern)

JP7 on the solder side selects 3.3V power supply to PCIe host side and device side. In the figure-10, center pad is connected to 3.3V power supply source of this adapter board. And short to the upper pad by solder can supply 3.3V to the host (A) side PCIe power supply, while short to the lower pad can supply 3.3V to the device (B) side PCIe power supply. Factory default setting is short between center and lower pad, so 3.3V is supplied to PCIe device side only.

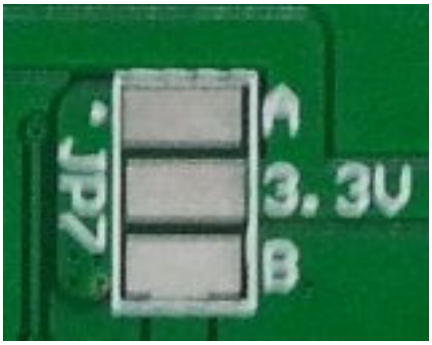


Figure-10: JP7 soldering can select 3.3V PCIe power supply to host/device side

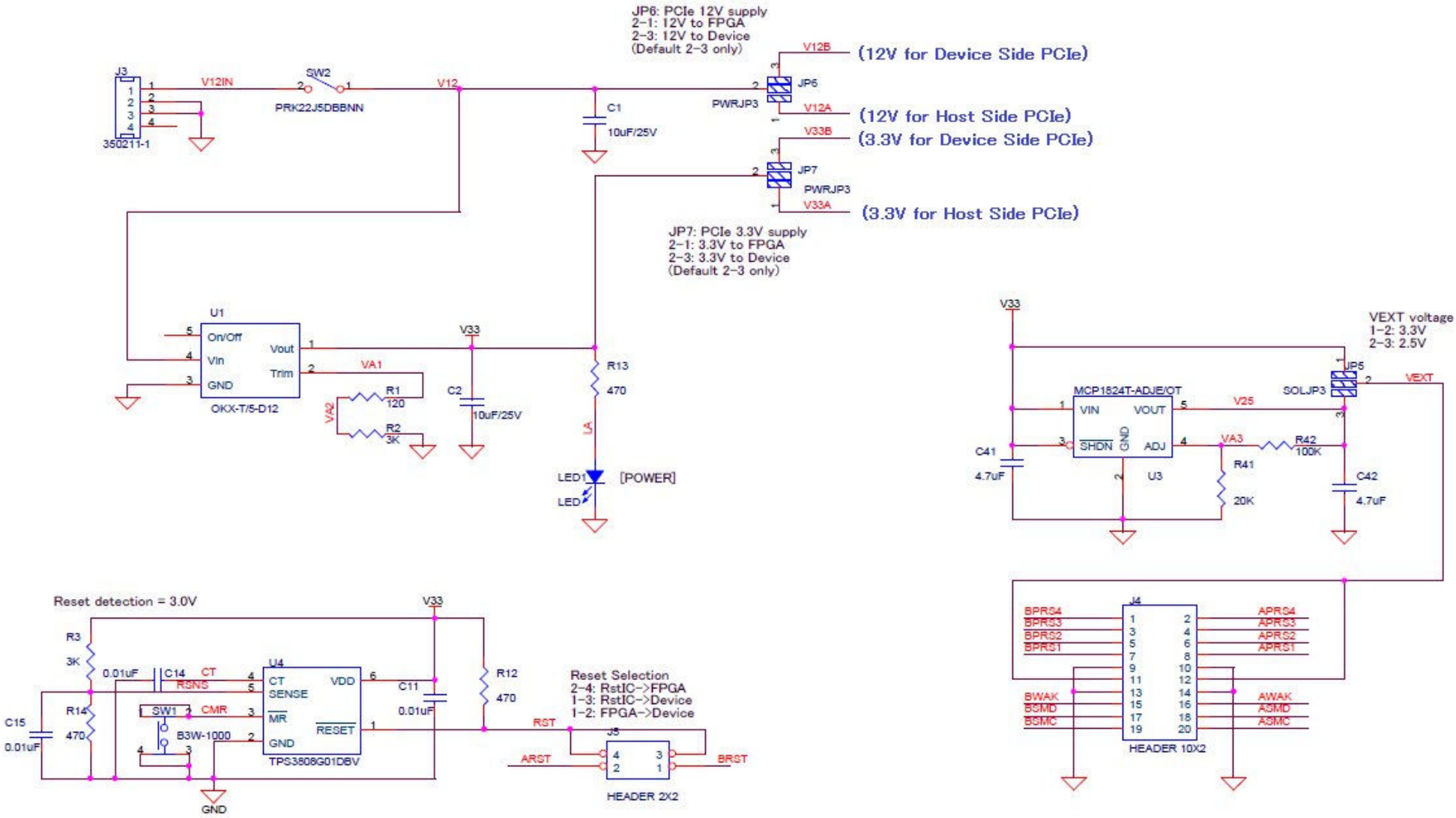


Figure-11: Adapter board schematic (1/2)

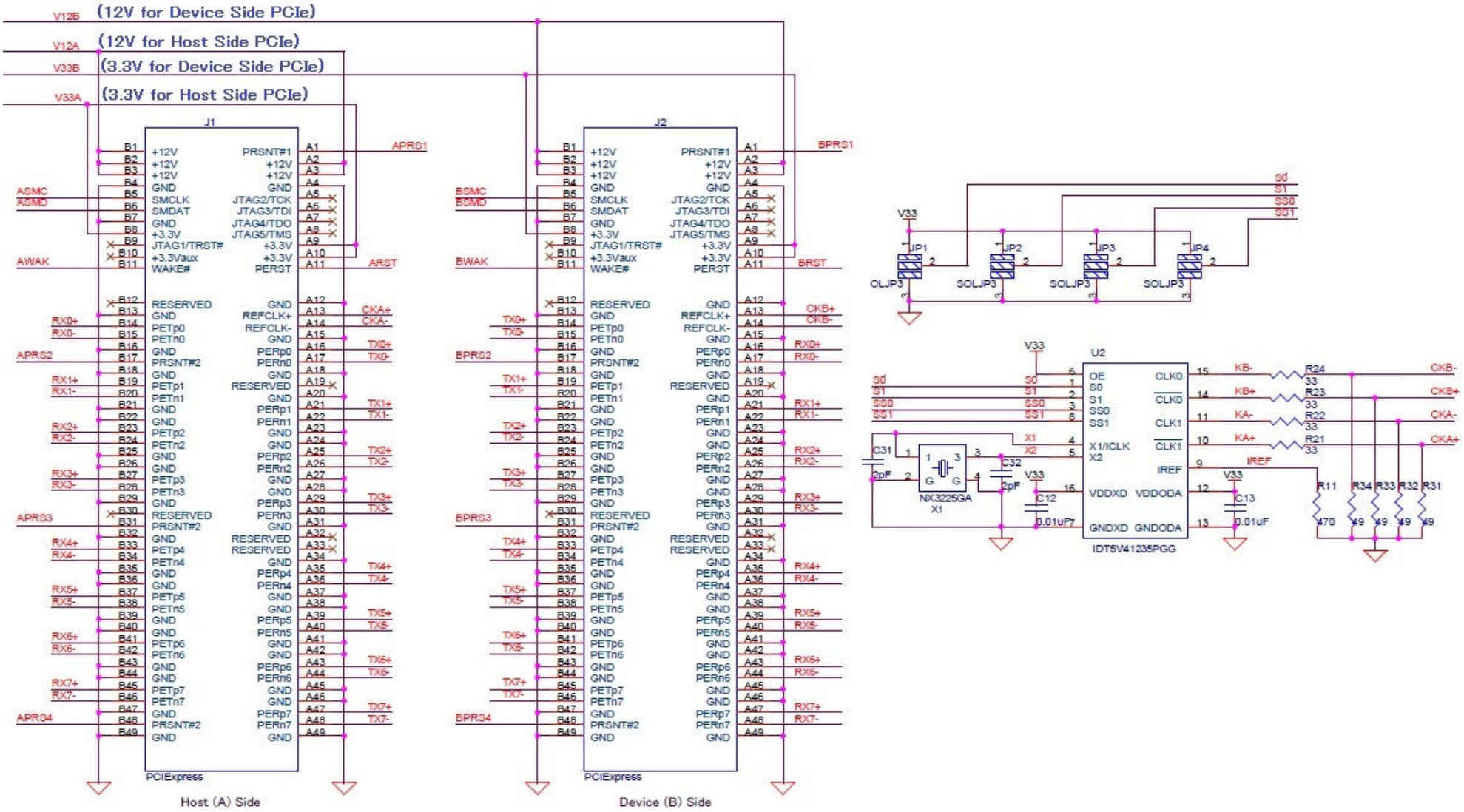


Figure-12: Adapter board schematic (2/2)

Disclaimer

The manufacturer of the product limits liability in following situation or use.

- Any damage to the FPGA evaluation board connected with the adapter board.
- Any damage to the PCIe device connected with the adapter board.
- DesignGateway does not guarantee PCIe operation between FPGA board and PCIe device via the adapter board.

[Contact]
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Revision History

Revision	Date	Description
1.0J	17-Sep-2015	Initial Japanese manual
1.0E	09-Oct-2015	Initial English manual