# E1.S-PCIe adapter board [AB21-E1PCI] Manual

**[ Rev. 1.0E]**

## About AB21-E1PCI

This product is an adapter board exclusively for evaluating the NVMe-IP core manufactured by Design Gateway (DG) and for customer design prototyping using said IP core.
Learn more about DG NVMe-IP core for AMD FPGAs | Learn more about DG NVMe-IP core for Altera FPGAs

Since this product is a dedicated item for the DG NVMe-IP core, if the operating environment does not include the DG NVMe-IP core, the operating guarantee of this product and all technical support, including Q&A, are excluded from the seller's responsibility; in such cases, please use products from other companies.

## Introduction

The AB21-E1PCI E1.S-PCIe conversion adapter (hereinafter referred to as the "adapter") is a dedicated adapter board for verifying actual hardware operation using the DG NVMe-IP core. It can be applied to various FPGA evaluation boards supported by the DG NVMe-IP core and is used for actual hardware evaluation of the IP core or user product development using the core.

Four E1.S connectors are mounted on the component side of the adapter board to accommodate up to four E1.S SSDs. On the solder side, a 16-lane PCIe (PCI Express) connector is mounted, and lanes 3-0/7-4/11-8/15-12 connect to the SSDs mounted on CN1/CN2/CN3/CN4, respectively. Proper operation at PCIe Gen5 speed has been confirmed on actual hardware for all channels.

The adapter includes a low-jitter clock generator and reset circuitry to provide clock and reset signals to PCIe and E1.S SSDs. Power for the adapter and E1.S SSDs is provided by a standard 6-pin PCI Express auxiliary power supply.

The product includes a support stand that securely holds up to four SSD drives connected to the adapter, maintaining reliable electrical connections.

The adapter with E1.S SSDs and the support stand is shown in Figure 1 below.

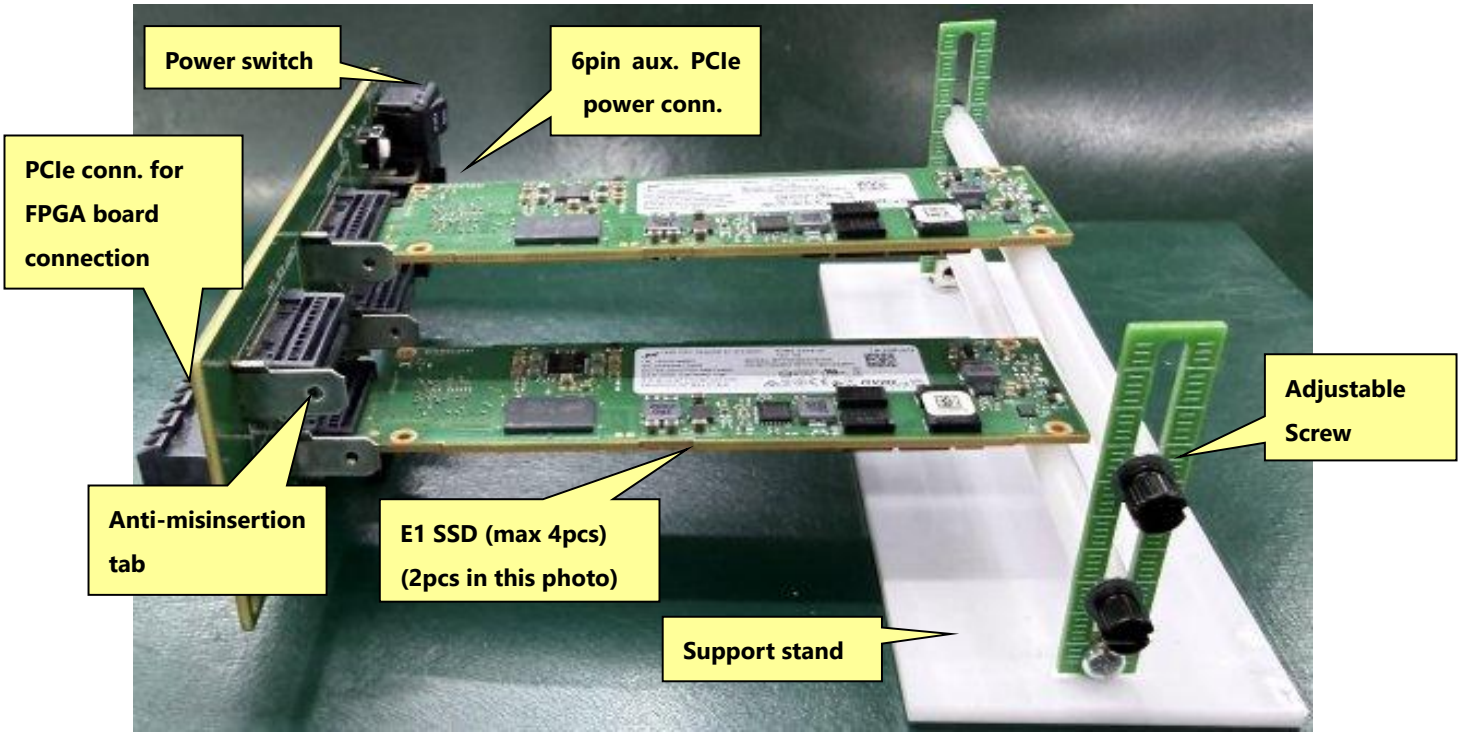



**Figure-1: AB21-E1PCI adapter with E1.S SSDs and support stand**

The features of this adapter are shown below.

- Expansion adapter board for E1.S SSD with 16-Lane PCI Express support
- Read/write access between FPGA and E1.S SSD in PCIe Gen5, confirmed in actual device operation
- Up to four E1.S SSDs can be installed simultaneously (CN1 and CN3 support E1.S SSDs up to 15 mm thick)
- Power is supplied at +12V from a standard external 6-pin PCIe auxiliary power supply
- Power supply to the adapter and E1.S SSDs can be controlled ON/OFF with a switch
- PCIe standard 100MHz low-jitter clock source mounted on the adapter
- Supplies low-jitter 100MHz differential clock signals of the same phase to PCIe and four SSDs
- Reset is selectable between PCIe-SSD direct connection and reset output on the adapter board via jumper socket

## Adapter outline

The adapter board size is 120 mm wide and 40 mm high. The component side and the solder side of the board are shown in Figure 2 and Figure 3, respectively.

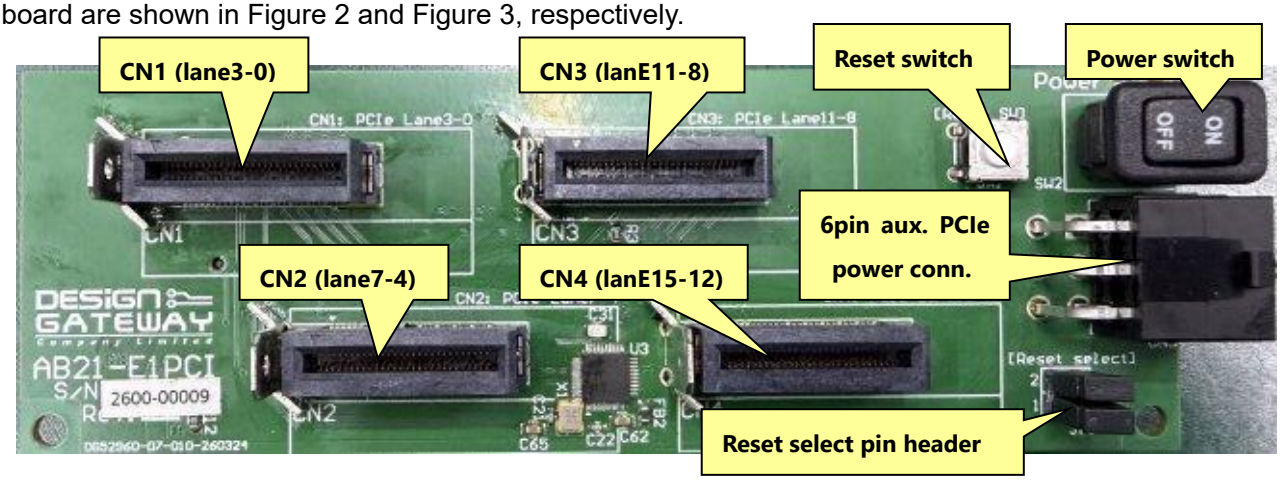



**Figure-2: adapter board component side**

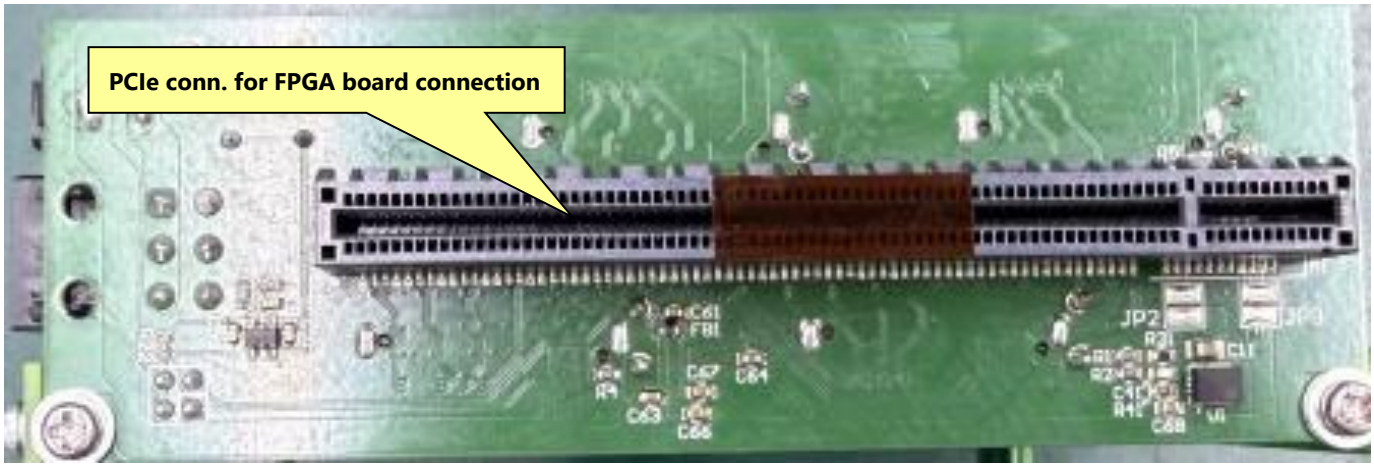



**Figure-3: adapter board solder side**

## Power Supply and Anti-Misinsertion Tabs

This adapter power is supplied by +12V from a 6-pin type PCIe auxiliary power supply as shown in Figure 4. The power switch controls the power supply to the adapter and the installed SSDs. The power-on status can be checked with the LED next to the power connector. The +12V power supply is used to generate a +3.3V power supply with a regulator inside the adapter, but +3.3V power is not supplied to the E1.S SSDs or +3.3V power pins of the PCIe connector. Therefore, +3.3V power cannot be supplied to the connected FPGA board via the PCIe connector.
Anti-misinsertion tabs near each E1.S connector prevent critical damage from incorrect SSD insertion.

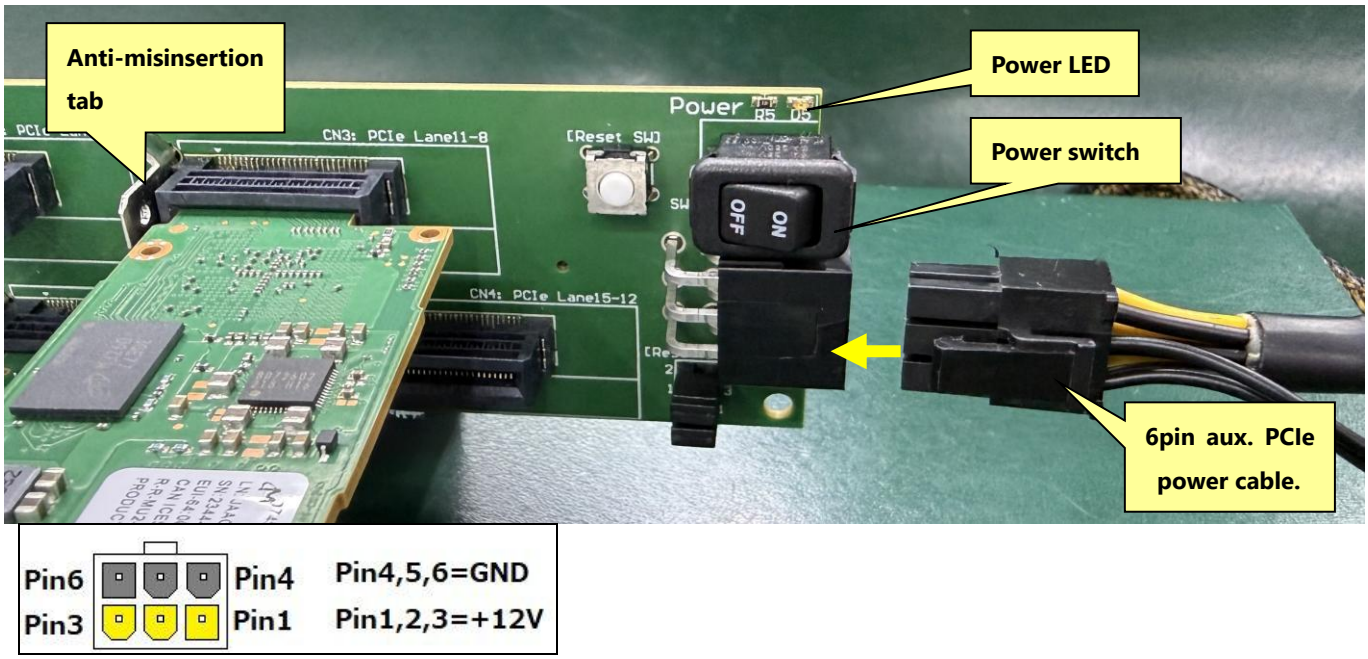



**Figure-4: Power switch, PCIe auxiliary power supply, and its pin assignment**

## Support Stand

Use the support stand to adjust the SSDs so that they are connected perpendicular to the adapter. The parts of the stand that contact the SSDs are made of insulating material.

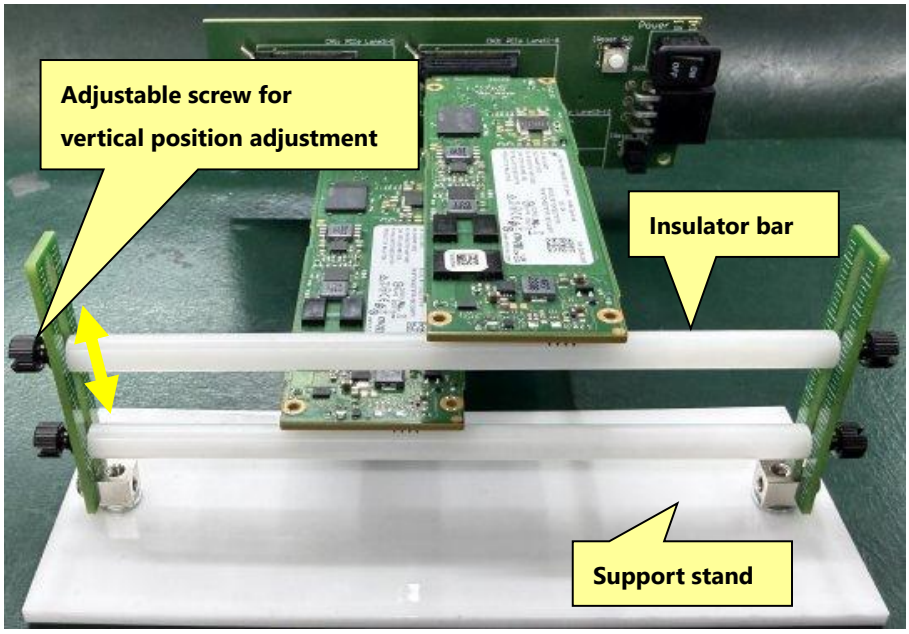


**Figure-5: Support stand**

## Clock circuit

The adapter is equipped with a low-jitter clock generator compliant with the PCIe standard and provides 100MHz differential clocks in the same phase to the PCIe clock pins (A13/A14) and all four E1.S SSD clock channels (B15/B14). The clock frequency is fixed at 100 MHz and cannot be changed.

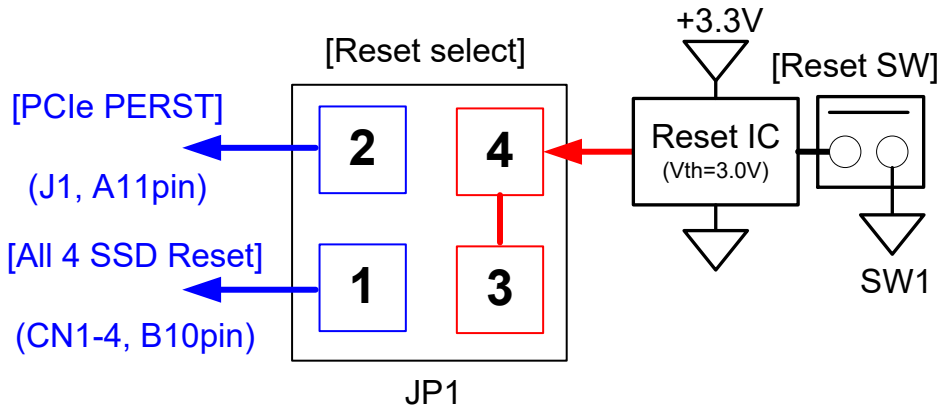
## Reset circuit

The adapter contains a reset IC that generates reset signals for PCIe and E1.S, a reset switch [SW1] for manually generating a reset signal, and a 2x2 jumper header [JP1] for selecting each reset system.

The reset IC constantly monitors the voltage level of the +3.3V power supply and outputs a low active reset signal when the voltage level falls below approximately 3.0V. It also generates a reset signal pulse of about 100msec when the reset switch is pressed.

The reset signal connection can be set as shown below by inserting a socket into the 2 x 2 4-pin header JP1 shown in Figure 6. (The factory default JP1 socket settings are the connections between 1-3 and between 2-4 as shown in Figure 6.)

Short between 1 and 3: Connects the reset IC output to the reset of all 4 E1.S SSDs (Pin# B10).
Short between 2 and 4: Connects the reset IC output to the PCI Express reset (Pin# A11)
Short between 1-2: Connects PCI Express reset (Pin#A11) to all 4 E1.S SSD resets (Pin#B10).



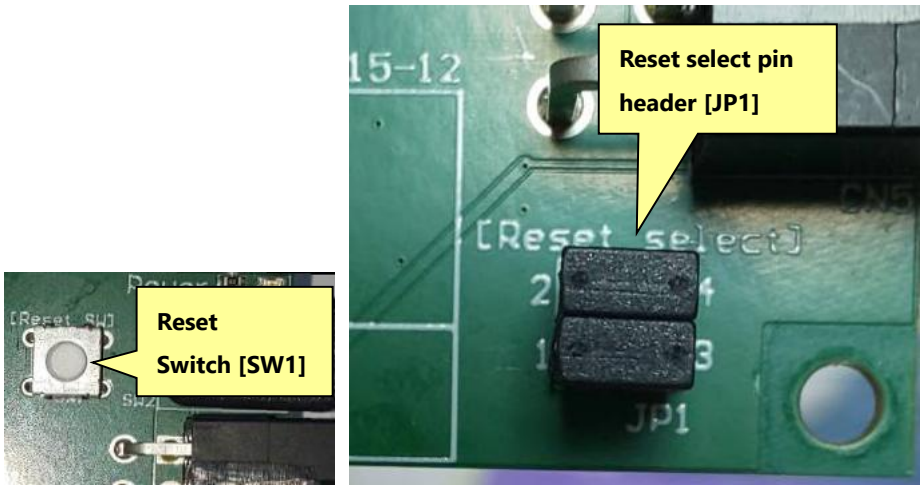




**Figure-6: Reset switch (SW1) and pin header (JP1) for reset connection settings**

## Connection between PCIe and each E1 SSD

The connection between each lane of the PCIe socket and the four E1 SSDs attached to CN1-CN4 in this adapter is as follows

| PCIe Lane# (signal direction) | PCIe signal name | PCIe Pin# | E1 Conn. | E1 Pin# |
|---|---|---|---|---|
| Lane0 Tx (FPGA->PCIe->E1) | PERp0/PERn0 | A16/A17 | CN1 | B18/B17 |
| Lane0 Rx (FPGA<-PCIe<-E1) | PETp0/PETn0 | B14/B15 | CN1 | A18/A17 |
| Lane1 Tx (FPGA->PCIe->E1) | PERp1/PERn1 | A21/A22 | CN1 | B21/B20 |
| Lane1 Rx (FPGA<-PCIe<-E1) | PETp1/PETn1 | B19/B20 | CN1 | A21/A20 |
| Lane2 Tx (FPGA->PCIe->E1) | PERp2/PERn2 | A25/A26 | CN1 | B24/B23 |
| Lane2 Rx (FPGA<-PCIe<-E1) | PETp2/PETn2 | B23/B24 | CN1 | A24/A23 |
| Lane3 Tx (FPGA->PCIe->E1) | PERp3/PERn3 | A29/A30 | CN1 | B27/B26 |
| Lane3 Rx (FPGA<-PCIe<-E1) | PETp3/PETn3 | B27/B28 | CN1 | A27/A26 |
| Lane4 Tx (FPGA->PCIe->E1) | PERp4/PERn4 | A35/A36 | CN2 | B18/B17 |
| Lane4 Rx (FPGA<-PCIe<-E1) | PETp4/PETn4 | B33/B34 | CN2 | A18/A17 |
| Lane5 Tx (FPGA->PCIe->E1) | PERp5/PERn5 | A39/A40 | CN2 | B21/B20 |
| Lane5 Rx (FPGA<-PCIe<-E1) | PETp5/PETn5 | B37/B38 | CN2 | A21/A20 |
| Lane6 Tx (FPGA->PCIe->E1) | PERp6/PERn6 | A43/A44 | CN2 | B24/B23 |
| Lane6 Rx (FPGA<-PCIe<-E1) | PETp6/PETn6 | B41/B42 | CN2 | A24/A23 |
| Lane7 Tx (FPGA->PCIe->E1) | PERp7/PERn7 | A47/A48 | CN2 | B27/B26 |
| Lane7 Rx (FPGA<-PCIe<-E1) | PETp7/PETn7 | B45/B46 | CN2 | A27/A26 |
| Lane8 Tx (FPGA->PCIe->E1) | PERp8/PERn8 | A52/A53 | CN3 | B18/B17 |
| Lane8 Rx (FPGA<-PCIe<-E1) | PETp8/PETn8 | B50/B51 | CN3 | A18/A17 |
| Lane9 Tx (FPGA->PCIe->E1) | PERp9/PERn9 | A56/A57 | CN3 | B21/B20 |
| Lane9 Rx (FPGA<-PCIe<-E1) | PETp9/PETn9 | B54/B55 | CN3 | A21/A20 |
| Lane10 Tx (FPGA->PCIe->E1) | PERp10/PERn10 | A60/A61 | CN3 | B24/B23 |
| Lane10 Rx (FPGA<-PCIe<-E1) | PETp10/PETn10 | B58/B59 | CN3 | A24/A23 |
| Lane11 Tx (FPGA->PCIe->E1) | PERp11/PERn11 | A64/A65 | CN3 | B27/B26 |
| Lane11 Rx (FPGA<-PCIe<-E1) | PETp11/PETn11 | B62/B63 | CN3 | A27/A26 |
| Lane12 Tx (FPGA->PCIe->E1) | PERp12/PERn12 | A68/A69 | CN4 | B18/B17 |
| Lane12 Rx (FPGA<-PCIe<-E1) | PETp12/PETn12 | B66/B67 | CN4 | A18/A17 |
| Lane13 Tx (FPGA->PCIe->E1) | PERp13/PERn13 | A72/A73 | CN4 | B21/B20 |
| Lane13 Rx (FPGA<-PCIe<-E1) | PETp13/PETn13 | B70/B71 | CN4 | A21/A20 |
| Lane14 Tx (FPGA->PCIe->E1) | PERp14/PERn14 | A76/A77 | CN4 | B24/B23 |
| Lane14 Rx (FPGA<-PCIe<-E1) | PETp14/PETn14 | B74/B75 | CN4 | A24/A23 |
| Lane15 Tx (FPGA->PCIe->E1) | PERp15/PERn15 | A80/A81 | CN4 | B27/B26 |
| Lane15 Rx (FPGA<-PCIe<-E1) | PETp15/PETn15 | B78/B79 | CN4 | A27/A26 |

**Table-1: Connection between each PCIe lane and four E1 SSDs**

## Disclaimer

No product warranty or support is provided if this adapter is used in environments without the DG NVMe-IP core. Design Gateway is not liable for any damage to FPGA evaluation boards or SSD devices resulting from improper use. This board is for evaluation purposes only and may not operate correctly depending on the characteristics of the connected devices.

[Contact]
URL : https://design-gateway.com
Email : ip-sales@design-gateway.com

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0E | Jul-14th-2026 | English manual first release |