AHCI PCIe SSD-IP (APS-IP) Demo Instruction

Rev1.1 13-Jul-16

This document describes the instruction to run APS-IP demo on ArriaV GX Starter board/ArriaV SoC Development board/Arria10 SoC Development board. For the ArriaV GX Starter board, AB16-PCIeXOVR board is required to connect with the AHCI PCIe SSD. The demo is designed to write/verify data with AHCI PCIe SSD. User can control test operation through NiosII command shell.

1 Environment Requirement

To demo APS-IP on Altera board, please prepare the following hardware/software.

1) Altera ArriaV GX Starter board/ArriaV SoC Development board/Arria10 SoC Development board
2) PC with QuartusII programmer and NiosII command shell software
3) For ArriaV SoC Development board only, AB16-PCIeXOVR board + PCIeSub board from AB16 delivery set
4) Altera Power adapter
5) AHCI PCIe SSD (Gen2 for ArriaV board, Gen3 for Arria10 board)
6) A cable for programming FPGA and NiosII command shell connecting between FPGA board and PC
   - USB Type-B cable in case of ArriaV GX Starter board
   - USB Mini-B cable in case of ArriaV SoC Development board
   - USB Micro cable in case of Arria10 SoC Development board

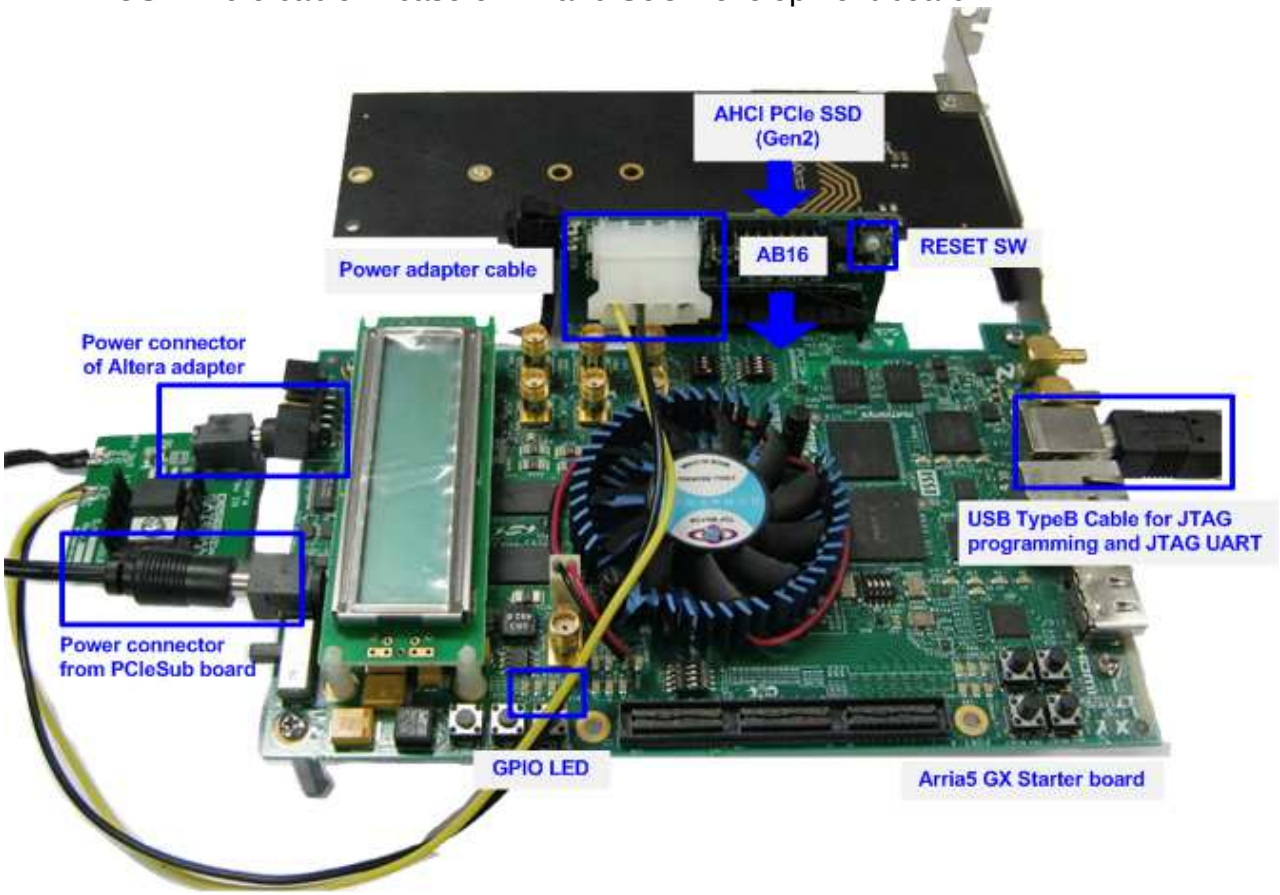

Figure 1-1 APS-IP Demo Environment Setup on ArriaV GX Starter Board

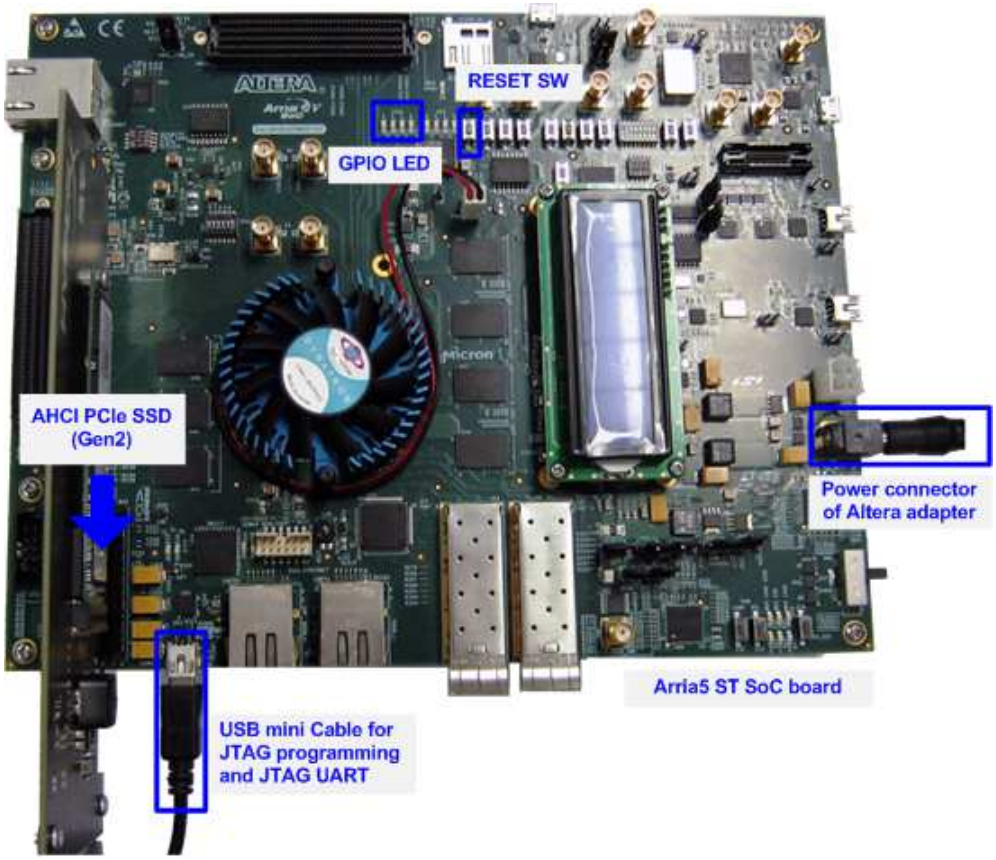

Figure 1-2 APS-IP Demo Environment Setup on ArriaV SoC Development Board

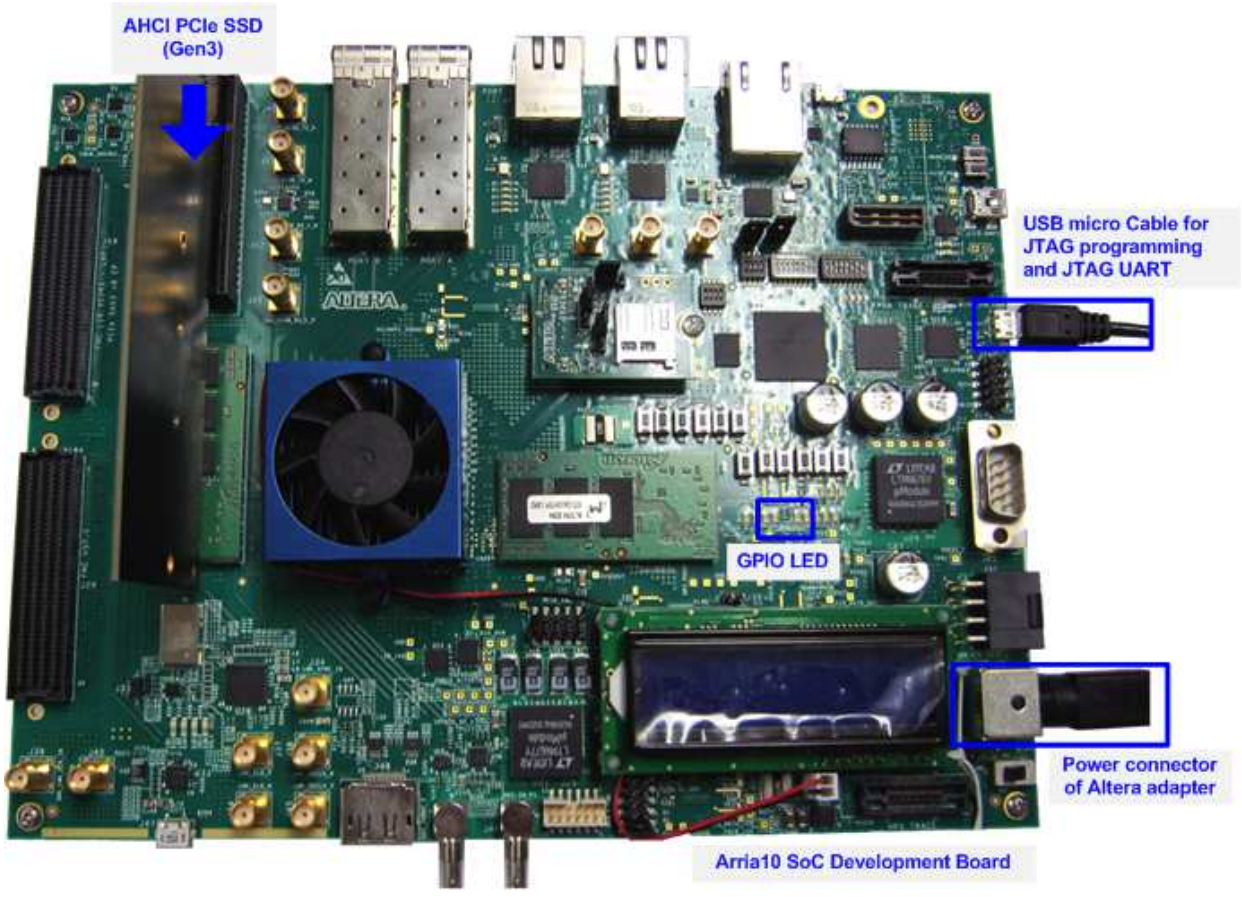

Figure 1-3 APS-IP Demo Environment Setup on Arria10 SoC Development Board

2 Demo setup

2.1 PCIe setup

a) ArriaV GX Starter board by AB16-PCIeXOVR

- Power off system.
- Connect power connector on PCIeSub board to power connector on FPGA board.
- Connect ATX power connector on PCIeSub board to AB16-PCIeXOVR board.
- Connect Altera power adapter to connector on PCIeSub board.

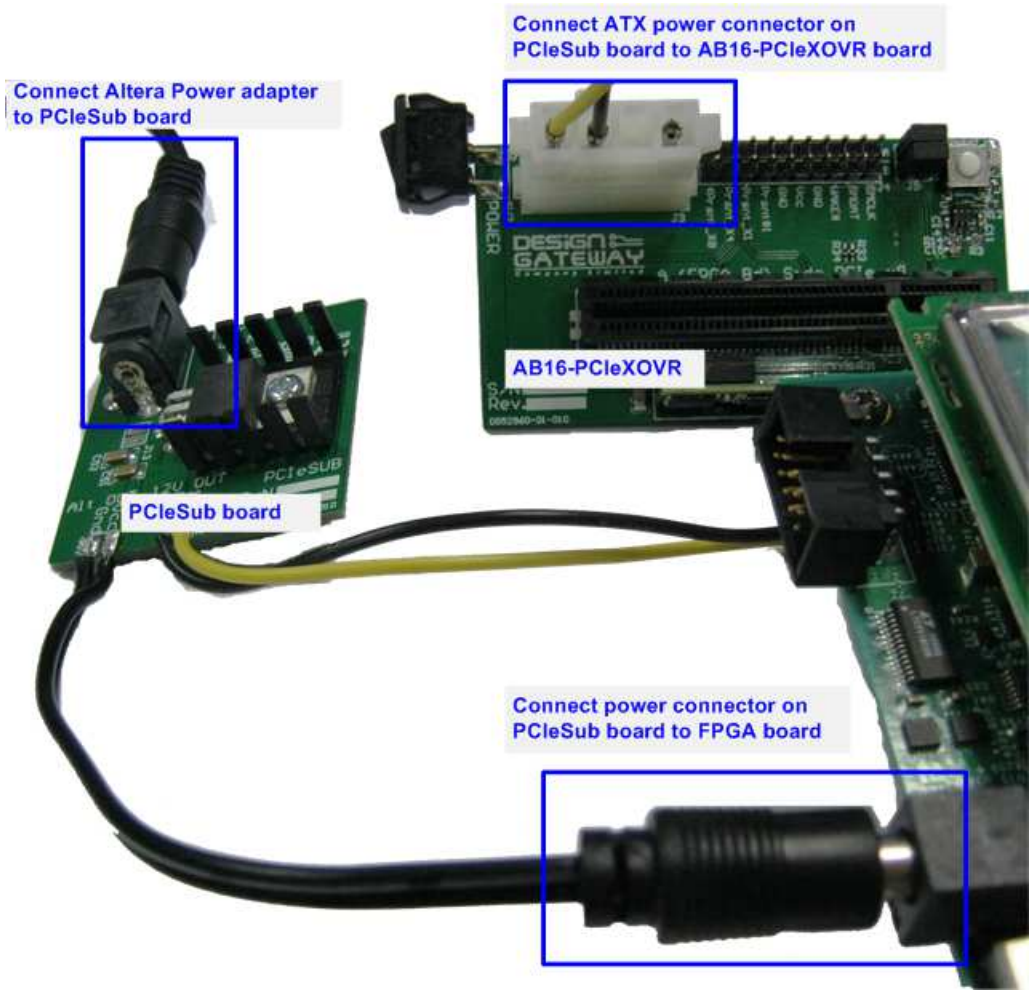

Figure 2-1 Connect PCIeSub board to FPGA board, AB16, and Altera adapter

- Connect A Side of PCIe connector on AB16-PCIeXOVR board to PCIe connector on FPGA board, as shown in Figure 2-2.
- Check that two mini jumpers are inserted at J5 connector on AB16.

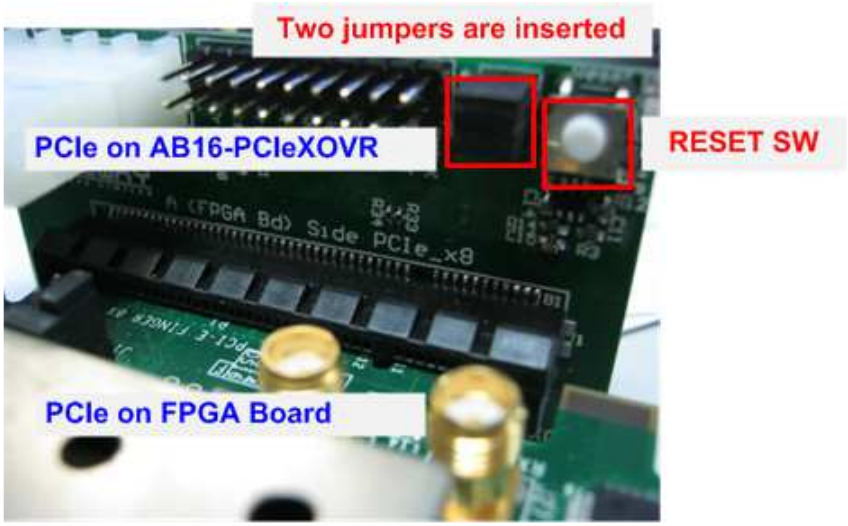

Figure 2-2 Connect PCIe connector between AB16 and FPGA board

- Connect AHCI PCIe SSD to B Side of PCIe connector on AB16-PCIeXOVR board.

Figure 2-3 Connect AHCI PCIe SSD to AB16 board

- Connect USB Type-B cable from FPGA board to PC for JTAG programming and NiosII command shell.

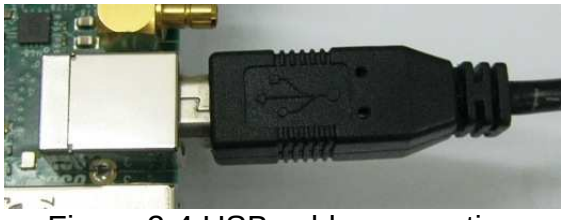

Figure 2-4 USB cable connection

- Power on FPGA development board and power on AB16-PCIeXOVR board.

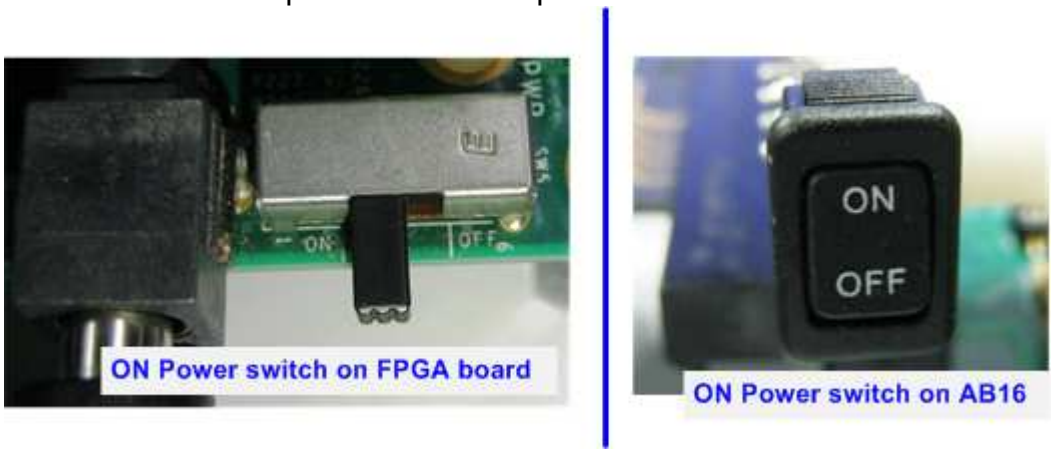

Figure 2-5 Power on FPGA and AB16 board on ArriaV GX Starter board.

b) ArriaV/Arria10 SoC Development board by PCIe root complex connector

- Power off system.
- Connect Altera power adapter to FPGA board.
- Connect AHCI PCIe SSD to PCIe connector on FPGA board.
  Note: ArriaV board can support PCIe Gen2 device while Arria10 board can support PCIe Gen3 device.
- Connect USB mini/micro cable from FPGA board to PC for JTAG programming and NiosII command shell.

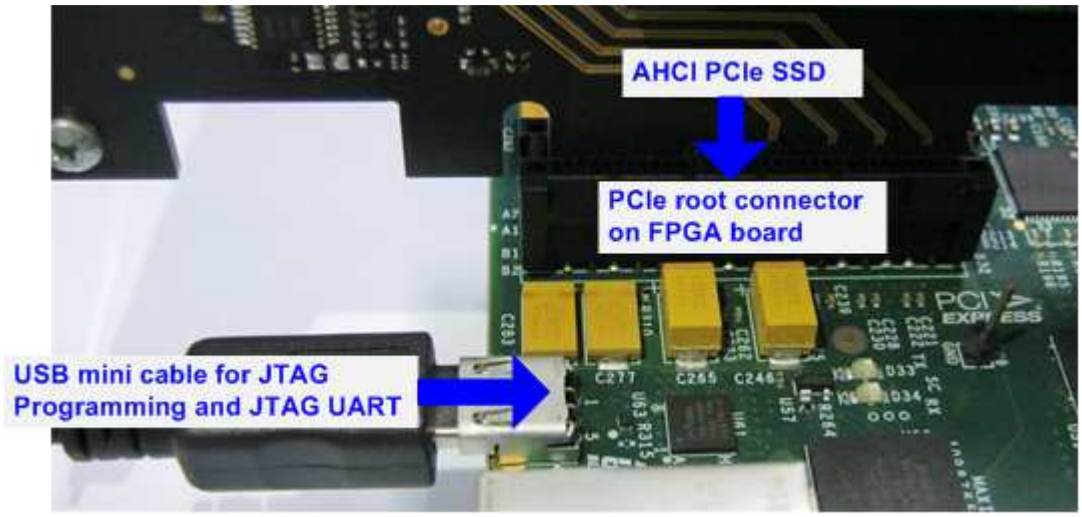

Figure 2-6 AHCI PCIe SSD connection on ArriaV SoC board

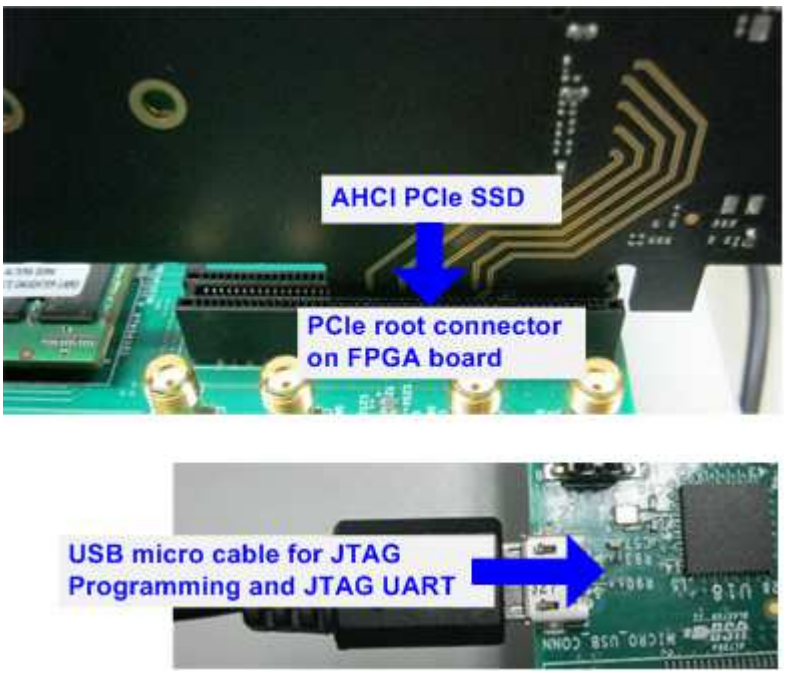

Figure 2-7 AHCI PCIe SSD connection on Arria10 SoC board

- Power on FPGA development board

Figure 2-8 Power on ArriaV SoC board

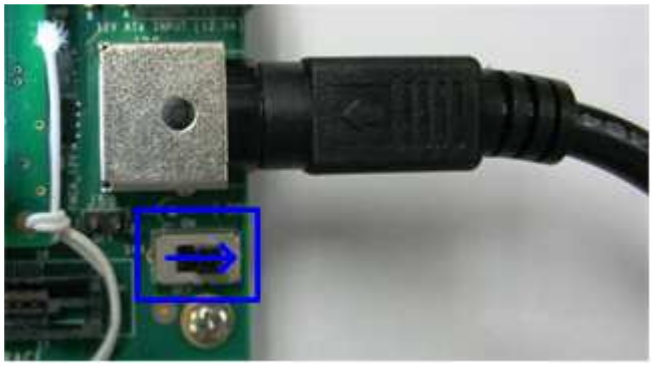

Figure 2-9 Power on Arria10 SoC board

2.2 Board setup

- Use QuartusII Programmer to program “APSIPTest.sof” file, as shown in Figure 2-10.

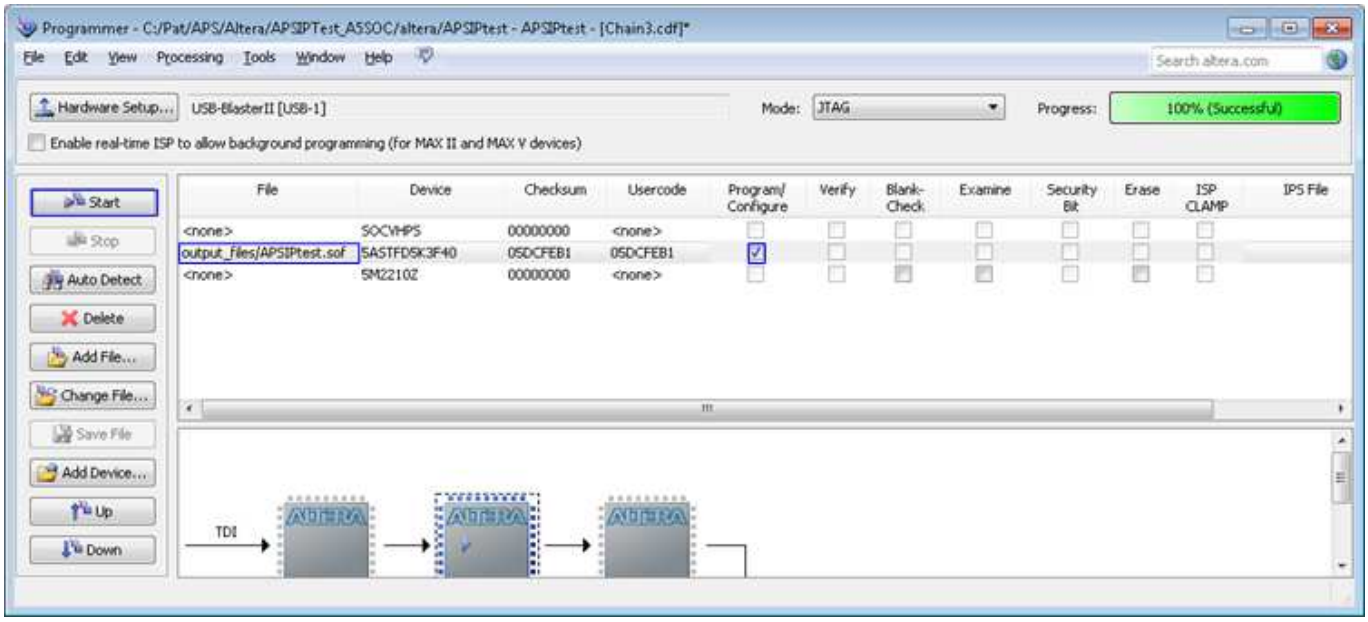

Figure 2-10 Programmed by QuartusII Programmer

- Open NiosII Command Shell and run nios2-terminal command. Boot message will be displayed.
  “Waiting device ready” message is displayed during system initialization.
  “PCIe Gen3/2/1 Device Detect” shows PCIe speed after PCIe linkup.
  Main menu will be displayed to receive command from user.

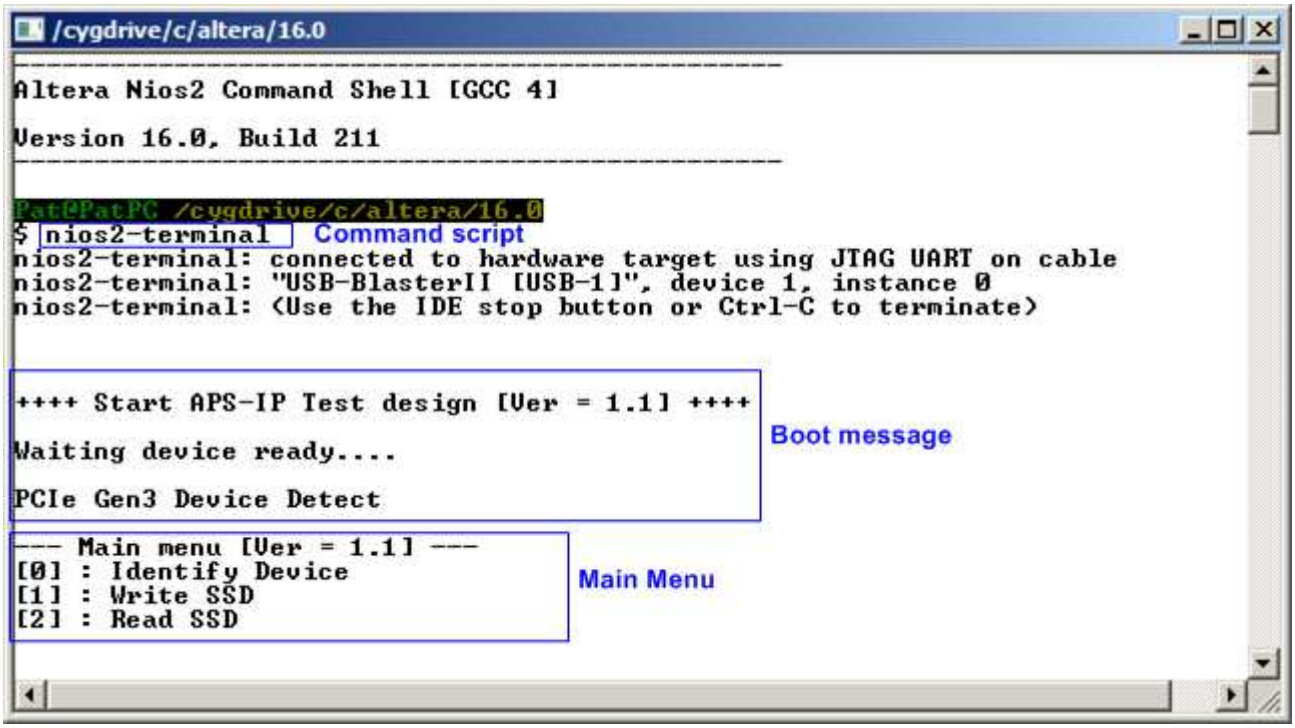

Figure 2-11 NiosII Terminal

- Check LED status on FPGA board. The description of LED is follows.

Table 2-1 LED Definition

GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1	System is busy	Idle status
2	PCIe Error detect	Normal operation
3	Data verification fail	Normal operation

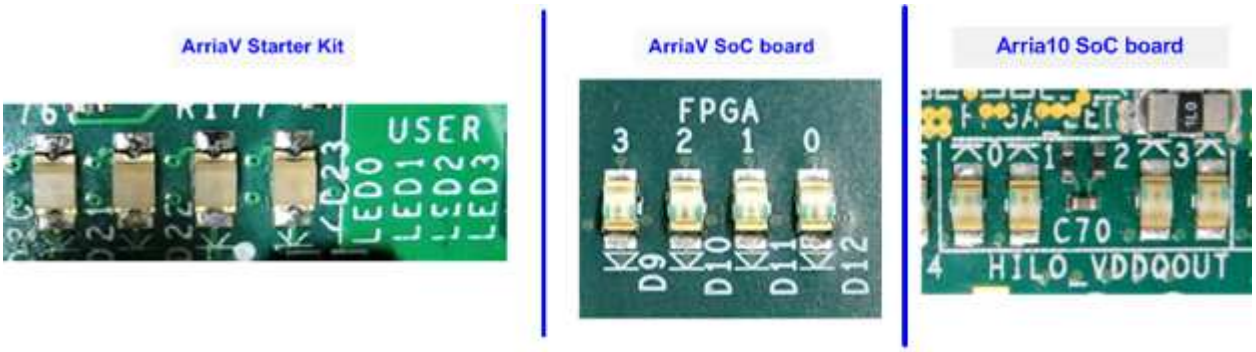

Figure 2-12 4-bit LED Status for user output

- After programming completely, LED[0] and LED[1] will be ON during PCIe initialization process. Then, LED[1] will be OFF to show that PCIe completes initialization process and now system is ready to receive command from user.

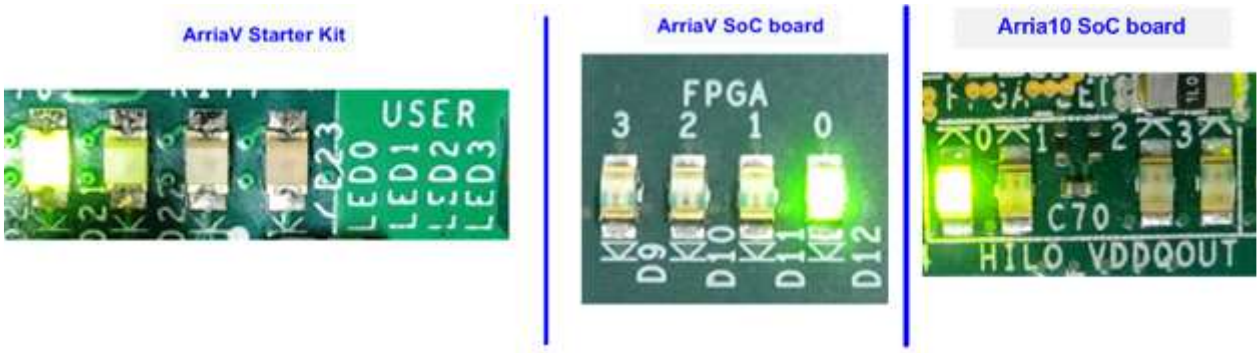

Figure 2-13 LED status after program configuration file and PCIe initialization complete

3 Test Menu

3.1 Identify Device

Select ‘0’ to send Identify device command to AHCI PCIe SSD. When operation is completed, SSD capacity will be displayed on the console.

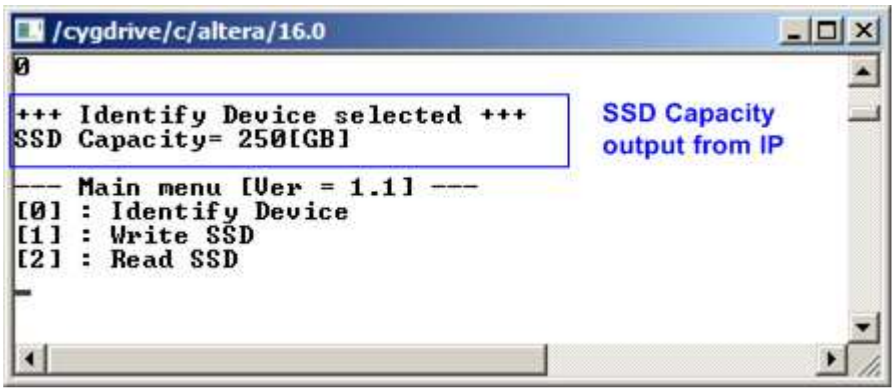

Figure 3-1 Result from Identify Device menu

3.2 Write SSD

Select ‘1’ to send Write command to AHCI PCIe SSD. Three inputs are required for this menu.
- Start LBA: Input start address of SSD in sector unit
- Sector Count: Input total transfer size in sector unit
- Test pattern: Select test pattern of test data for writing to SSD. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

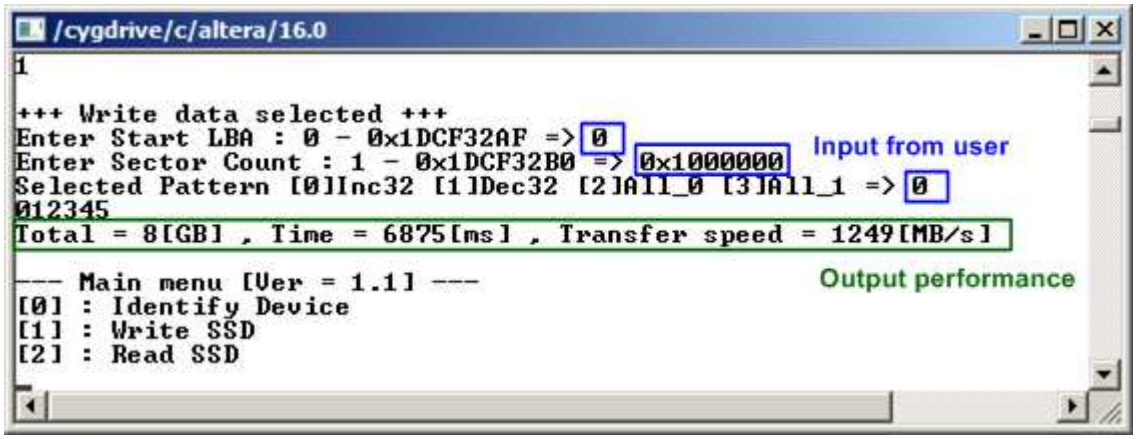

Figure 3-2 Input and result of Write SSD menu

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, number 0-9 will be printed out to the console to show that system still be alive. Finally, test performance with the size and time usage will be displayed on the console.

Figure 3-3 - Figure 3-5 shows error message when user input is invalid. “Invalid input” message will be displayed on the console, and then return to main menu to receive new command.

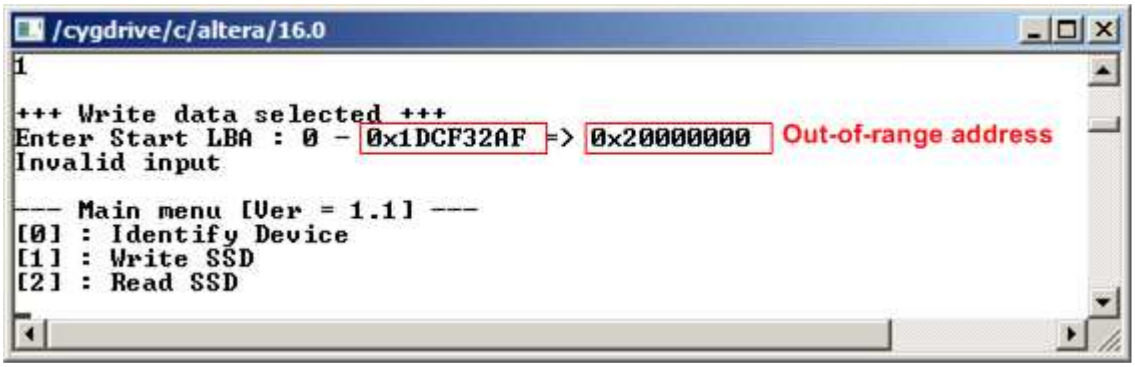

Figure 3-3 Invalid Start LBA input

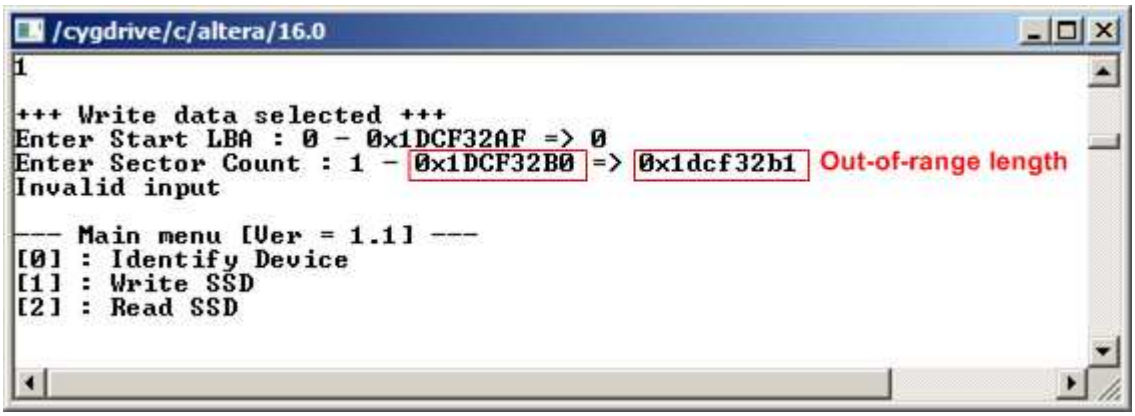

Figure 3-4 Invalid Sector count input

Figure 3-5 Invalid Test pattern input

3.3 Read SSD

Select '2' to send Read command to AHCI PCIe SSD. Three inputs are required for this menu.
- Start LBA: Input start address of SSD in sector unit.
- Sector Count: Input total transfer size in sector unit
- Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with write test. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

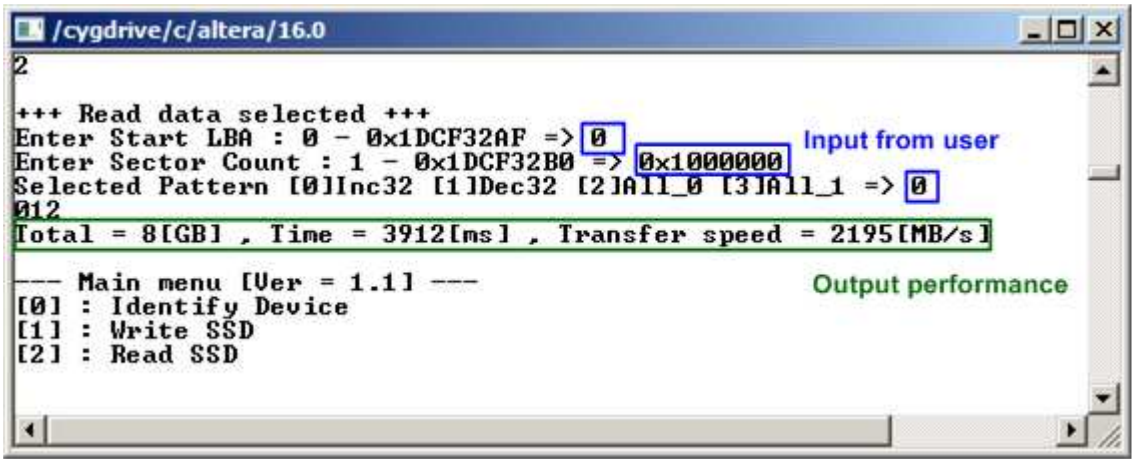

Figure 3-6 Input and result of Read SSD menu

Similar to write test if all inputs are valid, the operation will be started and test performance will be displayed when end of transfer. "Invalid input" will be displayed if any input value is out-of-range.

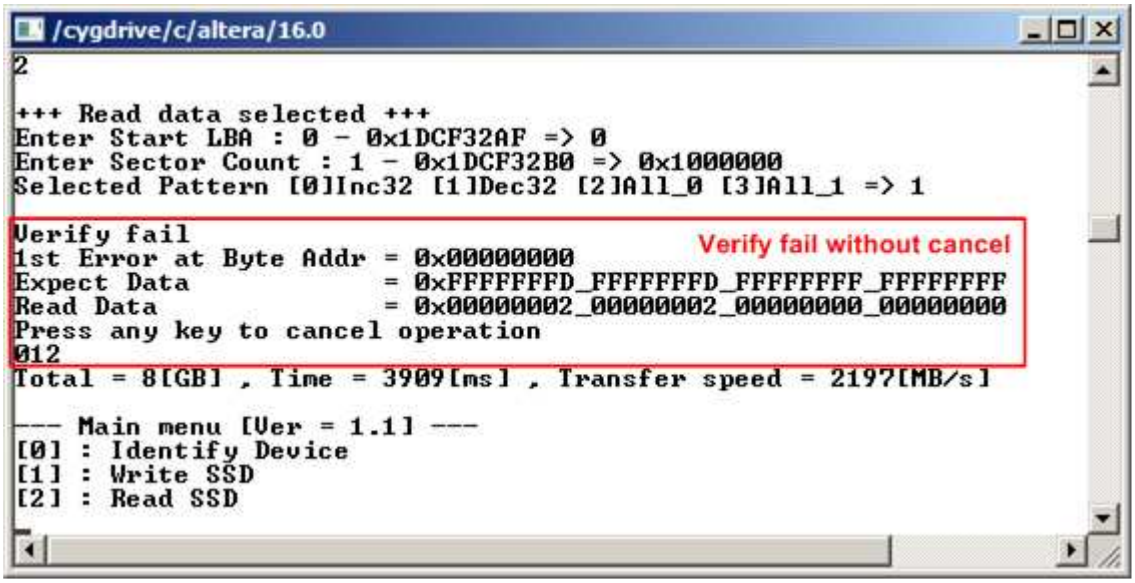

Figure 3-7 Data verification is failed, but wait until read complete

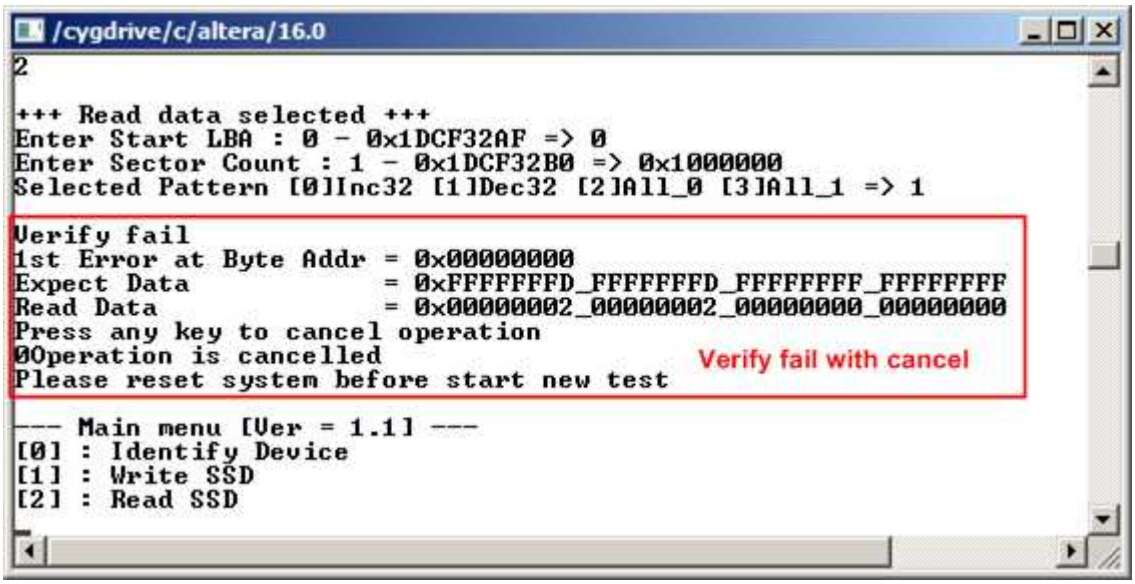

Figure 3-8 Data verification is failed, and press key to cancel operation

Figure 3-7 and Figure 3-8 show the error message when data verification is failed. “Verify fail” message will be displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete. “RESET” button should be pressed to restart the system before starting new test.

4 Revision History

Revision	Date	Description
1.0	3-Feb-16	Initial version release
1.1	13-Jul-16	Support Gen3 speed