Design Gateway

Product Portfolio

for the Vertical Market

altera solution acceleration partner

Design Gateway is the Altera Solution Acceleration Partner

Storage IPs
Networking IPs
Security IPs

All pure hardware logic
No CPU & external memory required
Proven by Real board
High performance & High reliability
Compact resource & Simple user interface

- **Support the Latest Devices**
  The Altera Agilex™ high-performance FPGA is available.
- **Ready to Evaluate on Real FPGA Boards**
  Evaluate IP core performance before purchase and watch the demo on YouTube.
- **Reference Design provided together with IP core License**
  Enables step-by-step development for faster and more reliable results.
- **Rich Technical Documents**
  All technical information is publicly available on the official website.

DESIGN GATEWAY

COMPANY LIMITED

NVMe IP core Series

Direct Connection to PCIe Gen5/Gen4 SSD for Agilex™ 7 and Agilex™ 5 FPGA

The NVMe-IP Core series is an IP core that interfaces with PCIe SSDs without requiring a CPU or external memory. It is ideal for storage applications demanding ultra-high-speed performance at gigabytes per second. By enabling GB/s-level data transfers with a single SSD—previously achievable only through multiple SSDs in a RAID setup—this core contributes to system compactness and efficiency.

A reference design for Altera FPGAs is included as a standard feature, helping to accelerate product development. Additionally, free demo files for Altera FPGA evaluation boards are available, allowing users to test and evaluate the core on real hardware before purchase.

Features

- Implement application layer to access NVMe PCIe SSD without CPU and external memory (DDR)
- Support IDENTIFY, Write, Read, SMART, Shutdown, FLUSH, Secure Erase Command
  * Optional Support: Format, Write Zero, Sanitize command
- CPU-Free exFAT/FAT32 Access * optional
- Support PCIe switch * customize support
- Free evaluation before purchasing



CPU & External Memory Not Required



Simple Interface



Proven Reference Design



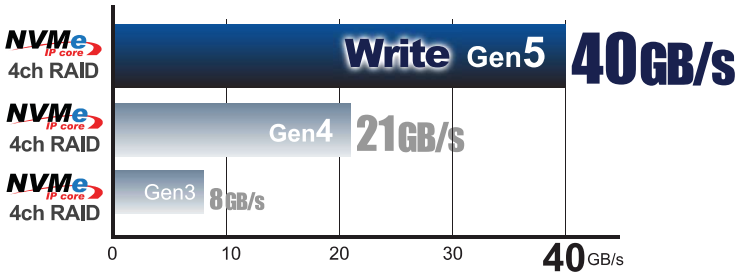
Rich Documents

Line up & Options

IP core	NVMe IP core	NVMe G3 IP core	rmNVMe IP core	muNVMe IP core
Function	NVMe IP core (Standard)	NVMe IP core with PCIe Soft IP	rmNVMe IP Random Access by Multiple Users	muNVMe IP Multiple Users Simultaneously Access
PCIe IP	PCIe Hard IP Gen5/Gen4/Gen3	PCIe Soft IP Gen3	PCIe Hard IP Gen5/Gen4	PCIe Hard IP Gen4/Gen3
User Access	Single User	Single User	Multiple Users	Multiple Users
Access Pattern	Sequential	Sequential	Random	Sequential
Simultaneous Write/Read	-	-	Support	Support
Max. Speed	Write 11,200MB/sec with PCIe Gen5	Write 3,400MB/sec	Single-user 2,484K IOPS with PCIe Gen5	Total 7,306MB/sec (Wr 2,117MB/sec x2 Rd 1,536MB/sec x2)
Target Application	High-speed Data Acquisition System	High-speed Data Acquisition System	Data Center (Search engines, shared storage)	Data Logging with Real-time Monitoring
Optional IP & Reference Design	exFAT IP FAT32 IP 2ch/4ch RAID0 PCIe Switch DDR Sustain Rate FTP Server 100GbE Data Logger	exFAT IP FAT32 IP 2ch RAID0 * Contact us.	* raNVMe IP, Single-user random-access is also available.	exFAT IP 2ch RAID0 FTP Server * Contact us.

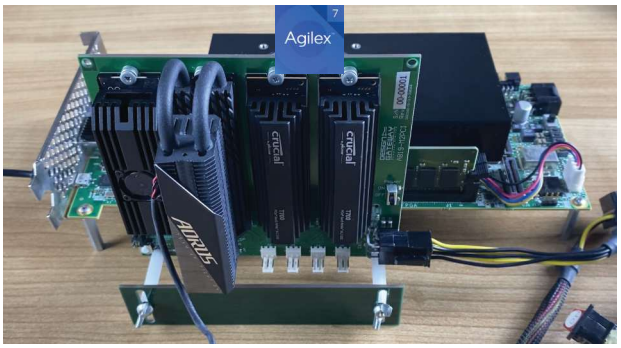
Blazing Fast & Sustained Performance

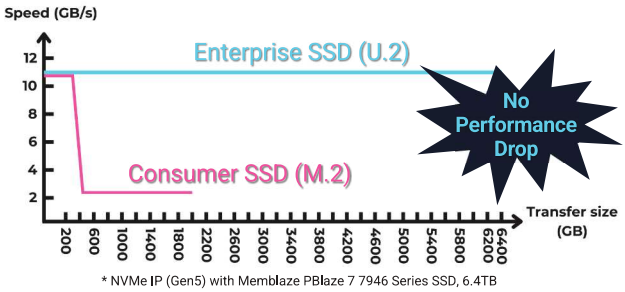
The performance result of NVMe-IP PCIe **Gen5**
4ch RAID0 on Agilex™ I-Series



* Gen5 NVMe SSDs: Gigabyte AORUS 10000, CFD Gaming, Crucial T700 x2 drives
* Gen4 NVMe SSDs: WD Black SN850 x4 drives.
* Gen3 NVMe SSDs: Samsung 960 Pro ×2 drives, 970 Pro ×2 drives).

Free Evaluation Demo of NVMe-IP PCIe **Gen5**
4ch RAID0 on Agilex™ I-Series





* NVMe IP (Gen5) with Memblaze PBlaze 7 7946 Series SSD, 6.4TB

Enables Sustained Recording
of **6.4TB** Full Disk at **11,000MB/sec**



Free Evaluation Demo of NVMe-IP PCIe **Gen5**
with E1 Enterprise SSD on Agilex™ I-Series

Suitable Applications

MANUFACTURING & EQUIPMENT



Data Logger

TEST & MEASUREMENT



4K/8K Display tester
Image Measuring Device

AUTOMOTIVE



LiDAR

MEDICAL



High resolution CT scanner

AEROSPACE



Satellite tracking station

BROADCASTING & MEDIA



4K/8K Video
Recording System

100G Ethernet File-Based Data Logger System

Reference design available



YouTube Demo Video



NVMe-IP PCIe Gen5 4ch RAID0
performance demo on Agilex 7 I-Series



rmNVMe-IP PCIe Gen5
performance demo on Agilex 7 I-Series



High-Speed File-Based 100G Ethernet
Data Logging with NVMe Gen5 IP and exFAT2-IP

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/nvme-ip.html

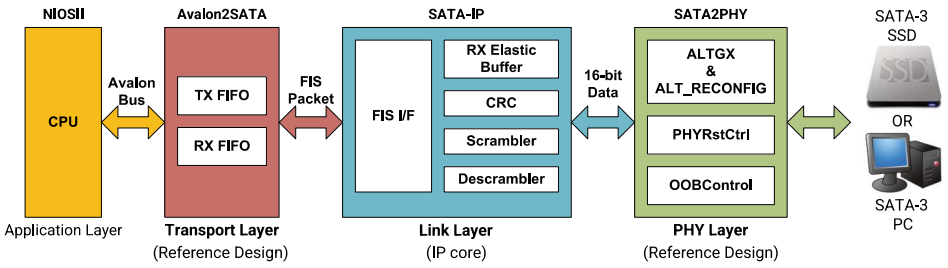
SATA IP
Serial ATA Transport&Link Layer IP Core

Proven High-Performance & Reliable SATA-IP, Trusted by NASA



4ch RAID0 evaluation on Arria 10 SX Development Kit

The SATA IP core is a link layer IP core designed to implement a SATA channel on Altera FPGAs. It compliant with the Serial ATA specification revision 3.0 (6Gbps) and maximizes the performance of SATA-III SSDs. By utilizing the FPGA's built-in transceivers as SATA ports, no external PHY chip is required. Additionally, a reference design with source code, verified on Altera FPGA evaluation kits, is included as a standard feature, enabling rapid product development.

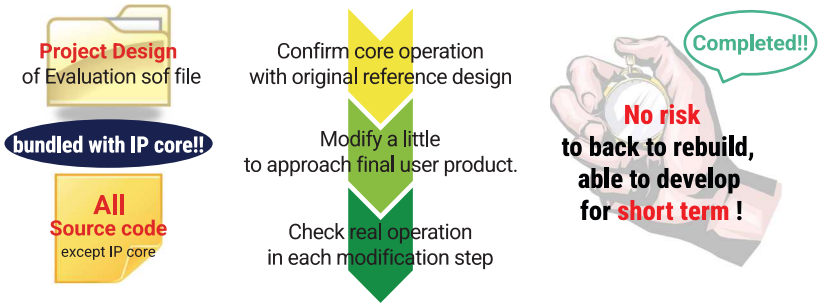


Features

- CPU & External Memory Not Required
- Simple Interface
- Proven Reference Design
- Rich Documents

- Compliant with SATA 3.0 6Gbps
- Support both Host and Device
- exFAT/FAT32 access without CPU
  * with optional HCTL-IP
- Free evaluation before purchasing
- The Reference Design is provided with the IP core license

Enhanced development support



Suitable Applications



Flight data loggers require the highest levels of data integrity and stable performance for real-time sensor data logging. Our SATA Host IP Core simplifies system design by enabling data logging directly from sensors to SATA SSDs without CPU and OS intervention. This offers more efficient system implementation while meeting stringent performance requirements.



Satellites have limited space and power resources. Implementing a SATA storage solution enables reliable and stable data collection with a compact design and low power consumption.

Performance

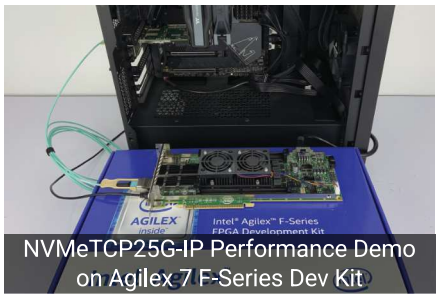


The live performance evaluation of the SATA IP core series is available to watch on YouTube.

SATA HCTL-IP **4-Channel RAID0** Performance Demo on Arria 10 SX Dev Kit
Achieves over **2 GB/s** Read and Write.

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/sata-ip.html

CPU-Free End-to-End NVMe Over Fabric TCP Connectivity



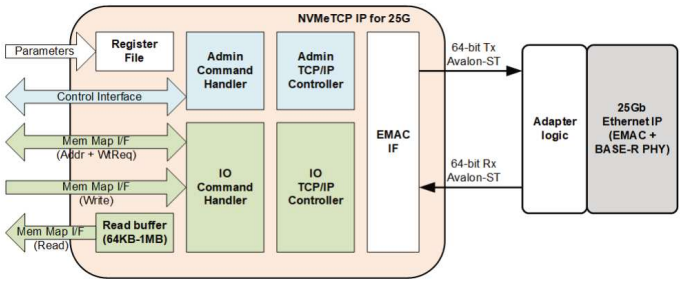
NVMeTCP25G-IP Performance Demo on Agilex 7 F-Series Dev Kit

The NVMeTCP IP core series is a standalone host-side NVMe over Fabric (NVMe/TCP) controller that operates without a CPU or external memory. It enables high-performance remote access to NVMe-oF storage servers using simple user logic, significantly reducing design complexity and development time.

With direct, high-speed connectivity over the FPGA's network interface, your FPGA card or board can seamlessly integrate with existing NVMe-oF storage infrastructure. The IP core license includes a reference design for Altera FPGA boards, further accelerating development and lowering costs.

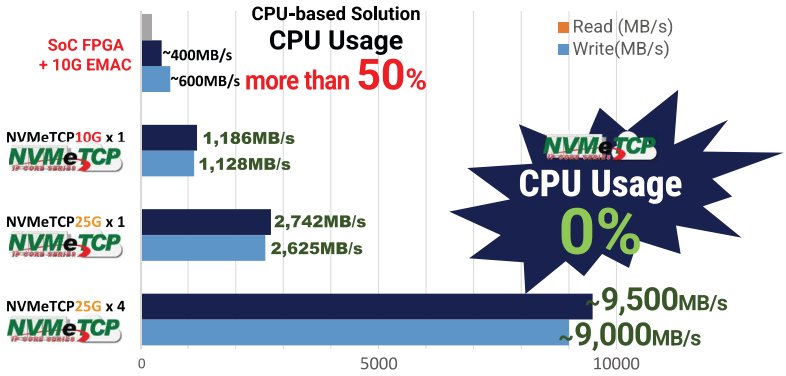
Merits & Advantages

- Simply attach the remote NVMe-of storage server to FPGA Card/Board without PCIe hard IP and/or SoC
- Very high performance with over 95% network band-width utilization
- Enabling NVMe/TCP host side on FPGA with no CPU and DDR
- Scalable storage capacity & performance with multiple IPs implementation



Block diagram * NVMeTCP25G-IP

Performance



By utilizing multiple NVMe TCP IP cores, each data stream can be transferred simultaneously to individual SSDs.

This IP enables the development of applications that maximize the high-speed capabilities of 10Gbit and 25Gbit Ethernet while harnessing the exceptional performance of NVMe SSDs.

Suitable Applications



In modern vehicles, FPGAs process data from sensors, cameras, and radar systems. Our NVMeTCP IP Core enables real-time data processing and seamless transmission over 10G or 25G Ethernet to a remote NVMeTCP storage server.

This approach optimizes space and power efficiency while ensuring reliable and efficient storage of massive data volumes.



At satellite ground stations, FPGAs handle the downlink of satellite data. With the NVMeTCP IP Core, this critical data can be rapidly transmitted over 10G or 25G Ethernet to remote storage servers.

This approach ensures secure, efficient storage of large satellite data volumes while maintaining high performance and scalability.

YouTube Demo Video



FPGA-Accelerated Cloud Storage with NVMe/TCP on Silicom N6010

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/nvme-tcp-ip.html

CPU-less TCP/IP Offloading Engine with Multi-Stream Support, up to 200GbE

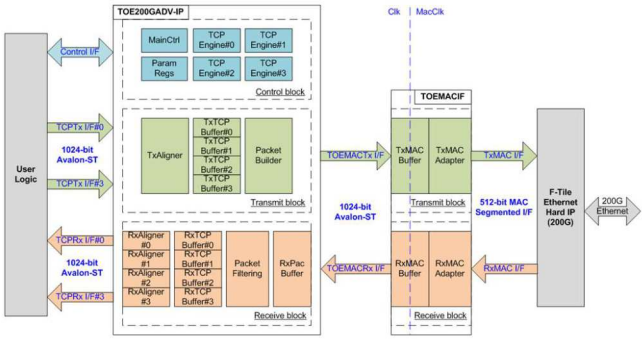
The TCP Offloading Engine IP Core series (TOE200G/100G/40G/25G/10G/1G-IP) is an innovative, CPU-less solution for high-speed TCP processing. Traditionally, TCP protocol handling requires complex processing and high-performance CPUs. However, the TOE-IP core series achieves full TCP offloading through pure hardwired logic, eliminating the need for an external CPU.

This IP core includes a complete reference design for Altera FPGAs, significantly reducing your development time. Design Gateway also provides free demo bitstreams for Altera FPGA kits, allowing you to evaluate the TOE-IP core on real board before making a purchase.



TOE200G*ADV*-IP Evaluation on Altera Agilex 7 I-Series

Block diagram * TOE200GADV-IP



Features

- **Pure hardwire logic**: No CPU or external memory required
- **Configurable TCP Buffer**: Up to 1MB * TOE100GADV-IP/TOE200GADV-IP
- **Up to 4 TCP Sessions**: For optimal TCP transmission speed with network infrastructure * TOE100GADV-IP/TOE200GADV-IP
- **High performance processor interface**: 1024bit Avalon-ST interface with byte alignment * TOE200GADV-IP

Effective transfer speed over **24** GB/sec

Application Examples



High bandwidth 8K Video Multi-Streaming

8K@60fps raw video streaming requires 6GB/s bandwidth per 1 video stream. TOE200GADV-IP can accommodate four 8K video stream transmission over 200G simultaneously. Ensures smooth and stable video transmission on cutting edge video display systems, like the MSG Sphere.


Satellite Tracking System


CT Scan


Pipeline inspection System


Semiconductor Manufacturing


Radar System


Ophthalmic Medical


Scanning sonar Fish detection system


Industrial Printer

Performance

The live performance evaluation of the TOE IP core series is available to watch on YouTube.


TOE200G*ADV*-IP Performance Demo on Agilex 7 I-Series Dev Kit


TOE10G-IP Performance Demo on Agilex 9 Direct RF Series Dev Kit

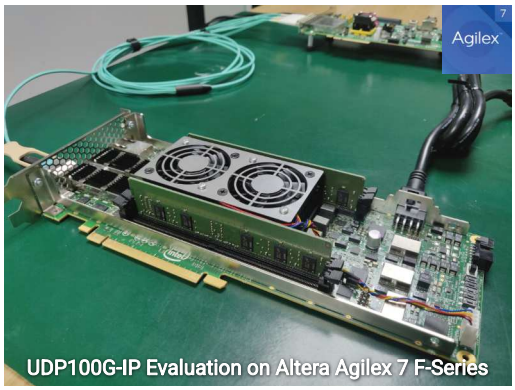
Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/toe-ip.html

UDP xxG IPcore series
User Datagram Protocol IP Core

UDP Offload Engine without CPU for Real-Time Applications

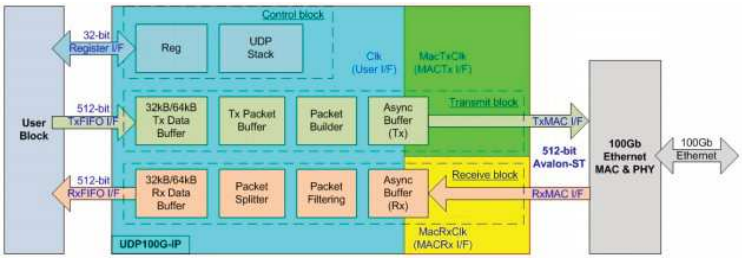
The UDP IP Core series (UDP100G/40G/25G/10G/1G-IP) is ideal for broadcast and low-latency network applications. UDP-IP cores are fully implemented in hardware, delivering minimal overhead and low latency. They are well-suited for aerospace applications such as radar systems, where both rapid response and high-speed broadcast data transfer are essential.

This IP core includes a complete reference design for Altera FPGAs, significantly reducing your development time. Free demo bitstreams are available for Altera FPGA boards, enabling evaluation of the UDP-IP core on real hardware before purchase.



UDP100G-IP Evaluation on Altera Agilex 7 F-Series

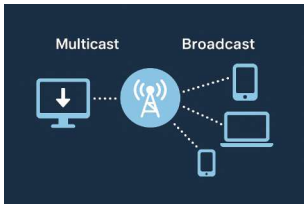
Block diagram * UDP100G-IP



Features

- **Pure hardwire logic**: No CPU or external memory required
- Support **Full Duplex**
- **Free** evaluation before purchasing
- Speed up development and minimize costs with our ready-to-use **Reference Design**

Supports Multicast & Broadcast Transmission



The UDP-IP core series, with customization, enables simultaneous data transmission to multiple targets. It is ideal for applications requiring real-time performance, such as aerospace radar systems.

Application Examples


Radar System


Delay Tolerant Network (DTN) Investigation


Electronics Control Unit (ECU)


Wireless Communication System


Network game Console

Introduction & Performance Videos

The live performance evaluation of the UDP IP core series is available to watch on YouTube.



UDP100G-IP Performance Demo on Altera Agilex 7 F-Series



UDP10G-IP Performance Demo on Altera Agilex 9 Direct RF Series

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/udp-ip.html

10Gbps CPU-less QUIC Offload IP with TLS 1.3 Security

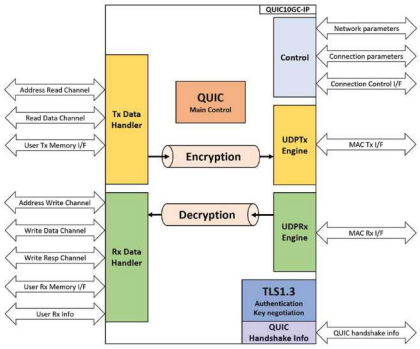
The QUIC IP core series is engineered from the ground up to implement the QUIC protocol with TLS 1.3 security entirely in hardware logic for FPGA-based applications. These IP cores completely offload the CPU by handling TLS 1.3 handshakes, payload encryption/decryption, and managing both QUIC and UDP/IP layers within a single IP core.

This IP core includes a complete reference design for Altera FPGAs, significantly reducing your development time. Free demo bitstreams are available for Altera FPGA boards, enabling evaluation of the QUIC-IP core on real hardware before purchase.

Features

- Pure hardwire logic, No CPU or External Memory required
- 10Gbps QUIC engine conforming to RFC9000
  * 1Gbps version is also available.
- Supports TLS1.3 cipher suite TLS_AES_128_GCM_SHA256
  - Key exchange: X25519
  - Derive key: HKDF with SHA256
  - Encryption/Decryption: AES128-GCM
- Signature algorithm
  - rsa_pss_rsae_sha256 with 2048-bit RSA public key
  - ecdsa_secp256r1_sha256
- Supports multiple streams compliant with the QUIC standard.

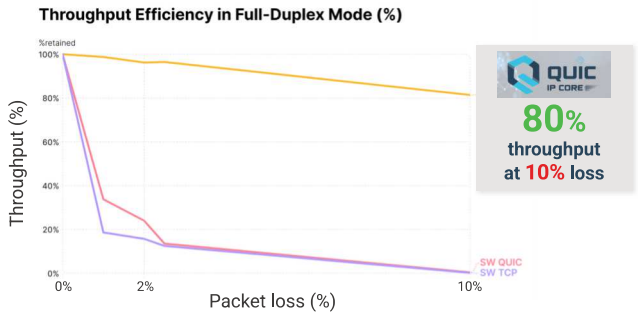
Block diagram

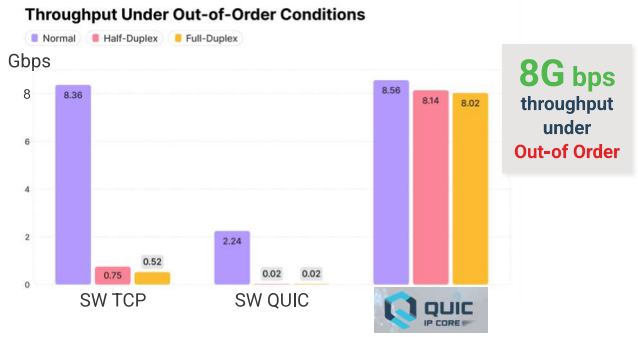


Performance

* QUIC 10Gbps IP

CPU-less QUIC-IP maintains an overwhelming throughput **up to 400 times** greater than conventional TCP/IP protocols and common software-based QUIC (such as MsQuic) in high-speed, lossy network environments and in congested networks prone to out-of-order packets.





Both software-based TCP and QUIC suffer severe performance degradation with as little as 1-2% packet loss, while QUIC-IP **sustains 80% throughput even under 10% packet loss**.

Under out-of-order conditions where packets arrive out of sequence, software-based QUIC suffers significant performance degradation due to high CPU load. In contrast, QUIC-IP consistently delivers **over 8 Gbps** regardless of network conditions.

Introduction & Performance Videos

The live performance evaluation of the QUIC IP core series is available to watch on YouTube.



QUIC10GC IP core Demo on Agilex 7 I-Series



QUIC10GC IP core Demo on Agilex 5 E-Series



QUIC1GC IP core Demo on Agilex 5 E-Series

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/altera/quic-ip.html

WireGuard IP core Full-Speed VPN Encryption in Pure HW Logic

The **WireGuard IP** core implements the complete WireGuard VPN protocol entirely in hardware, delivering full line-rate encryption and decryption with no CPU load and no external memory required.

It eliminates CPU overhead by performing the full Noise handshake, ChaCha20-Poly1305 encryption, X25519 key exchange, and BLAKE2s key derivation entirely in programmable logic. Proven with real WireGuard software interoperability testing on FPGA evaluation boards.

- Pure hardwire logic, No CPU or External Memory required
- Supports 1Gbps line-rate encryption and decryption
  * 10GbE version is also scheduled for release
- Internal Handshake Support
- IPv4 Protocol Support without IP fragmentation
- Integrated UDP/IP and ARP Protocol Controllers
- User Data Interface: 64-bit AXI4-Stream
- Ethernet MAC Interface: 64-bit AXI4-Stream

10Gbps CPU-less TLS 1.3 Offload IP core for Mission-critical Applications

TLS1.3 IP (Transport Layer Security IP) is the CPU-less & High-performance TLS v1.3 protocol engine for FPGA Acceleration with no CPU and external memory required. Providing maximum Gigabit Ethernet throughput for highly secure data transmission over 1G/10G/25G/100G network. Protect your valuable data from potential security breaches by using TLS secure transmission now!

- Supports TLS1.3 cipher suite
  - TLS_AES_256_GCM_SHA384
  - Key exchange: X25519
  - Derive key: HKDF with SHA384
  - Encryption/decryption: AES256GCM
- Signature algorithm
  - rsa_pss_rsae_sha256 with 2048-bit RSA public key
  - ecdsa_secp256r1_sha256



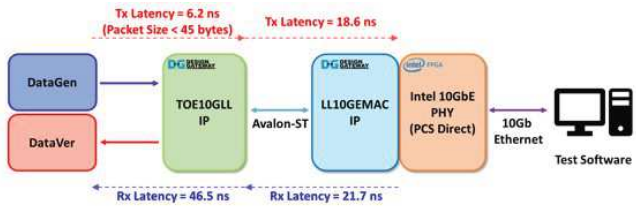
Aerospace Telemetry
Ensure the integrity and confidentiality of sensitive inflight data streams from remote sensors in aerospace applications. FPGA-accelerated TLS 1.3 outpaces software-only solutions, safeguarding critical flight information.



Medical Device Connectivity
Protect patient data in transit between medical devices and healthcare systems. Our solution provides the robust encryption and authentication mechanisms needed to comply with stringent healthcare regulations and safeguard patient privacy.

Nanosecond-Class Ultra-Low-Latency Networking IP cores

Ultra-Low Latency Networking IP core (LL Networking IP) is purpose-built to address the stringent requirements of mission-critical applications—spanning FinTech sectors such as High-Frequency Trading (HFT) and High-Speed Trading (HST), as well as aerospace and defense, telecommunications infrastructure, industrial control, automotive, and medical devices - that demand extremely low latency and high determinism.



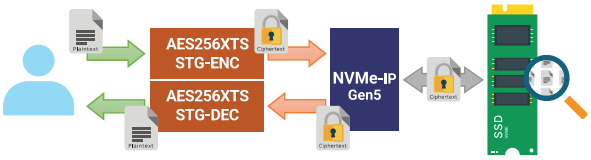
- **LL 10GEMAC-IP**
  - Tx 18.6ns
  - Rx 21.7ns
- **LL UDP10GRx-IP**
  - Rx 37.2ns
- **TOE10GLL-IP**
  - Tx 6.2ns
  - Rx 46.5ns

High throughput for Secure Storage Applications

STG PCIe Gen3 | STG-2X PCIe Gen4 | STG-4X PCIe Gen5

AES256-XTS-STG IP implement the advanced encryption standard (AES) with XEX (XOR Encrypt XOR) tweakable block cipher which operates sequences of complete blocks and is widely used in protecting the confidentiality of data on various storage devices with interfaces such as NVMe and SATA. We also have a lineup of "2X" ideal for NVMe PCIe Gen4, and "4X", supported **Gen5**.

- Support AES-XTS mode, 256-bit key size
- Support input data width128-bit
- Support Auto Increment Iv every 512-byte Mode
- Peak throughput rate at 512Mbits/MHz (AES256-XTS-STG-4X IP)
- High-throughput, up to **204.8 Gbps** @400MHz



Over 10GB/sec Secure write with NVMe-IP core

Performance Video



Enhancing NVMe Gen5 SSD Security with AES256-XTS-STG Encryption

High throughput for Secure Communication Applications

The AES256-GCM IP core implements the Advanced Encryption Standard (AES) with a 256-bit key in Galois/Counter Mode (GCM), which is widely used for Authenticated Encryption with Associated Data (AEAD) applications. This IP has been verified against the official NIST (National Institute of Standards and Technology) test vectors, as defined in SP 800-38D, ensuring standards compliance. It is well-suited for high-performance, low-latency, and secure communication applications.

- Support AES-GCM mode standard
- Support 256-bit key size, 96-bit iv size
- Support zero-length AAD or data input
- Validated against NIST official test vectors

	AES-256-GCM-100G IP	AES-256-GCM-10G25G IP
Peak throughput rate	512 Mbits/MHz	128 Mbits/MHz
Max. throughput	112.64 Gbps @220MHz	38.4 Gbps @300MHz

* 1Gbps version is also available.

Demo Video



Validating AES256GCM IP with NIST Test Vectors

High-Performance & Highly Secure AEAD Encryption Engine

The ChaCha20-Poly1305 IP core implements the ChaCha20 stream cipher together with the Poly1305 message authentication code (MAC), following the IETF standard for Authenticated Encryption with Associated Data (AEAD).

ChaCha20 provides high-speed encryption and decryption with strong resistance against timing attacks, while Poly1305 ensures message authentication and integrity. Together, they form a widely adopted AEAD construction. The core supports a 256-bit key size and a 96-bit IV size. It also supports zero-length Additional Authenticated Data (AAD) or plaintext input, making it flexible for a wide range of secure applications.

- Fully compliant with ChaCha20Poly1305 AEAD (RFC 8439)
- Supports 256-bit key size and 96-bit IV
- Supports zero-length AAD or data input
- Peak throughput rate of 128 Mbits/MHz

Demo Video



ChaCha20-Poly1305 IP Introduction & Demo

Hardware-Accelerated Digital Signature Verification for High-Security Systems

The ECDSA256V-IP core implements Elliptic Curve Digital Signature Algorithm (ECDSA) verification on the NIST P-256 curve, providing a high-performance, hardware-only solution for secure authentication in modern communication and IoT systems. It eliminates CPU load by performing full signature verification entirely in hardware, without requiring software or external memory.

- Pure hardware ECDSA signature verification compliant with FIPS 186-4
- Supports NIST P-256 curve with 256-bit message digest
- Over 60 verifications per second @140 MHz
- Supports other elliptic curves on request
- Proven via NIST Test Vectors & SSL Validation

High Throughput & Low latency Encryption

AES-256SS IP specializes in ultra-high throughput and ultra-low latency. IP computes 128-bit data blocks in every 1 clock cycle. Delivering 128Mbps throughput per 1MHz such as **51.2 Gbps @ 400MHz**.

* AES128 is also available

	AES-256SS IP	AES-256 IP	AES-128 IP
Key size	256 bits	256 bits	128 bits
Throughput	51.2 Gbps @400MHz	3.41 Gbps @400MHz	4.65 Gbps @400MHz
Latency 128 bit data block	15 clocks	15 clocks	11 clocks

High efficiency & High throughput Hash

The SHA2 IP core supports SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/224, and SHA-512/256 secure hash algorithms. The core is fully compliant with the FIPS PUB 180-4 (Federal Information Processing Standard) specification. Suitable for applications such as secure communication, password authentication, and blockchain data integrity.

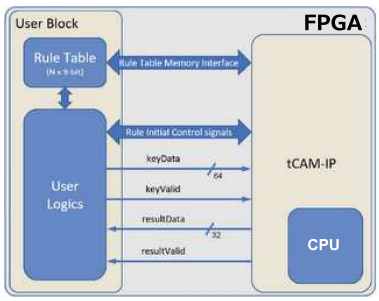
- Input Message Lengths (max.)
  SHA-224/256: 2^{61}-1 bytes (2^{64}-8 bits)
  SHA-384/512: 2^{125}-1 bytes (2^{128}-8 bits)
- Ultra High-Throughput
  SHA-224/256: **65 cycles** per 64-byte block
  SHA-384/512: 81 cycles per 128-byte block
- Hash Speed (max.)
  SHA-256: 1.969 Gbps @ 250 MHz
  SHA-512: 3.160 Gbps @ 250 MHz

Ultra-Fast TCAM Search Engine: 400 MSPS, 7 clock Cycle Latency

tCAM-IP is a high-performance, extremely low-latency, and highly configurable ternary content-addressable memory IP. tCAM-IP can make continuous deterministic search at **400 MSPS** with constant latency of **7 clock cycles**. It can achieve matching/filtering performance of 400,000,000 packets per second over Gigabit Ethernet.

Features

- Key width 64/56/48/40/32/24/16 bits
- Up to 1M rule entries
- Searching latency is constant at 7 clock
- 400 MSPS @ 400MHz searching speed, 1,000,000 Search/MHz
- Easy to customize rule table memory
- Simple rule table memory setup and user interface signals



Application Examples





Performance



tCAM-IP performance demo on Arria 10 SX



Adapter Boards for IP Core Evaluation

AB Series are extension adapters that simplify Gigabit IP core evaluation on Altera FPGA boards, enabling quick bring-up and on-hardware testing.

Pre-Purchase Evaluation

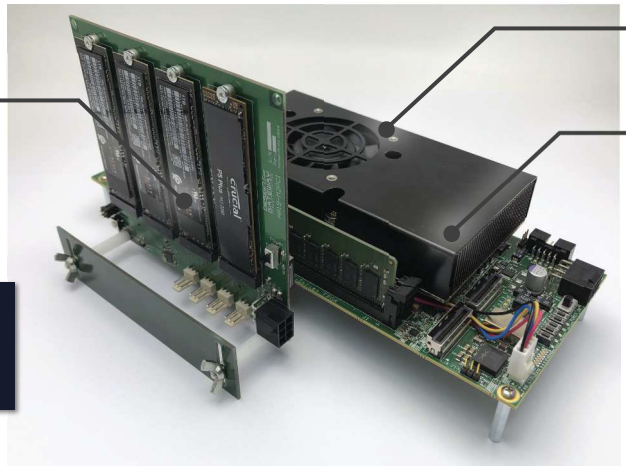
Accelerate Your Decision

Program the FPGA board with the evaluation file downloaded from DG website

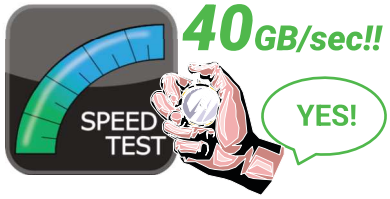
sof file

AB19-M2PCI
& NVMe PCIe Gen5 SSD x4

Agilex™ 7 FPGA I-Series Dev kit



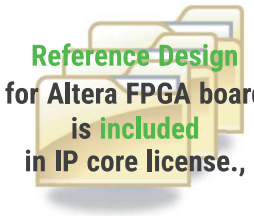
Validate on Real Hardware First
Make a Clear, Confident Decision.

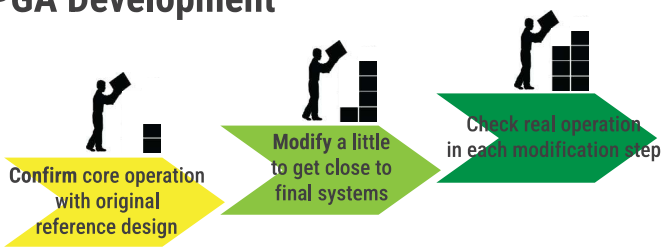


NVMe-IP PCIe Gen5 4 channel RAID0 Evaluation on Agilex™ 7 I-Series Dev kit with AB19-M2PCI

Start from Proven Reference Designs

Accelerate Your FPGA Development

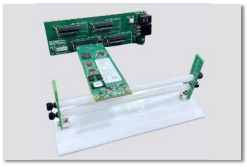






Product Line up

* SSDs not included.



AB21-E1PCIe

PCIe-to-E1.S adapter board for NVMe-IP evaluation with PCIe Gen5 NVMe SSD support; connects up to four E1 SSDs.



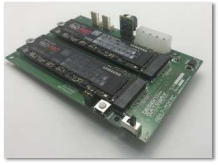
AB18-PCIeX16

PCIe x16 Crossover Adapter Board for NVMe-IP evaluation.



AB20-U2PCIe

PCIe-to-U.2/U.3 adapter board for NVMe-IP evaluation with PCIe Gen5 NVMe SSD support; connects up to four U.2/U.3 SSDs.



AB17-M2FMC

M.2-FMC adapter board for NVMe-IP evaluation, supporting up to two M.2 NVMe SSDs.



AB19-M2PCIe

PCIe-to-M.2 adapter board for NVMe-IP evaluation with PCIe Gen5 NVMe SSD support; connects up to four M.2 NVMe SSDs.



AB09-FMCRAID

FMC-SATA (10ch) adapter board for SATA-IP with RAID evaluation.

Detailed technical information, including datasheets, is available on our website https://dgway.com/en/ab.html

IP Lock

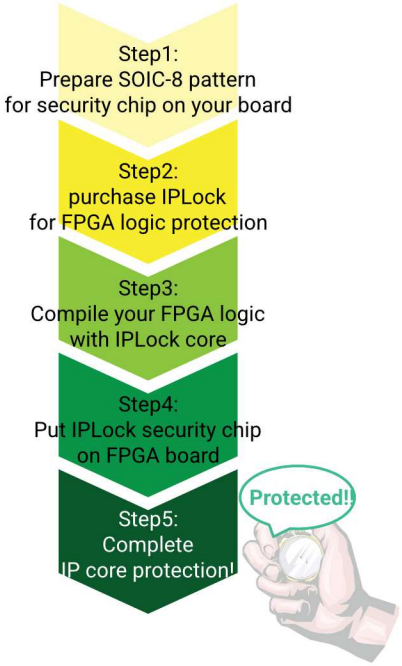
Logic Security System to Protect Intellectual Property from Illegal Duplication



IP Lock is an FPGA logic security system using robust AES encryption. Just include it in your FPGA and connect to an encryption controller chip to protect your IP from illegal duplication.

- Strong security by **AES-128** encryption
- Change & encrypt true random authentication data
- Immediately stop user logic without the chip
- **Just 2 line** connection between FPGA and IP Lock
- **Laboratories Pack** for prototype, already written unique ID
- **Writer Set & Blank Encryption chip** for mass production

Easily Protect Your IP Core & Logic Data





Start with the affordable **Laboratories Pack** for evaluation. Each encryption chip is pre-programmed at shipment with a unique user ID.



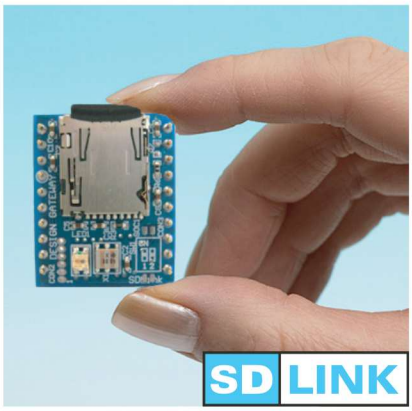
For Mass Production - Use the **IP Lock Writer** with **Blank Chips** to program your own unique IDs.

Detailed technical information, including datasheets,is available on https://dgway.com/en/ip-lock.html

SD LINK

High-Speed FPGA Configuration with microSD Easy FPGA Updates — Just Swap the Card

SDLink is a compact module that performs high-speed FPGA configuration at power-up using data stored on a microSD card. By simply swapping the microSD, FPGA circuit data can be easily updated in the field.





Drastic short programming time for large scale FPGAs!!

Just **3 sec** to program **20MBytes (=160Mbit)** configuration data.
(comparison with on board flash, it takes about 7 minutes...)



Instant FPGA Updates - Simply Swap the microSD!

Convenient update without Programming tools,
Download cable and System suspended.



SDLink Introduction & Demo Video



IPLock Introduction & Demo Video

Detailed technical information, including datasheets, is available on https://dgway.com/en/sd-link.html

Technical Documents on Website



NVMe-IP core series page

Find the latest IP core information and technical documents on the Design Gateway website.

Technical Documents

Datasheet
Reference Design Document
Demo Instruction



Free Evaluation Demo Files

Performance Demo Videos



Sales Materials

Brochure
Presentation
Selection Guide



Performance Evaluation Demo on YouTube

Design Gateway IP core performance evaluation demos on real FPGA boards are available on YouTube. Watch the video clips to learn how to run free evaluation demo files with your FPGA development kit.



Recommended contents



NVMe-IP PCIe Gen5 4ch RAID0 Demo on Agilex 7 I-Series Dev Kit



rmNVMe-IP PCIe Gen5 Demo on Agilex 7 I-Series Dev Kit



TOE200G*ADV*-IP performance demo on Agilex 7 I-Series Dev Kit



UDP100G-IP performance demo on Agilex 7 F-Series Dev Kit



QUIC 10G Client IP performance demo on Sulfur Agilex 5 E-Series Dev Kit



100G Ethernet Data Logging by NVMe-IP on Agilex 7 I-Series Dev Kit



WireGuard1G IP performance demo on Sulfur Agilex 5 E-Series Dev Kit



UDP10G-IP performance demo on Agilex 9 Direct RF Series Dev Kit

News & Articles

Design Gateway regularly shares the latest updates in an easy-to-follow format through social media. You can access them directly via the icons in the website header.



Design Gateway's Technology Blog
Technology Articles Featuring DG Products

Design Gateway Hot! News Backnumber

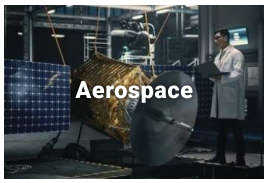
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Get Hands-On with IP Core Demos from GitHub

Proven Applications Across Diverse Industry Segments

Explore real-world examples of how we have met stringent frontline requirements to enable commercialization across diverse industry segments. Visit the "**Vertical Market**" page on our website for more details.

Over **40 GB**/s Transfer ■ **Nano**second Latency ■ **100%** CPU Offload



Space exploration system
Satellite tracking station
Base station system
Radar system
Marine sonar



LiDAR
Pedestrian radar
ECU evaluation device



Cutting-Edge Camera Systems for Live Sport
4K/8K Video Recording System
Variable Speed Video Recorder
Infrared Camera



ADAS
Genetic research
Advanced Scientific Research



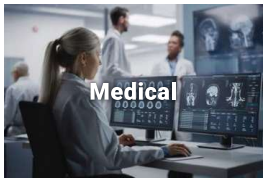
Network Security Accelerator
Smart Network Accelerator
Network Storage Accelerator



High-frequency Trading (HFT)
High-speed Trading (HST)
Accelerated Algorithmic Trading (AAT)
ATM



Pipeline Inspection System
Banknote Validator
Industrial Printer
Wireless Communication system



High resolution CT scanner
X-ray inspection equipment



Storage Option for Measuring Instruments
4K/8K Display tester
Fishfinder System
Telemetry Device
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We offer ready-to-integrate "Special Reference Designs" alongside complimentary "Advanced Reference Designs." By enabling rapid setup of near-production evaluation environments, these designs minimize validation risks and dramatically accelerate your time to market. Visit the "**Zero-CPU Solutions**" page on our website for more details.

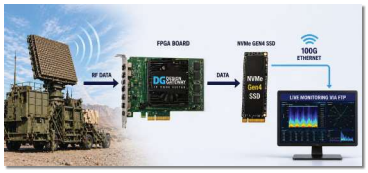
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Solutions page



Special Reference Design
for 100G Ethernet Data Logger



Advanced Reference Design
Ideal for Real-Time SAR Recorders



Advanced Reference Design
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with Live FTP Monitoring



Advanced Reference Design
Ideal for CT Scanner
Real-Time Imaging Pipeline



Advanced Reference Design
for Cloud Storage
with FPGA-Based NVMe over TCP



Optional IP Core
for Multiple NVMe SSDs
via PCIe Switch



Design Gateway is the expert in Intellectual Property (IP) Cores on FPGA,
with more than 38 years experience in FPGA logic design and development.
We can provide total solution with rich IP core portfolio
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