LL10GEMAC IP Demo Instruction

Rev1.0 21-May-20

This document describes the instruction to run loopback demo on FPGA development board. The demo is designed to run LL10GEMAC IP loopback test for measuring the latency time. User sets test parameter on FPGA board and monitors the hardware status via Serial console. More details of the demo are described as follows.

1 Environment Setup

To run loopback demo of LL10GEMAC IP, please prepare following test environment.

1) FPGA development board (ZCU102)
2) SFP+ Loopback cable
3) Two micro USB cables for programming FPGA and Serial console monitoring, connecting between FPGA board and PC
4) Serial console software such as TeraTerm installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
5) Vivado tool for programming FPGA, installed on PC

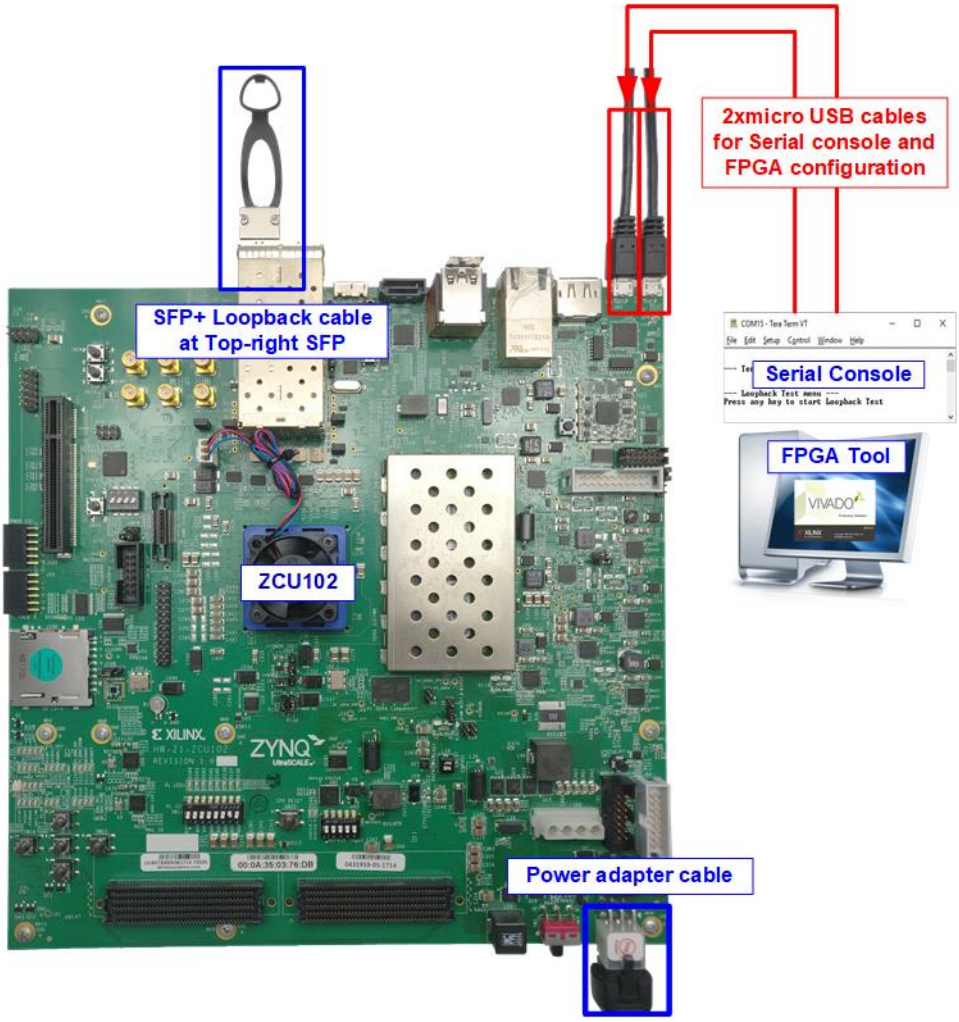

Figure 1-1 LL10GEMAC demo on ZC102

2 FPGA board setup

1) Check DIPSW and jumper setting on FPGA board as shown in Figure 2-1.
   - Insert jumper to J16 to enable Tx SFP+
   - Set SW6=all ONs to use USB-JTAG.

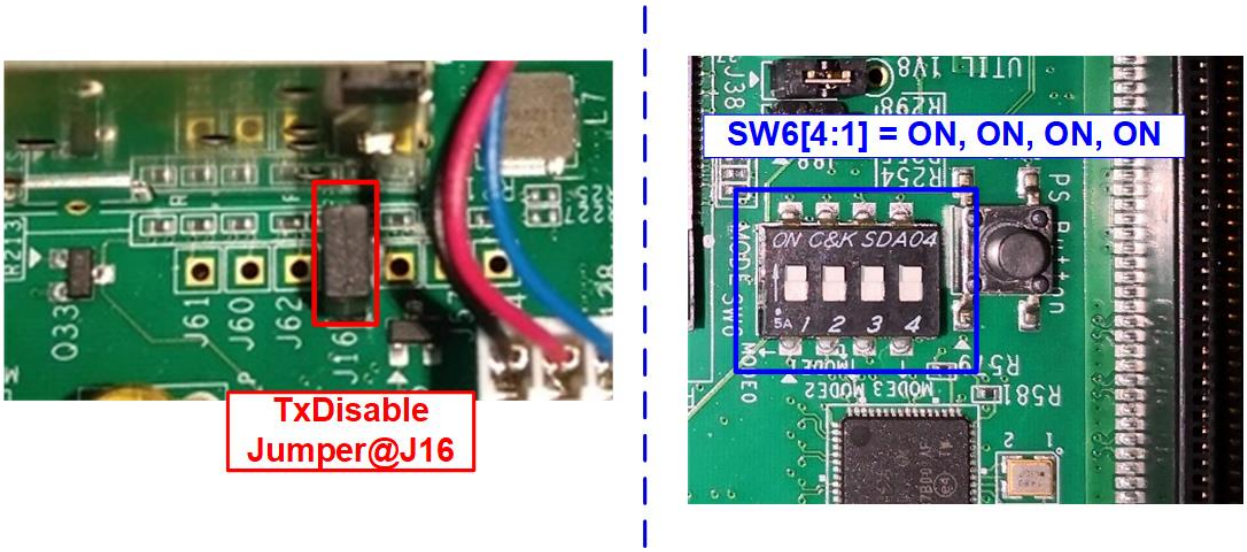

Figure 2-1 ZCU102 board setting

2) Connect two micro USB cables from FPGA board to PC for JTAG programming and USB UART.
3) Connect power supply to FPGA development board.
4) Connect SFP+ Loopback cable at the top-right SFP+ channel, as shown in Figure 2-2.

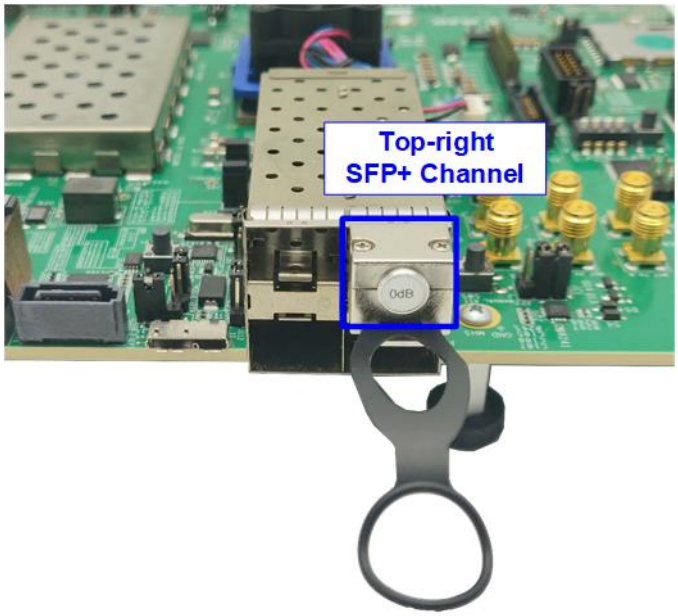

Figure 2-2 Loopback cable on ZCU102 board

5) Power on FPGA board.
6) Open Serial console. When connecting FPGA board to PC, many COM ports from FPGA connection are detected and displayed on Device Manager.

   For ZCU102, select COM port number of Interface0 to be Serial console.

   On Serial console, use following setting: Buad rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

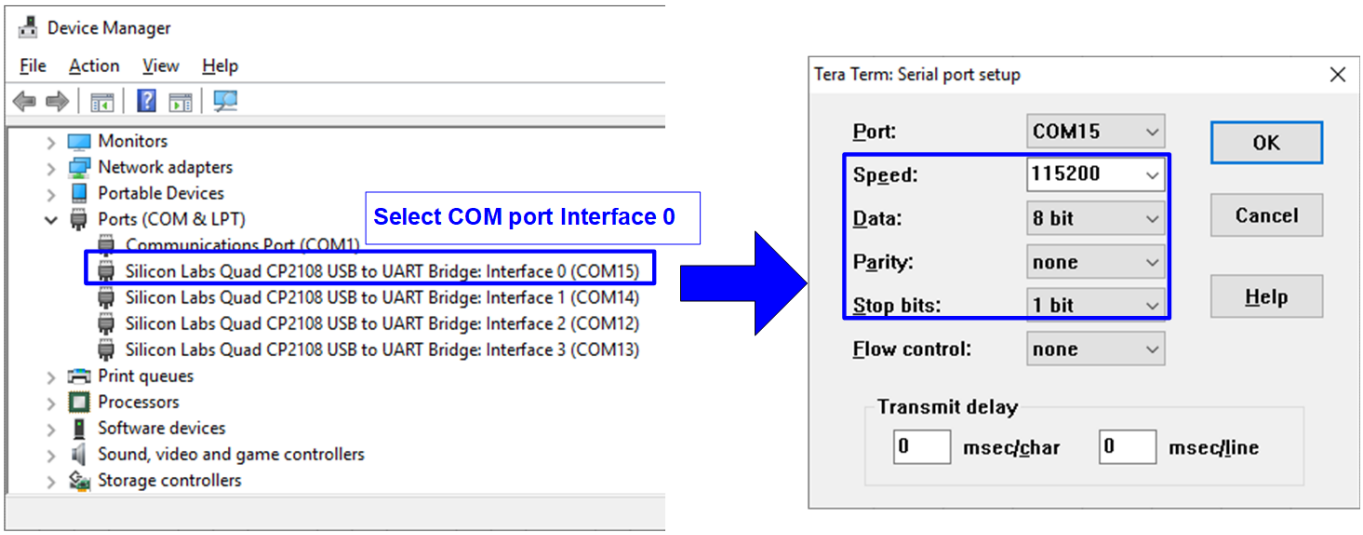

Figure 2-3 COM port number for Serial console

7) Download configuration file and firmware to FPGA board.

   Open Vivado TCL shell and change current directory to download folder which includes demo configuration file and command script file for download.

   Type “lpbackll10gemactest_zcu102.bat” to configure FPGA and download firmware, as shown in Figure 2-4.

   After that, main menu is displayed on the console, as shown in Figure 2-5.

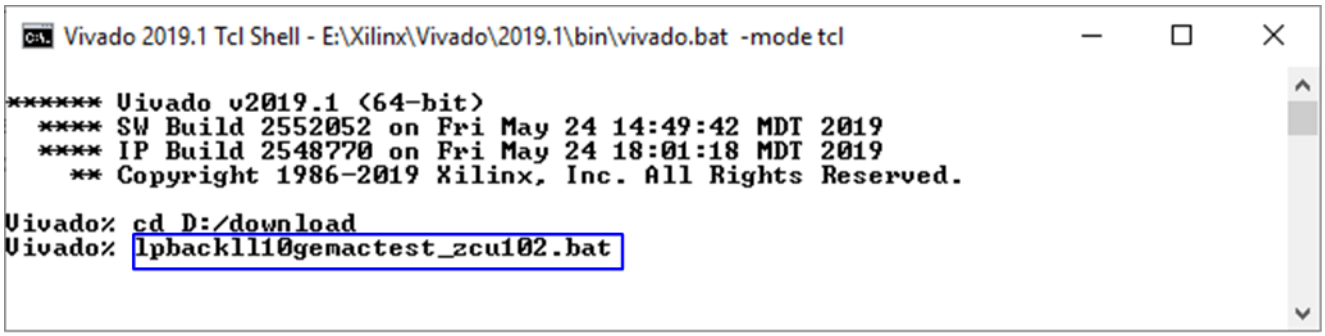

Figure 2-4 Example command script for download to ZCU102 by Vivado tool

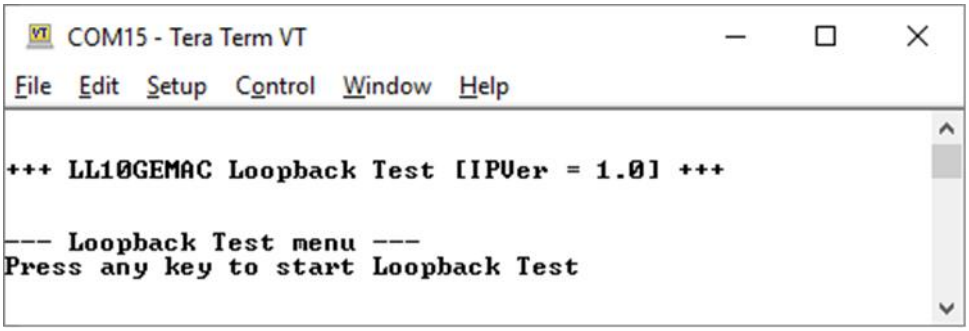

Figure 2-5 Main menu after system boot-up

3 Test menu

User enters any keys on Serial console to start the test operation. The details to run the test is described as follows.

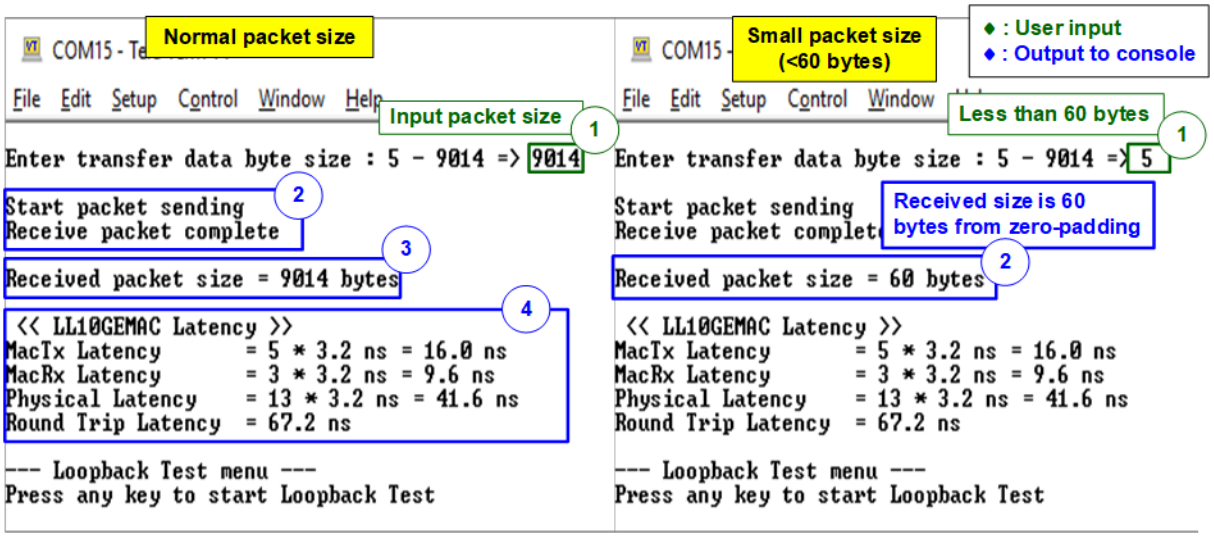

Figure 3-1 Example test result

1) On Serial console, input packet size parameters. Unit of transfer size is byte. Valid value is 5 – 9014. The input is decimal unit when user inputs only digit number. User can add "0x" to be a prefix for hexadecimal unit.
   Note: If the packet size is less than 60, zero-padding is filled by LL10GEMAC-IP.
2) If input is valid, "Start packet sending" is displayed when test logic begins packet sending out. "Receive packet complete" is displayed after the sent packet is returned to the test logic completely.
3) Total received size is displayed on the console. Typically, the received size must be equal to the input size from user. However, if the packet size is less than 60 bytes, the received packet size is equal to 60 from zero-padding, filled by LL10GEMAC-IP.
4) Latency time of each submodule are displayed on Serial console.
   a) MacTx Latency Time: The latency time of Tx data path within LL10GEMAC IP in clock cycle unit (3.2 ns per 1 clock cycle) and nanosecond unit.
   b) MacRx Latency Time: The latency time of Rx data path within LL10GEMAC IP in clock cycle unit (3.2 ns per 1 clock cycle) and nanosecond unit.
   c) PMA Latency Time: The latency time of transceiver (PMA) and SFP loopback cable in clock cycle unit (3.2 ns per 1 clock cycle) and nanosecond unit.
   d) Round Trip Latency Time: The sum of all latency times in the loop back test in nanosecond unit.

If the input is invalid, “Out-of-range input” is displayed and the operation is cancelled, as shown in Figure 3-2.

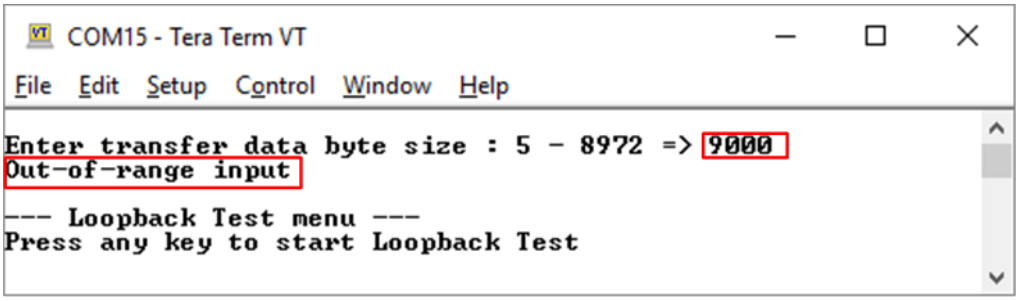

Figure 3-2 Error from invalid packet size

4 Revision History

Revision	Date	Description
1.0	21-May-20	Initial version release