The Very Best Solution for Data Recording Application!

Agenda

- NVMe-IP Introduction
  - Summary, Lineup, Merit
  - High Performance and Compact Size
  - Easy User Interface
  - Rich Features
  - Development Environment/Reference Design
- Optional product (exFAT-IP core)
- Application
What’s NVMe-IP

- **What’s NVMe-IP?** -> Directly connect NVMe SSD with FPGA
- **How to use?** -> Just connect with user logic. No need for CPU, its F/W, External Memory
- **Application** -> Best for ultra high speed data recording system
- **User Merit?** -> Can develop Storage Application in short period

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**NVMe-IP Lineup**

- Multiple lineup for various functions
- PCIe Soft-IP furnished version (Gen3) available
- raNVMe-IP suitable for random access application

<table>
<thead>
<tr>
<th>Core type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard NVMe-IP core</td>
<td>Standard core using Avalon-ST PCIe Hard IP in FPGA</td>
</tr>
<tr>
<td>NVMeG3-IP core</td>
<td>PCIe Soft-IP furnished in NVMe-IP, 4-Lane PCIe Gen3</td>
</tr>
<tr>
<td>NVMeSW-IP core</td>
<td>Multiple SSD connection via external PCIe switch</td>
</tr>
<tr>
<td>raNVMe-IP core</td>
<td>Supports random read or write access</td>
</tr>
</tbody>
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27-Aug-20
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PCIe Soft-IP furnished IP core

- **NVMeG3-IP core**
  - Can operate without Avalon-ST PCIe Hard IP
  - Includes data link layer and connect with transceiver by PCIe Gen3
  - More SSD connection regardless of PCIe Hard IP count in FPGA.

raNVMe-IP for random access

- User can select either Write or Read operation
- Executes 32 commands at maximum concurrently with different (random) address.
- Write or read data per one command is fixed to 4KBytes.
NVMe-IP Merit

1. High Performance and Compact size
   - Write=2145MB/s, Read=3347MB/s (measured by Arria10SoC)
   - Support PCIe GEN3 (Operation confirmed on Arria10SX/GX board)
   - Core size: 1820ALM, 3680DFF (for Arria10SX case)

2. Interface: Simple and easy connection
   - User I/F control is parameter with pulse, data is simple FIFO
   - Use Block Mem. for data buffer (external DDR memory not required)

3. Rich Features: Custom command in addition to Read/Write
   - Supports SMART/FLUSH/Shutdown custom command
   - Supports both legacy 512byte and 4Kbyte Sector format

4. Environment: Full reference design project
   - Full Quartus project with real board operation in the package

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NVMe-IP Merit1: Performance

- Automatic PCIe SSD access by pure hard-wired logic
  - Intelligent state machine for complete read/write command execution
  - Minimum over head and best performance by synchronized circuit
NVMe-IP Merit1: Compact Size (Standard core)

- Optimized size with minimum resource consumption
  - Implements dedicated and optimized logic for NVMe SSD control
- Block memory for data buffer
  - Internal block memory can minimize access overhead

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Logic utilization (ALMs)</th>
<th>Registers</th>
<th>Block Memory bit</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arria V GX</td>
<td>5AGXFB3H4F35C4</td>
<td>212</td>
<td>1835</td>
<td>3637</td>
<td>2,162,688</td>
<td>Quartus II 16.0</td>
</tr>
<tr>
<td>Stratix V GX</td>
<td>5SGXMA7N2F45C2</td>
<td>350</td>
<td>1813</td>
<td>3682</td>
<td>2,162,688</td>
<td>Quartus II 16.0</td>
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<tr>
<td>Arria10 SX</td>
<td>10AS066N3F40E2S6E2</td>
<td>300</td>
<td>1820</td>
<td>3680</td>
<td>2,162,688</td>
<td>Quartus II 16.0</td>
</tr>
</tbody>
</table>

NVMe-IP (standard) Core standalone resource usage

NVMe-IP Merit1: Compact Size (PCIe Soft-IP furnished)

- Resource usage of PCIe Soft-IP furnished IP core

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<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Logic utilization (ALMs)</th>
<th>Registers</th>
<th>Block Memory</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arria10 GX</td>
<td>10AX115S2F46I1SG</td>
<td>300</td>
<td>8560</td>
<td>10884</td>
<td>140 M20Ks</td>
<td>Quartus II 18.0</td>
</tr>
</tbody>
</table>

NVMeG3-IP core (PCIe Soft-IP furnished) standalone resource usage

- Limitation point of NVMeG3-IP core
  - PCIe Gen3 only, not support other speed (Gen1/2)
  - 4-Lane only, not support other lane count (1/2/8/16)
  
  (Ask other lane count as core customization)
**NVMe-IP Merit2: Command I/F**

- **Easy Connection User I/F**
  - Set Command/Address/Length
  - Issue UserReq pulse

- **Full Automatic control for SSD access**
  - User only can wait UserBusy negation

  ![Command I/F waveform]

- Issue command by UserReq together with Cmd, Addr, and Len
- Can set next parameter for next access after UserBusy assertion

  ![Basic Command I/F Signals]

- UserCmd[1:0]
- UserAddr[47:0]
- UserLen[47:0]
- UserReq
- UserBusy

**NVMe-IP Merit2: Data I/F**

- **Simple 128bit FIFO for each of read and write**
  - General FIFO of standard Intel library
  - Data buffer using 256KByte Block memory in NVMe-IP

  ![Data path of NVMe-IP]
NVMe-IP Merit 3: Rich Features

- SMART command for SSD health condition check
  - Can monitor internal temperature, total write size, etc.
- FLUSH command to force cache flush operation
  - User can adjust trade-off between performance and data evacuation
- Safe Shutdown before SSD power down
  - IP-core executes safe shutdown by user request
- Supports both 512bytes and 4Kbytes sector format
  - IP-core automatically selects sector format via Identify command

<table>
<thead>
<tr>
<th>SMART Log Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature           : 32 Degree Celsius</td>
</tr>
<tr>
<td>Total Data Read       : 47669 GB</td>
</tr>
<tr>
<td>Total Data Written    : 65973 GB</td>
</tr>
<tr>
<td>Power On Cycles       : 3991 Times</td>
</tr>
<tr>
<td>Power On Hours        : 79 Hours</td>
</tr>
<tr>
<td>Unsafe Shutdowns      : 220 Times</td>
</tr>
</tbody>
</table>

NVMe-IP Merit 4: Environment

- Real operation check with Intel evaluation board
- Free sof-file for evaluation before IP-core purchase
**NVMe-IP Merit4: Development Tool#1**

- PCIe Adapter board for evaluation (Part#: AB16-PCIeXOVR)
  - Connect FPGA board to PCIe socket on component side
  - Connect PCIe SSD to PCIe socket on solder side
  - SSD R/W access via adapter board from NVMe-IP in FPGA

**NVMe-IP Merit4: Development Tool#2**

- FMC Adapter board for evaluation (Part#: AB17-M2FMC)
  - Two M.2 sockets on component side
  - FMC HPC connector for FPGA connection on solder side
  - High capacity power supply (max 5A for 3.3V output per one SSD)
NVMe-IP Merit 4: Reference Design

- Quartus/Qsys project is attached with NVMe-IP deliverables
- Full source code (VHDL) except IP core
- Can save user system development duration
  - Confirm real board operation by original reference design.
  - Then modify a little to approach final user product.
  - Check real operation in each modification step.

Short-term development is possible without big turn back

Optional product: exFAT-IP Core Introduction

- Optional products for NVMe-IP core
  - Supports data recording with exFAT file format
- PC can directly access to recorded data as a file
  - FPGA writes data to device, reconnect with PC, then PC can read data

PC can directly read recorded data as a file
• Feature description
  – Executes drive format and data write to file by pure hardwired logic.
  – IP core automatically generates file name.
  – User logic sends file data via FIFO interface.

• Limitation
  – Drive must be formatted by the IP core, not by the PC.
  – Files other than those generated by the IP core cannot be written to the drive.
  – File size is determined at format execution and cannot be changed.

Optional product: exFAT-IP (Cont’d 1)

Optional product: exFAT-IP (Cont’d 2)

• Reference design for real operation available
  – Executes test file generation via serial console.
  – User can confirm file read compatibility by drive re-plug to the PC.
NVMe-IP Application Example 1

• Space-Saving FPGA data logging system
  – Latest FPGA + M.2 type SSD

Include data logging user logic and NVMe-IP in FPGA
Record log data to M.2 SSD

System space image by UBGA 484 FPGA and M.2 SSD (unit: mm)

NVMe-IP Application Example 2

• Recording and Analysis system on Linux
  – Mount Linux and user analysis application on SoC device
  – Very high-speed data recording to SSD via NVMe-IP core
  – Data read from SSD via device driver and analyze by user application

Recording and Analysis system on Linux (device driver and reference design available)
NVMe-IP Application Example 3

- **Ultra High-Speed Recorder**
  - Double write speed with multiple SSDs RAID0 configuration
  - Provide RAID0 reference design with 2 NVMe SSDs

![Diagram showing Ultra High-Speed Recorder with NVMe SSDs and Intel FPGA with PCIe Gen3 support]

When system requires 4GByte/sec write speed
Build 2ch RAID0 with 2 NVMe-IP

NVMe RAID system supporting 4GByte/sec recording rate

2020/8/27
Design Gateway

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NVMe-IP Application Example 4

- **Super multi-channel SSD Array by NVMeG3-IP**

![Diagram showing Super multi-channel SSD Array with NVMe SSDs and FPGA (Arria10GX900 UF45Pkg)]

Can build NVMe channels up to ¼ of total transceiver count

24 channels SSD connection possible by Arria10GX (UF45 package with 96 transceivers)

24 channels M.2 SSD Array system using NVMeG3-IP core
For more detail

- Detailed technical information available on the web site.
  - [https://dgway.com/NVMe-IP_A_E.html](https://dgway.com/NVMe-IP_A_E.html)

- Contact
  - Design Gateway Co., Ltd.
  - sales@design-gateway.com
  - FAX: +66-2-261-2290

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Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1E</td>
<td>4-Aug-16</td>
<td>English Temporary Version (Ver0.1E)</td>
</tr>
<tr>
<td>1.0E</td>
<td>10-Aug-16</td>
<td>First release with resource usage information</td>
</tr>
<tr>
<td>1.1E</td>
<td>25-Aug-16</td>
<td>Modify page17 because only one x16 DDR4 device can keep NVMe SSD performance</td>
</tr>
<tr>
<td>1.2E</td>
<td>21-Dec-16</td>
<td>NVMe-IP core improvement by removing external DDR chip for data buffer</td>
</tr>
<tr>
<td>1.3E</td>
<td>23-May-17</td>
<td>Performance improved by internal PCIe bridge in NVMe-IP core</td>
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<tr>
<td>1.4E</td>
<td>6-Jun-17</td>
<td>Data buffer size fixed to 256KByte</td>
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<tr>
<td>1.5E</td>
<td>2-Nov-17</td>
<td>Added Linux driver application and 2ch RAID0 reference design</td>
</tr>
<tr>
<td>1.6E</td>
<td>18-Jul-18</td>
<td>Added 4KB sector format, SMART/FLUSH/Shutdown command support</td>
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<td>1.7E</td>
<td>9-Jan-19</td>
<td>Add FAT32-IP/exFAT-IP for NVMe-IP optional products</td>
</tr>
<tr>
<td>2.0E</td>
<td>3-May-20</td>
<td>Add new product of NVMeG3-IP that includes PCIe Soft IP core inside</td>
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<td>2.1E</td>
<td>27-Aug-20</td>
<td>Add new product of raNVMe-IP for random access application</td>
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