

Optimal Solution for DataRecording Application!

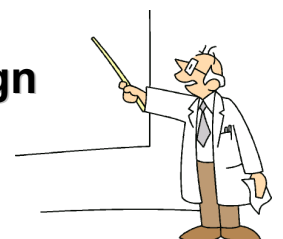
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Agenda

- **NVMe SSD Overview**
 - SSD Trends
 - Merit of NVMe SSD for embedded system
- **NVMe-IP Introduction**
 - Summary
 - High Performance and Compact Size
 - Easy User Interface
 - Rich Features
 - Development Environment/Reference Design
- **Application**



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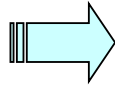
SSD Trends 1

- SATA interface is now performance bottle neck
 - SSD Read/Write speed is limited to 600MB/sec SATA bandwidth
- Move to PCI Express for faster speed
 - PCIe GEN3 x4lane can provide 4GB/sec transfer speed
- M.2 and BGA package suitable for compact application
 - M.2: Wid=22mm, Len=20/42/80/120mm DIMM-like small outline
 - BGA: 20mm x 16mm x 1.5mm, 1gram package



Current 2.5" SATA SSD

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Latest M.2 type PCIe SSD

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BGA type SSD

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SSD Trends 2

- Host Controller Standard moves from AHCI to NVMe
 - Latest standard to extract maximum performance of SSD
 - Extended Queue size, 65536 concurrent command process
 - Most OS provides NVMe driver

FlashMemory NVMe™ Driver Ecosystem

Windows 8.1, Windows 8, Windows 10, redhat, suse, ubuntu, solaris, FreeBSD, vmware ESXi 6.0, Windows Server 2012, Windows Server 2008 R2, Windows 7, vmware ESXi 5.5

Native / in-box
Install NVMe driver

FMS2015 "Annual Update on Interfaces" presentation

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Merit of NVMe SSD for Embedded System 1

- High Bandwidth: 3.5GB/s for Read, 2.5GB/s for Write
- Cost effective: Cost difference from SATA SSD is small



\$197.99 for 500GB

Samsung
Samsung 970 EVO 500GB - NVMe PCIe M.2 2280 SSD (MZ-V7E500BW)
★★★★★ 161 customer reviews
| 55 answered questions
Amazon's Choice for "mz-v7e500bw"
Price: **\$197.99** + \$21.58 Shipping & Import Fees
Deposit to Japan Details
Capacity: 500 GB

1 TB	2 TB	250 GB	500 GB
\$394.99	\$794.99	\$106.82	\$197.99

(Amazon.com 18-Jul-2018)

CrystalDiskMark 6.0.0 x64

	Read [MB/s]	Write [MB/s]
All		
Seq Q32T1	3571.5	2496.7
4KB Q8T8	1415.6	1329.4
4KB Q32T1	299.8	251.7
4KB Q1T1	47.17	146.3

<https://www.techadvisor.co.uk/review/ssd-hard-drives/samsung-970-evo-review-3677171/>

Cost and Performance of M.2 NVMe SSD (Samsung 970 EVO 500GB)

Merit of PCIe SSD for Embedded System 2

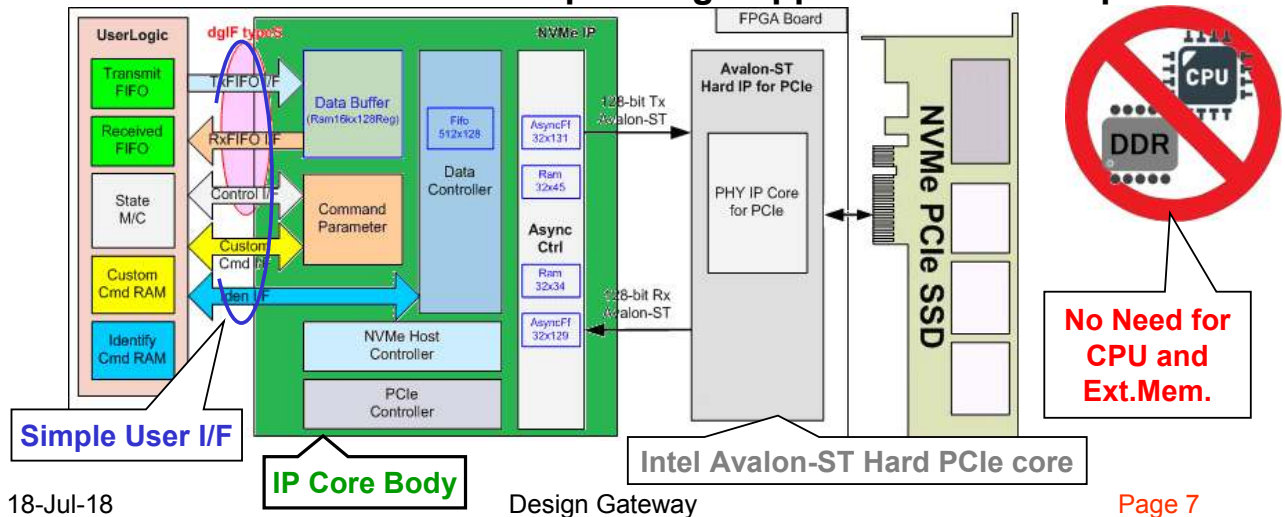
- Various form factor
 - HHL(Half-Height,Half-Length) general PCIe board
 - M.2 cost saving module
 - U.2 (SFF-8639) of 2.5" drive compatible size
 - BGA package for direct mount on PCB

Merit →

<p>Big Capacity</p> <p>HHHL PCIe board</p>	<p>Small, Extractable</p> <p>M.2 module (length=42/60/80mm)</p>	<p>Hot Swap</p> <p>U.2 package</p>	<p>Mount on PCB</p> <p>BGA package</p>
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What's NVMe-IP

- What's NVMe-IP? -> Directly connect NVMe SSD with FPGA
- How to use? -> Just connect with user logic. No need for CPU, its F/W, External Memory
- Application -> Best for ultra high speed data recording system
- User Merit? -> Can develop Storage Application in short period

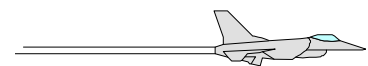


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NVMe-IP Merit

1. High Performance and Compact size
 - Write=2145MB/s, Read=3347MB/s (measured by Arria10SoC)
 - Support PCIe GEN3 (Operation confirmed on Arria10SoC board)
 - Core size: 1820ALM, 3680DFF (for Arria10SX case)
2. Interface: Simple and easy connection
 - Direct connection to Intel Avalon-ST PCIe hard IP-core
 - User I/F control is parameter with pulse, data is simple FIFO
 - Use Block Mem. for data buffer (external DDR memory not required)
3. Rich Features: Custom command in addition to Read/Write
 - Supports SMART/FLUSH/Shutdown custom command
 - Supports both legacy 512byte and 4Kbyte Sector format
4. Environment: Full reference design project
 - Full Quartus project with real board operation in the package



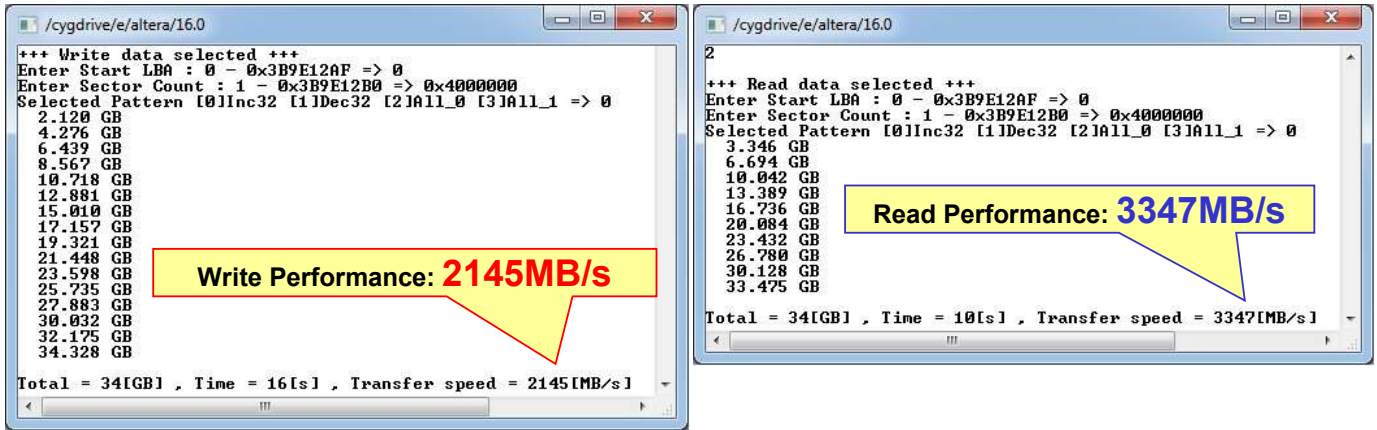
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NVMe-IP Merit1: Performance

- Automatic PCIe SSD access by pure hard-wired logic
 - Intelligent state machine for complete read/write command execution
 - Minimum over head and best performance by synchronized circuit



Performance Evaluation Result (Arria10SoC)

(SSD: Samsung MZ-V6P512BW)

NVMe-IP Merit1: Compact Size

- Optimized size with minimum resource consumption
 - Implements dedicated and optimized logic for NVMe SSD control
- Block memory for data buffer
 - Internal block memory can minimize access overhead

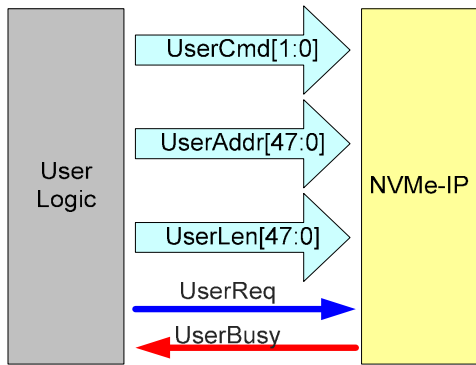
Family	Example Device	Fmax (MHz)	Logic utilization (ALMs)	Registers	Block Memory bit ¹	Design Tools
ArriaV GX	5AGXFB3H4F35C4	212	1835	3637	2,162,688	QuartusII 16.0
Stratix V GX	5SGXMA7N2F45C2	350	1813	3682	2,162,688	QuartusII 16.0
Arria10 SX	10AS066N3F40E2SGE2	300	1820	3680	2,162,688	QuartusII 16.0

NVMe-IP Core standalone resource usage

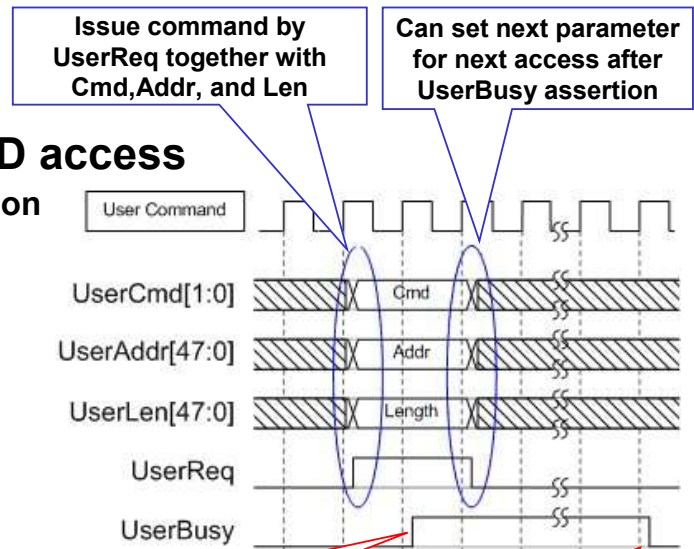
NVMe-IP Merit2: Command I/F



- **Easy Connection User I/F**
 - Set Command/Address/Length
 - Issue UserReq pulse
- **Full Automatic control for SSD access**
 - User only can wait UserBusy negation



Basic Command I/F Signals



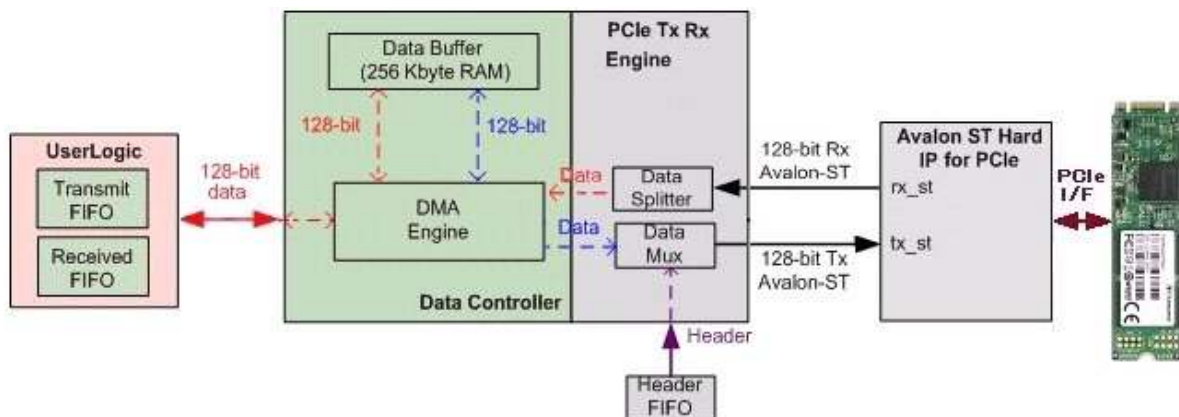
Issue command by UserReq together with Cmd,Addr, and Len
 Can set next parameter for next access after UserBusy assertion
 IP-Core asserts UserBusy='1' and start operation
 UserBusy='0' when operation finish

Command I/F waveform

NVMe-IP Merit2: Data I/F



- **Simple 128bit FIFO for each of read and write**
 - General FIFO of standard Intel library
 - Data buffer using 256KByte Block memory in NVMe-IP



Data path of NVMe-IP

NVMe-IP Merit 3: Rich Features

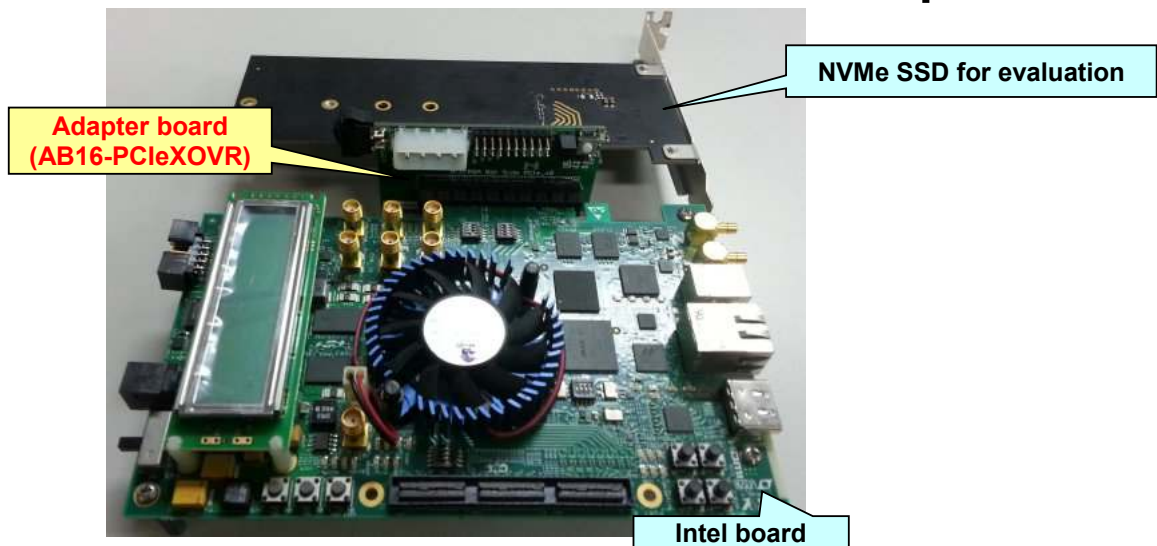
- **SMART command for SSD health condition check**
 - Can monitor internal temperature, total write size, etc.
- **FLUSH command to force cache flush operation**
 - User can adjust trade-off between performance and data evacuation
- **Safe Shutdown before SSD power down**
 - IP-core executes safe shutdown by user request
- **Supports both 512bytes and 4Kbytes sector format**
 - IP-core automatically selects sector format via Identify command

```
<< SMART Log Information >>
Temperature           : 32 Degree Celsius
Total Data Read       : 47469 GB
Total Data Written    : 65973 GB
Power On Cycles       : 3991 Times
Power On Hours        : 79 Hours
Unsafe Shutdowns     : 220 Times
```

SMART command result example

NVMe-IP Merit4: Environment

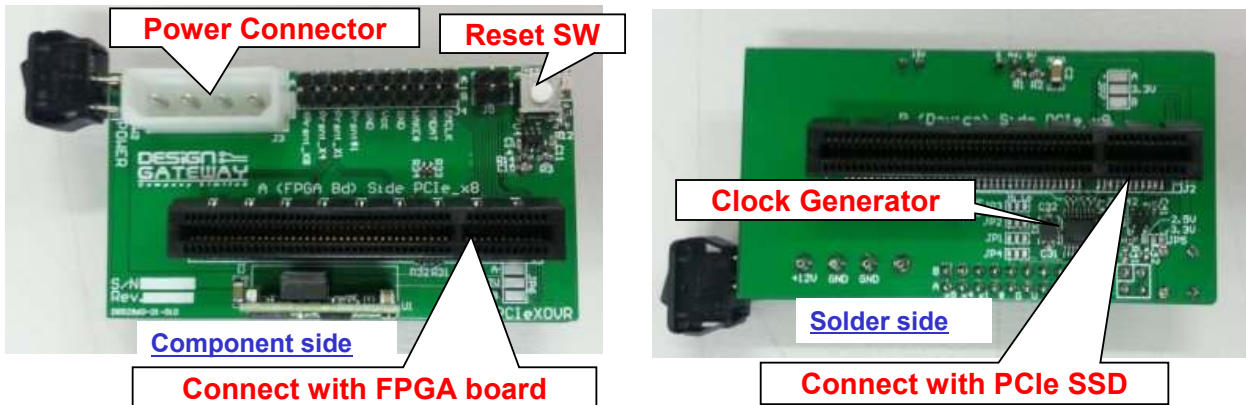
- **Real operation check with Intel evaluation board**
- **Free sof-file for evaluation before IP-core purchase**



NVMe-IP evaluation environment

NVMe-IP Merit4: Development Tool#1

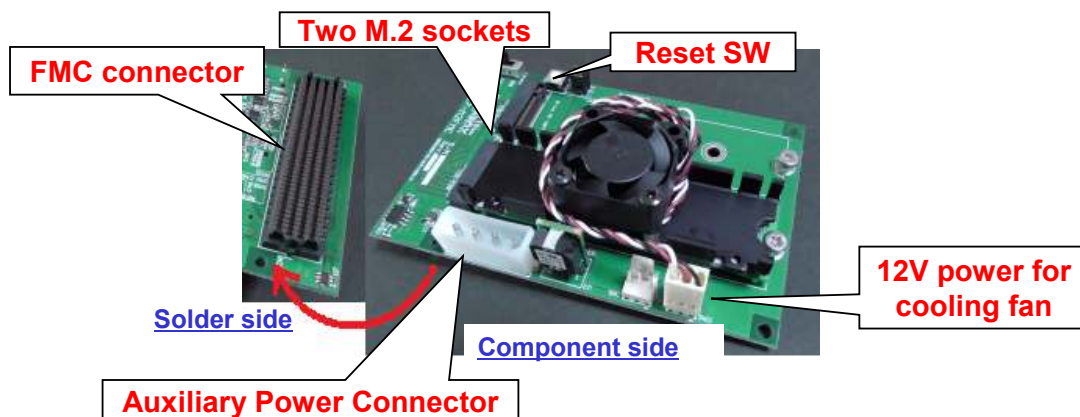
- PCIe Adapter board for evaluation (Part#: AB16-PCIeXOVR)
 - Connect FPGA board to PCIe socket on component side
 - Connect PCIe SSD to PCIe socket on solder side
 - SSD R/W access via adapter board from NVMe-IP in FPGA



PCIe adapter for NVMe-IP evaluation (AB16-PCIeXOVR)

NVMe-IP Merit4: Development Tool#2

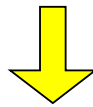
- FMC Adapter board for evaluation (Part#: AB17-M2FMC)
 - Two M.2 sockets on component side
 - FMC HPC connector for FPGA connection on solder side
 - High capacity power supply (max 5A for 3.3V output per one SSD)



FMC adapter for NVMe-IP evaluation (AB17-M2FMC)

NVMe-IP Merit4: Reference Design

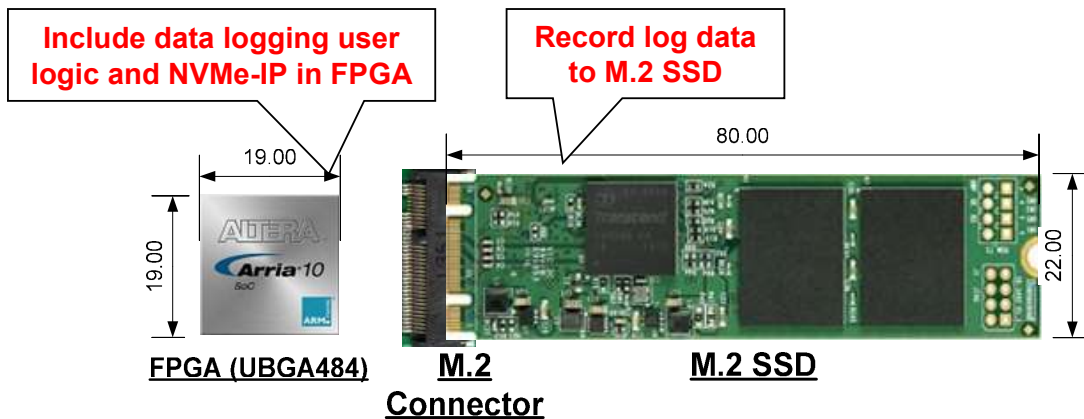
- Quartus/Qsys project is attached with NVMe-IP deliverables
- Full source code (VHDL) except IP core
- Can save user system development duration
 - Confirm real board operation by original reference design.
 - Then modify a little to approach final user product.
 - Check real operation in each modification step.



Short-term development is possible without big turn back

NVMe-IP Application Example 1

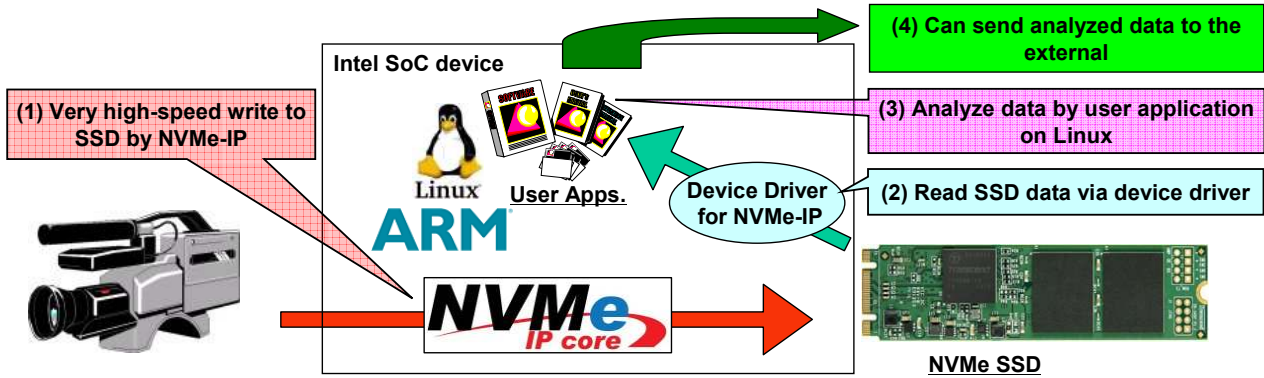
- Space-Saving FPGA data logging system
 - Latest FPGA+M.2 type SSD



System space image by UBGA 484 FPGA and M.2 SSD (unit: mm)

NVMe-IP Application Example 2

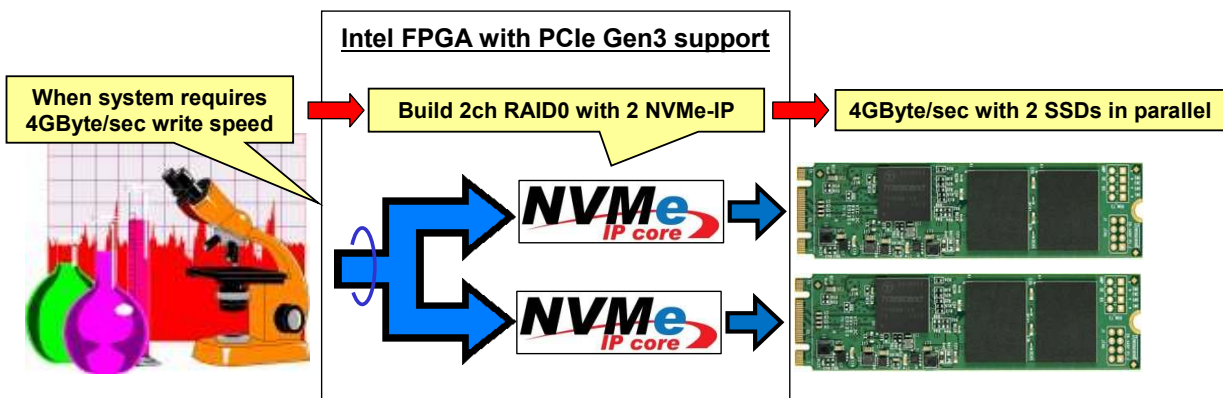
- Recording and Analysis system on Linux
 - Mount Linux and user analysis application on SoC device
 - Very high-speed data recording to SSD via NVMe-IP core
 - Data read from SSD via device driver and analyze by user application



Recording and Analysis system on Linux (device driver and reference design available)

NVMe-IP Application Example 3

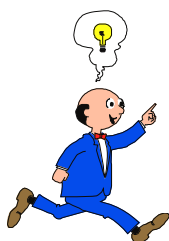
- Ultra High-Speed Recorder
 - Double write speed with multiple SSDs RAID0 configuration
 - Provide RAID0 reference design with 2 NVMe SSDs



NVMe RAID system supporting 4GByte/sec recording rate

For more detail

- Detailed technical information available on the web site.
 - http://www.dgway.com/NVMe-IP_A_E.html
- Contact
 - Design Gateway Co., Ltd.
 - sales@design-gateway.com
 - FAX: +66-2-261-2290



The screenshot shows the Design Gateway website with the following content:

- Header: DG DESIGN GATEWAY
- Navigation: TOP NEWS, GIGA BIT IP CORES (Storage & Network IP), PRODUCTS (PRODUCTS), SERVICE (Technology/Service), ABOUT (COMPANY)
- Section: NVMe IP core PCIeSSD Can Directly Connect To FPGA!
- Text: NVMe IP core operating with Avalon-MM Hard IP for PCIe from Intel is ideal to access NVMe PCIe SSD without CPU and external memory. It is recommended to use in the application which require high capacity storage at very high-speed performance. Small size system can be also designed by M.2 storage which uses PCIe protocol standard. The IP core license includes the reference design for Intel® FPGA boards. It helps you to reduce development time and cost.
- Diagram: FPGA connected to PCIe SSD via PCIe Gen3 8Gbps x 1/4/8 Lane.
- Section: Features
 - Implement application layer to access NVMe PCIe SSD without CPU and external memory (DDR)
 - Simple user interface by d3IP types
 - Direct connect to Avalon-ST Hard IP for PCI Express from Intel by using 128-bit bus interface
 - Include 256 Kbyte RAM to be data buffer
 - Support 6 commands, i.e. IDENTIFY, WRITE, READ, Shutdown, SMART, and Flush
 - Support NVMe device
 - Base Class Code 01h (mass storage), Sub Class code 0Bh (Non-volatile), Programming Interface 02h (NVMMCI)
 - MPSM (Memory Page Size Minimum): 0 (4Kbyte)

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Revision History

Rev.	Date	Description
0.1E	4-Aug-16	English Temporary Version (Ver0.1E)
1.0E	10-Aug-16	First release with resource usage information
1.1E	25-Aug-16	Modify page17 because only one x16 DDR4 device can keep NVMe SSD performance
1.2E	21-Dec-16	NVMe-IP core improvement by removing external DDR chip for data buffer
1.3E	23-May-17	Performance improved by internal PCIe bridge in NVMe-IP core
1.4E	6-Jun-17	Data buffer size fixed to 256KByte
1.5E	2-Nov-17	Added Linux driver application and 2ch RAID0 reference design
1.6E	18-Jul-18	Added 4KB sector format, SMART/FLUSH/Shutdown command support

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