

NVMe-IP Products Selection Guide

Ver1.0E



Standard product



PCIe Soft-IP built-in type



For Start-Stop recorder application



exFAT-IP, FAT32-IP, PCIeSW option

NVMe-IP Products Selection Guide

NVMe-IP product common features

- **Features common to all NVMe-IP core products**
 - **No CPU or external DDR memory required, fully automated NVMe protocol processing on the core.**
 - **Data interface with independent FIFOs for write and read.**
 - **For sequential writing applications such as video recorders and sensor data loggers.**
 - **For sequential readout applications such as pattern generators.**
 - **High speed write/read with multi-channel RAID.**
 - **With exFAT-IP option, record data to SSD on FPGA then re-connect it to PC to read data.**

Introduction of each NVMe-IP core product series

Product series	Product features	Suitable applications
NVMe-IP core	<ul style="list-style-type: none"> ✓ Standard NVMe-IP core product ✓ Work with PCIe Hard-IP built-in FPGA 	<ul style="list-style-type: none"> ✓ Low resource consumption
NVMeG3-IP core	<ul style="list-style-type: none"> ✓ No PCIe Hard-IP required, PCIe Soft-IP is built into the core. ✓ Fixed Gen3 (8Gbps) link speed. ✓ Fixed 4-Lane, (can customize lane count). 	<ul style="list-style-type: none"> ✓ Multi-channel ✓ When PCIe Hard-IP count is not enough.
NVMeG4-IP core	<ul style="list-style-type: none"> ✓ No PCIe Hard-IP required, PCIe Soft-IP is built into the core. ✓ Fixed Gen4 (16Gbps) link speed. ✓ Fixed 4-Lane, (can customize lane count). 	<ul style="list-style-type: none"> ✓ Multi-channel ✓ PCIe Hard-IP not support Gen4 case.
raNVMe-IP core	<ul style="list-style-type: none"> ✓ Fixed data size of each command to 4KByte. ✓ 32 concurrent command execution during Read and Write. ✓ High performance under both sequential and random access. 	<ul style="list-style-type: none"> ✓ Database search ✓ Video/Data recoder

NVMe-IP Core standard product

- Minimum resource consumption
- Many reference design on standard FPGA eval-bd available.
 - 2ch/4ch RAID, external DDR design, etc.

Many redesign for both Intel/Xilinx version available on Web site!

IPコア & オプション	データシート	リファレンス デザイン ドキュメント	デモ手順書	FPGAボード セットアップ ドキュメント	無償評価デモファイル *パスワード依頼	YouTube デモビデオ
Agilex F-series用 NVMe-IP	Rev1.0	Rev1.0	Rev1.0	Rev1.2	Agilex F-series	NVMe Gen4 Gen5 RAID
Agilex F-series用 NVMe-IP4ch RAID0		Rev1.1	Rev1.1	Rev1.0	Agilex E-series	Intel Agilex
Stratix® 10 GX 用 NVMe-IP	Rev1.0	Rev1.0	Rev1.2	Rev1.2	Stratix® 10 GX	
NVMe-IP	Rev3.1J	Rev3.1J	Rev3.0J		Arria® 10 SX Arria® 10 GX Cyclone® 10 GX Arria® V GX	NVMe IP core Arria 10 SX Dev Kit
	Rev1.4 (英語版)	Rev1.3 (英語版)	Rev1.2 (英語版)	Rev1.2	ALABIC DevKit Terasic TB5	ALABIC DevKit
2ch RAID0		Rev1.1	Rev1.1		Arria 10 SX Alaric DevKit	NVMe IP core 2ch RAID Arria 10 SX

Intel version reference design

January 17, 2022

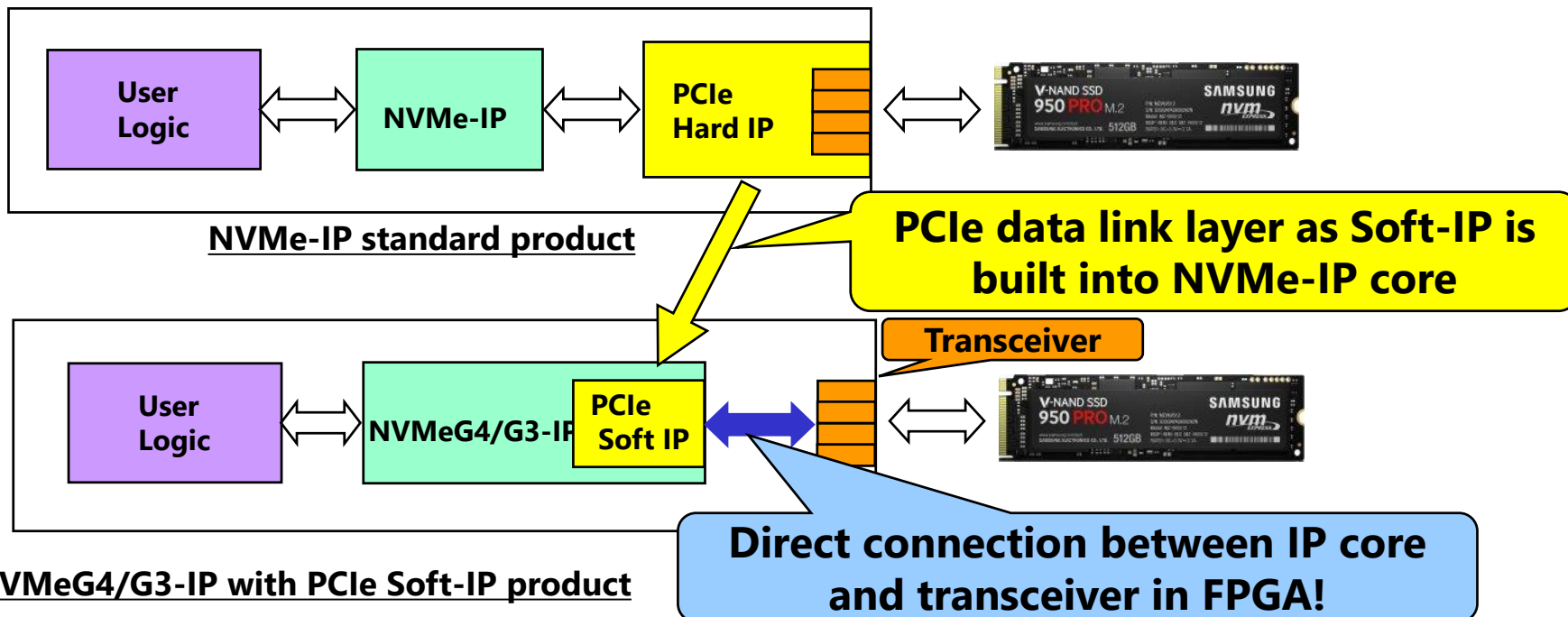
IPコア & オプション	データシート	リファレンス デザインドキュメント	デモ手順書	FPGAボード セットアップ ドキュメント	無償評価デモファイル *パスワード依頼	YouTube デモビデオ
ALVEO用 NVMe-IP (Gen4)	Rev1.0	Rev1.0	Rev1.4	Rev1.3	U50	
NVMe-IP	Rev3.7 Rev3.2J	Rev3.7 Rev3.1J	Rev4.3	Rev4.3	ZCU106 (AB18) ZCU106 (AB17) VCU118 (AB17) VCU118 (AB18) KCU105 (AB18) KCU105 (AB17) KC705 AC701 VC707 VC709 ZC706 Z7045	NVMe IP core ZCU106 NVMe IP core KCU105
	2ch RAID0		Rev1.4	Rev2.1	Rev2.1	KCU105 (AB18) KCU105 (AB17)
4ch RAID0		Rev1.1	Rev1.1		VCU118	
DDR使用 サステイナブル		Rev1.2	Rev1.1		KCU105	Standard NVMe IP core DDR Reference Design

Xilinx version reference design

Design Gateway

PCIe Soft-IP built-in product

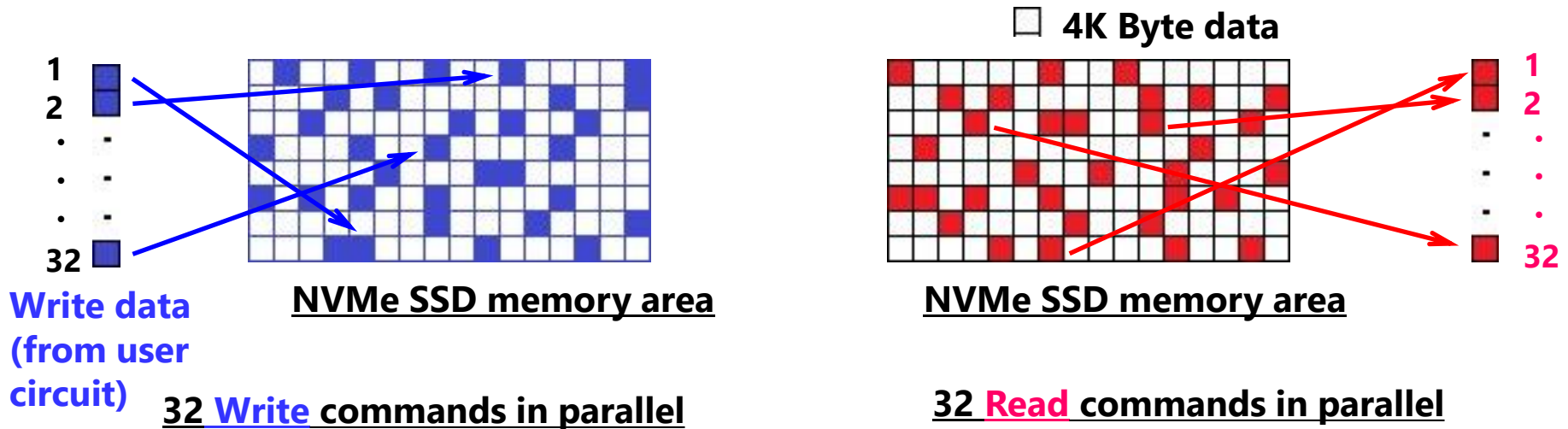
- PCIe Hard-IP in FPGA is not necessary
- Fixed Gen3 or Gen4, fixed 4-Lane
- The number of connected SSDs is not limited by the number of PCIe hard IPs!



raNVMe-IP core product

- raNVMe-IP core

- Concurrent either of write or read 32 commands execution.
- Data size per one command is fixed to 4K Byte.
- High performance: **Write=592KIOPs**、 **Read=226KIOPs**



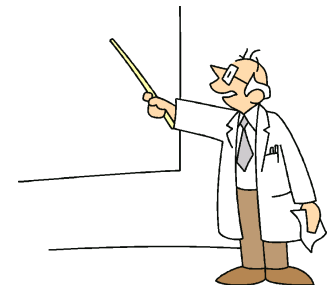
raNVMe-IP core Concurrent command execution image

Optional products

Option	Product features	Suitable applications
exFAT-IP core FAT32-IP core	<ul style="list-style-type: none"> ✓ Write or read data with exFAT/FAT32 format. ✓ No CPU required, but write operation is limited to sequential access only. 	<ul style="list-style-type: none"> ✓ Write data with file system, re-connect with PC to read from file.
PCIe switch support option	<ul style="list-style-type: none"> ✓ It supports external PCIe switch device connection. ✓ Access to selected SSD via switch device. ✓ Customization for original specification. 	<ul style="list-style-type: none"> ✓ Multi-channel (capacity expansion)

Remark :

* Optional products cannot be applied to raNVMe-IP core.



Optional products #1 (FAT32-IP/exFAT-IP)

- **Features**
 - Implements file system by hard-wired logic, no CPU necessary.
 - Supports 3 commands of format, file write, and file read.
- **Target Application**
 - Write data to SSD as a file, then reconnect with PC to read data.
- **Limitation**
 - Drive must be formatted by the IP core, not by the PC.
 - File write operation must be addendum, so random write inhibited.



Comparison of FAT32-IP and exFAT-IP

Item	FAT32-IP	exFAT-IP
Drive Capacity	64MB - 2TB	8GB - 64PetaB
File Size	32MB - 2GB	32MB - 512GB
Directory count	No (root directory only)	16 directory
Resource (Intel) *1	840ALM+42Kbit(Ram)	1840ALM+132Kbit(Ram)
Resource (Xilinx) *2	310CLB+2.5BRAMTile	570CLB+4BRAMTile
Name Hash	Not supported	Supported
Check Sum	Not supported	Supported

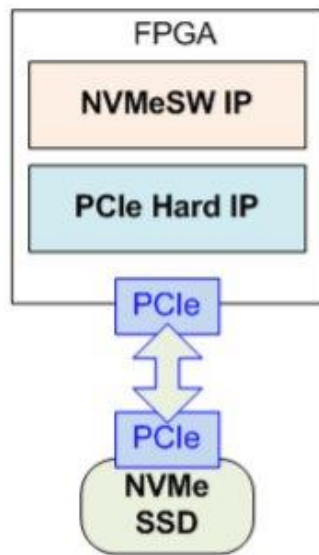
Comparison of FAT32-IP and exFAT-IP

※1 device family = Arria10

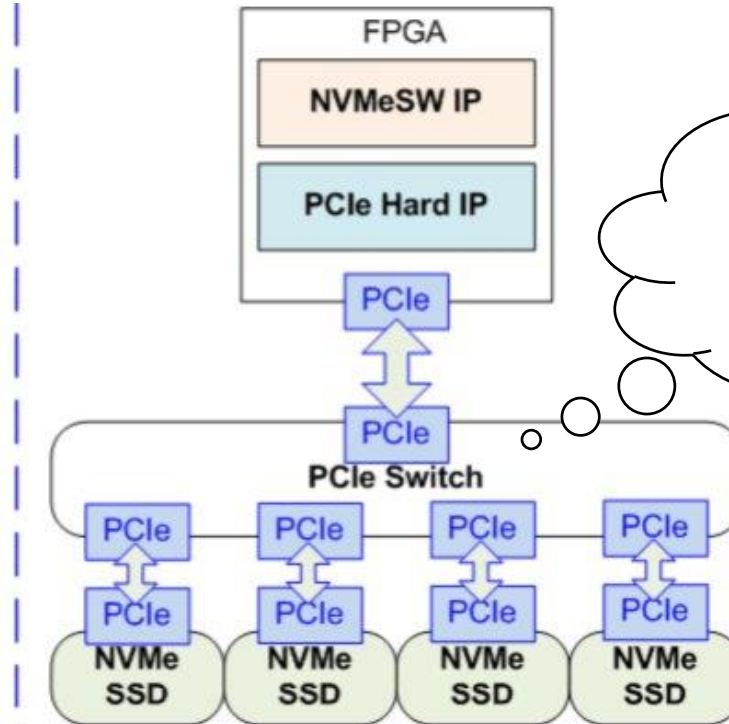
※2 device family = Kintex-Ultrascale

Optional product #2 (PCIe switch support)

- Access to SSD via external PCIe switch device.
- Application for storage capacity expansion.



Standard product connection



PCIe switch option product connection

URL list of each product

- **NVMe-IP core standard product and optional product**
 - Intel ver. : https://dgway.com/NVMe-IP_A_E.html
 - Xilinx ver. : https://dgway.com/NVMe-IP_X_E.html
- **NVMeG3/G4-IP (PCIe Soft-IP built-in) product**
 - Intel ver. : https://dgway.com/NVMeG4-IP_A_E.html
 - Xilinx ver. : https://dgway.com/NVMeG4-IP_X_E.html
- **raNVMe-IP product**
 - Intel ver. : https://dgway.com/raNVMe-IP_A_E.html
 - Xilinx ver. : https://dgway.com/raNVMe-IP_X_E.html

Revision History

Rev.	Date	Description
1.0E	January 17, 2022	Initila English version release