NVMe-IP Demo Instruction

Rev1.2 19-Dec-16

This document describes the instruction to run NVMe-IP demo on ArriaV GX Starter board/Arria10 SoC Development board. For the ArriaV GX Starter board, AB16-PCIeXOVR board is required to connect with the NVMe PCIe SSD. The demo is designed to write/verify data with NVMe PCIe SSD. User can control test operation through NiosII command shell.

1 Environment Requirement

To demo NVMe-IP on Altera ArriaV GX Starter board/Arria10 SoC Development board, please prepare the following hardware/software.

1) Altera ArriaV GX Starter board (PCIe Gen2)/Altera Arria10 SoC Development board (PCIe Gen3)
2) PC with QuartusII programmer and NiosII command shell software
3) For ArriaV GX Starter board only, AB16-PCIeXOVR board + PCIeSub board from AB16 delivery set
4) Altera Power adapter
5) NVMe PCIe SSD
6) A cable for programming FPGA and NiosII command shell connecting between FPGA board and PC,
   - USB Type-B cable in case of ArriaV GX Starter board
   - micro USB cable in case of Arria10 SoC Development board

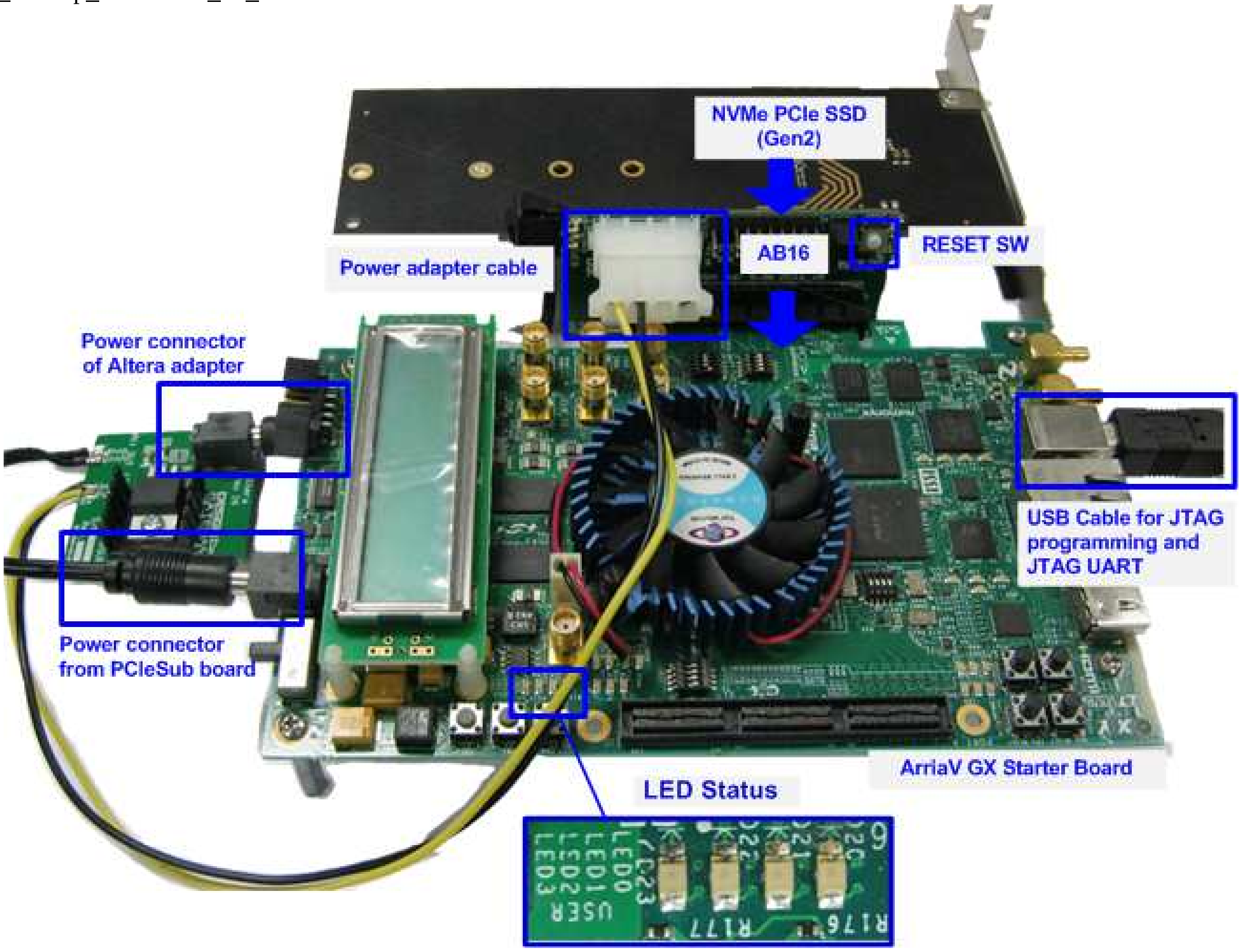


Figure 1-1 NVMe-IP Demo Environment Setup on ArriaV GX Starter Board

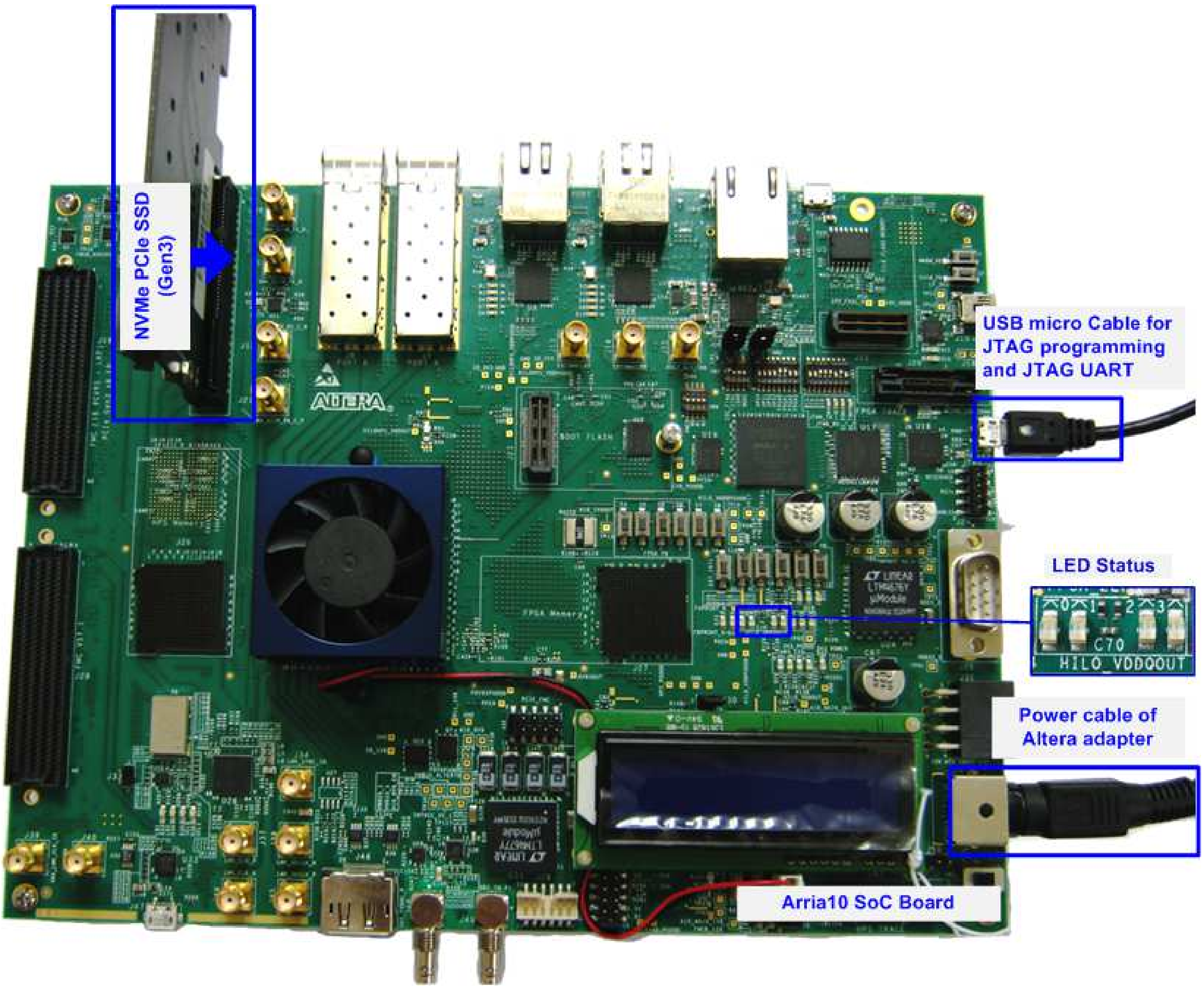


Figure 1-2 NVMe-IP Demo Environment Setup on Arria10 SoC Development Board

2 Demo setup

2.1 PCIe setup

a) ArriaV GX Starter board by AB16-PCIeXOVR

- Power off system.
- Connect power connector on PCIeSub board to power connector on FPGA board.
- Connect ATX power connector on PCIeSub board to AB16-PCIeXOVR board.
- Connect Altera power adapter to connector on PCIeSub board.

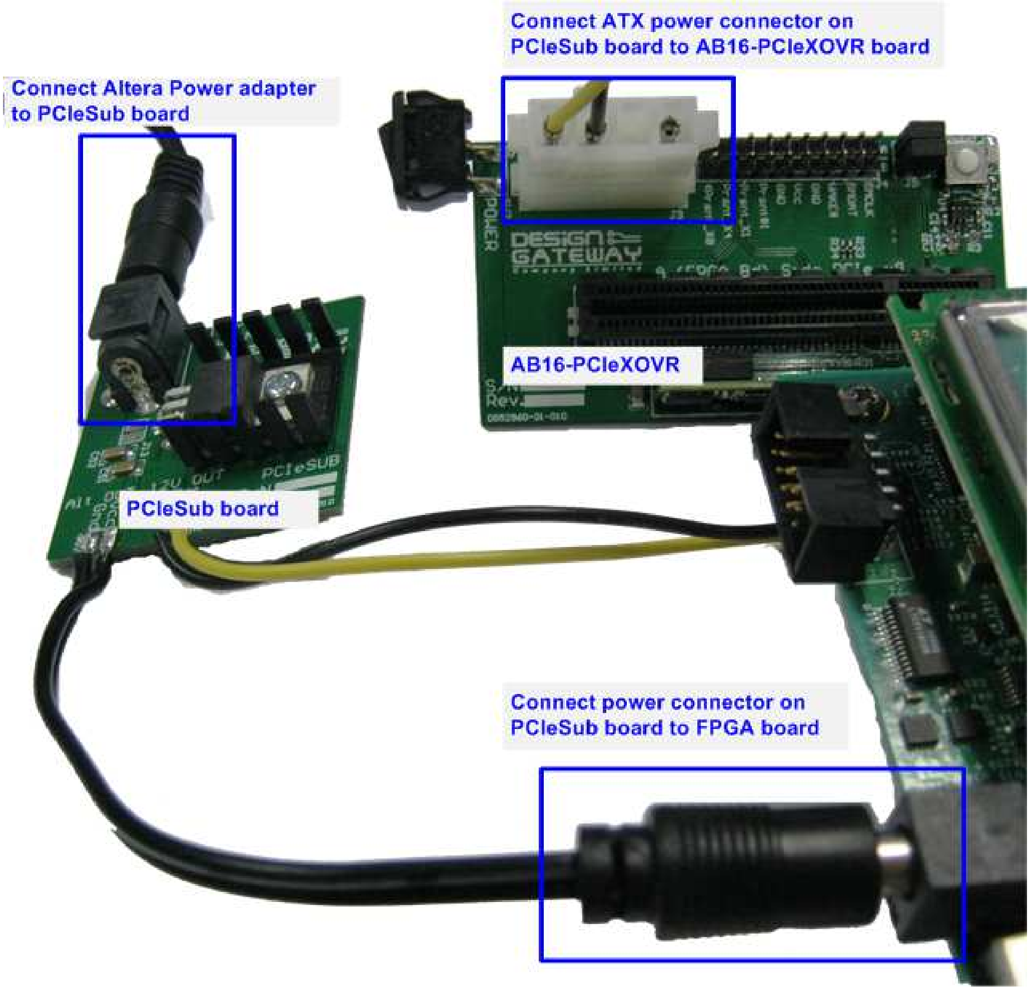

Connect ATX power connector on PCIeSub board to AB16-PCIeXOVR board
Connect Altera Power adapter to PCIeSub board
AB16-PCIeXOVR
PCIeSub board
Connect power connector on PCIeSub board to FPGA board

Figure 2-1 Connect PCIeSub board to FPGA board, AB16, and Altera adapter

- Connect A Side of PCIe connector on AB16-PCIeXOVR board to PCIe connector on FPGA board, as shown in Figure 2-2.
- Check that two mini jumpers are inserted at J5 connector on AB16.

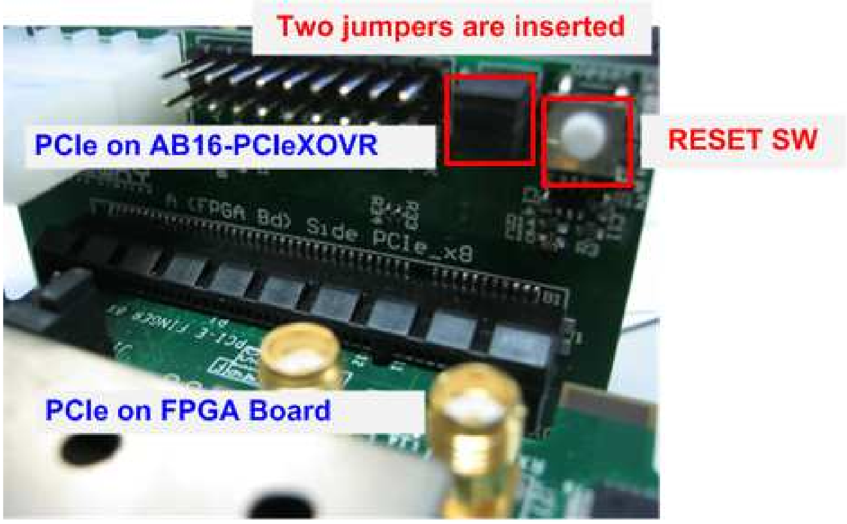


Figure 2-2 Connect PCIe connector between AB16 and FPGA board

- Connect NVMe PCIe SSD to B Side of PCIe connector on AB16-PCIeXOVR board.

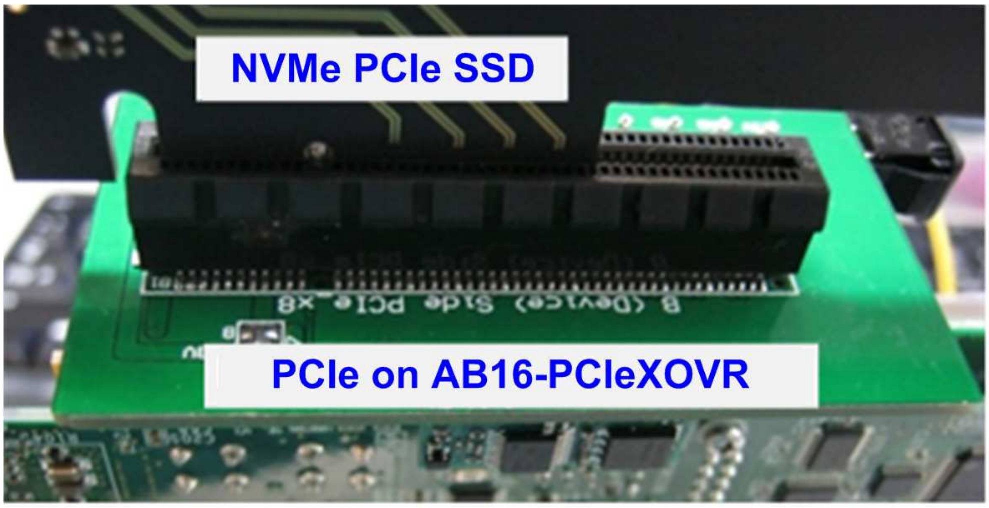


Figure 2-3 Connect NVMe PCIe SSD to AB16 board

- Connect USB Type-B cable from FPGA board to PC for JTAG programming and NiosII command shell.

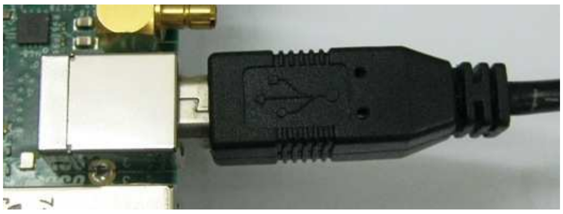


Figure 2-4 USB cable connection

- Power on FPGA development board and power on AB16-PCIeXOVR board.

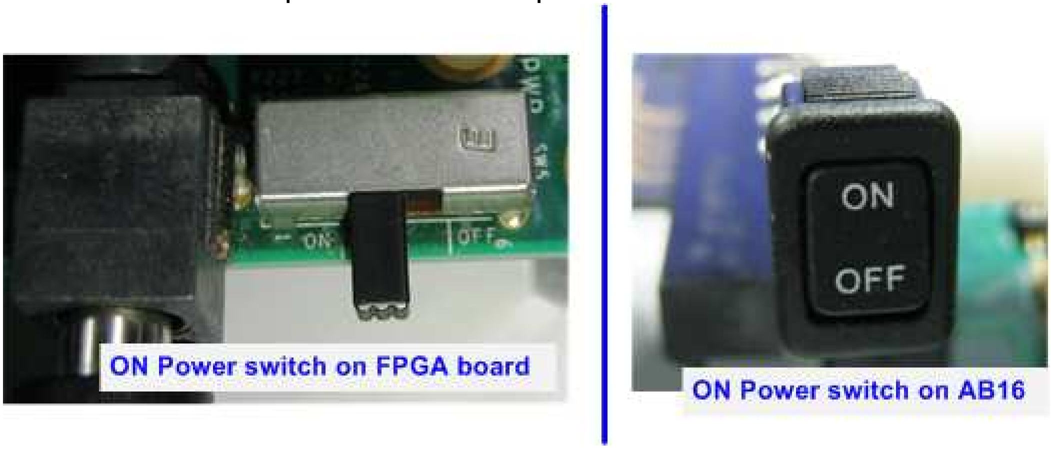


Figure 2-5 Power on FPGA and AB16 board on ArriaV GX Starter board

b) Arria10 SoC Development board by PCIe root complex connector

- Power off system.
- Connect NVMe PCIe SSD to PCIe connector on FPGA board, as shown in Figure 2-6.

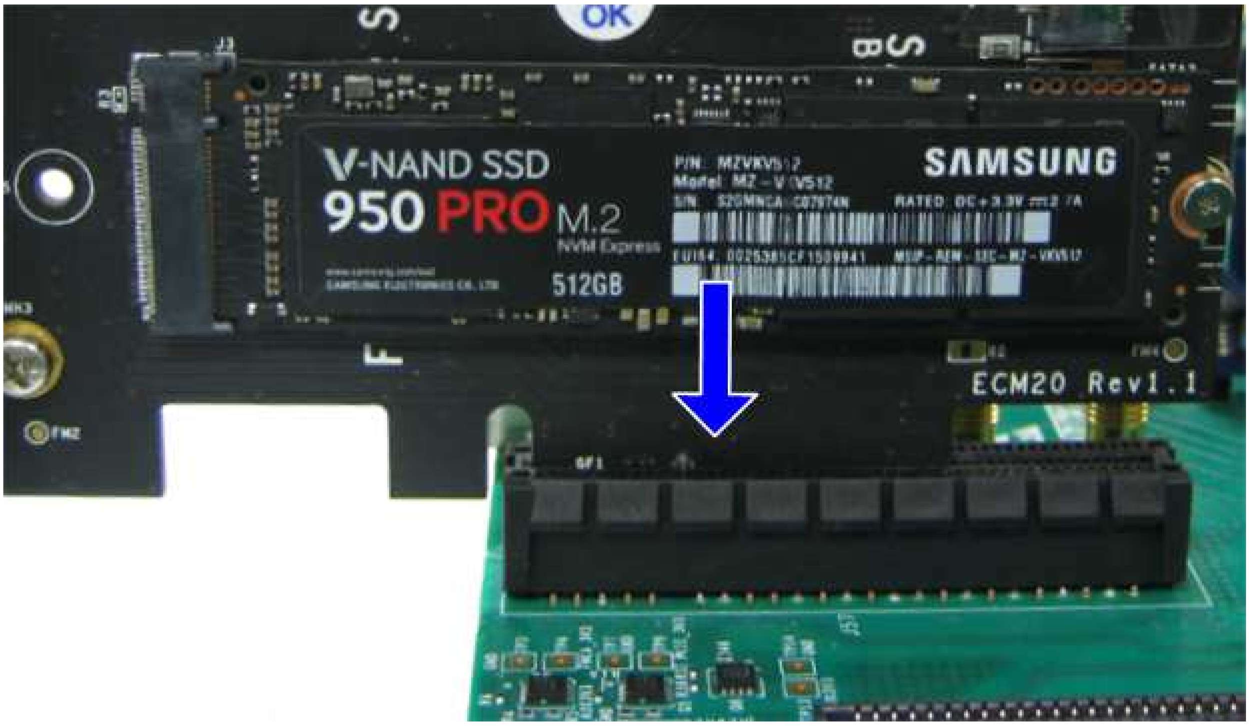


Figure 2-6 NVMe PCIe SSD connection on FPGA board

- Connect micro USB cable from FPGA board to PC for JTAG programming and NiosII command shell, as shown in Figure 2-7.

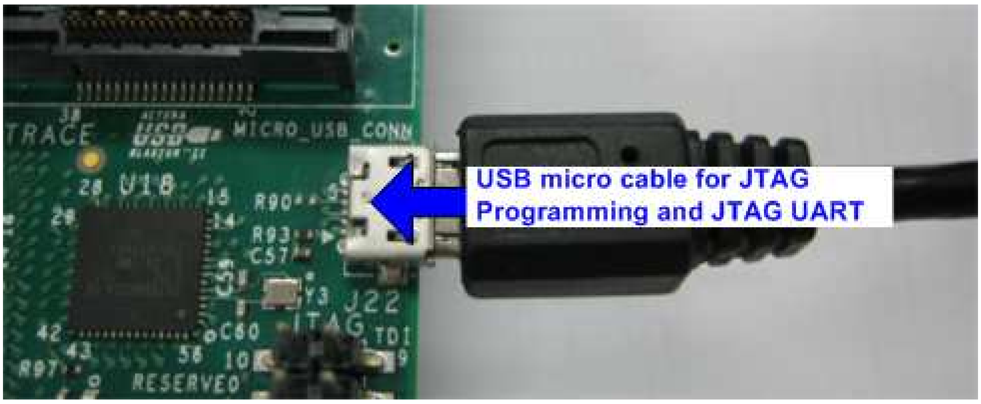


Figure 2-7 USB cable connection

- Set SW1[2] = OFF position to source power to the PCIe, as shown in Figure 2-8.

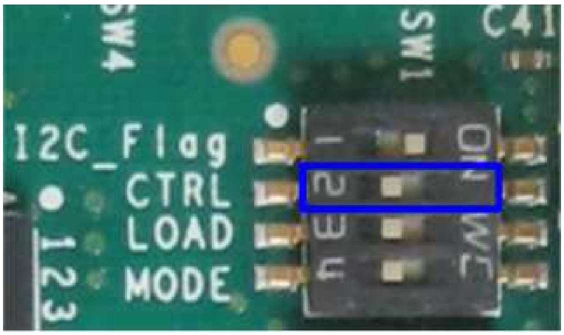


Figure 2-8 Source power to the PCIe for Arria10 SoC board

- Connect Altera power adapter to FPGA board, as shown in Figure 2-9.
- Power on FPGA development board.

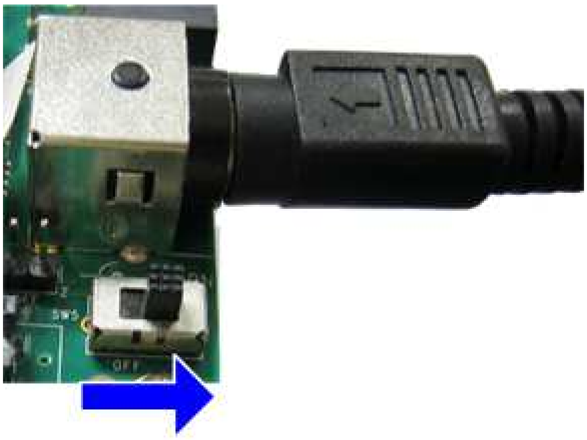
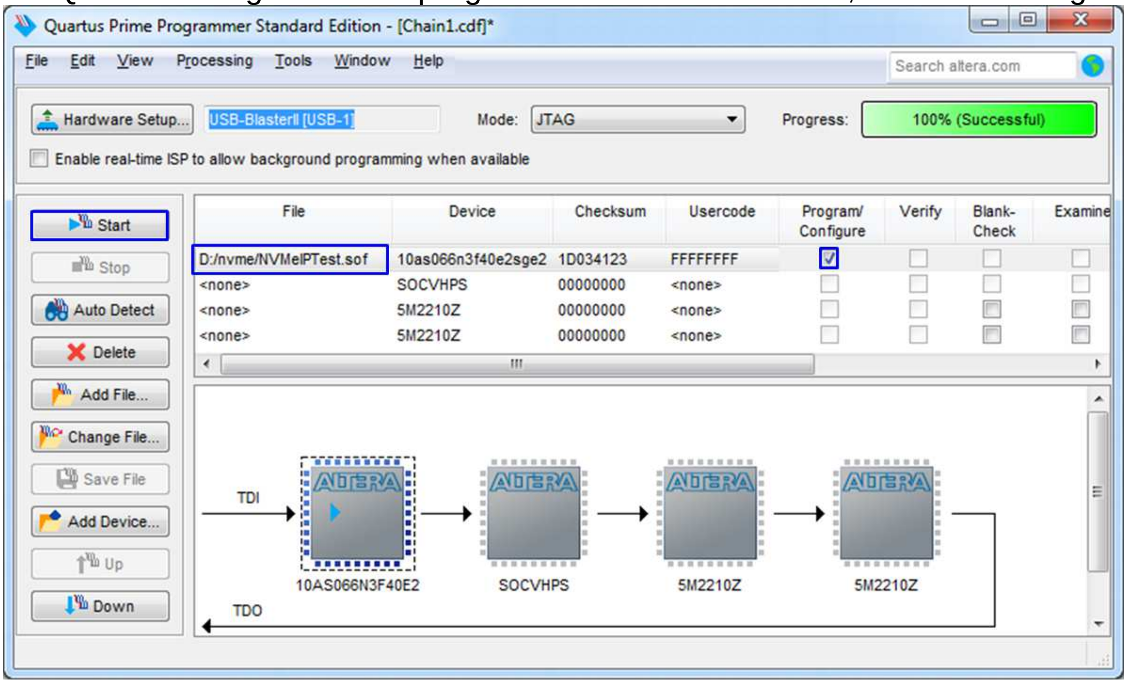


Figure 2-9 Power on FPGA board

2.2 Board setup

- Use QuartusII Programmer to program “NVMeIPTest.sof” file, as shown in Figure 2-10.



Quartus Prime Programmer Standard Edition - [Chain1.cdf]*

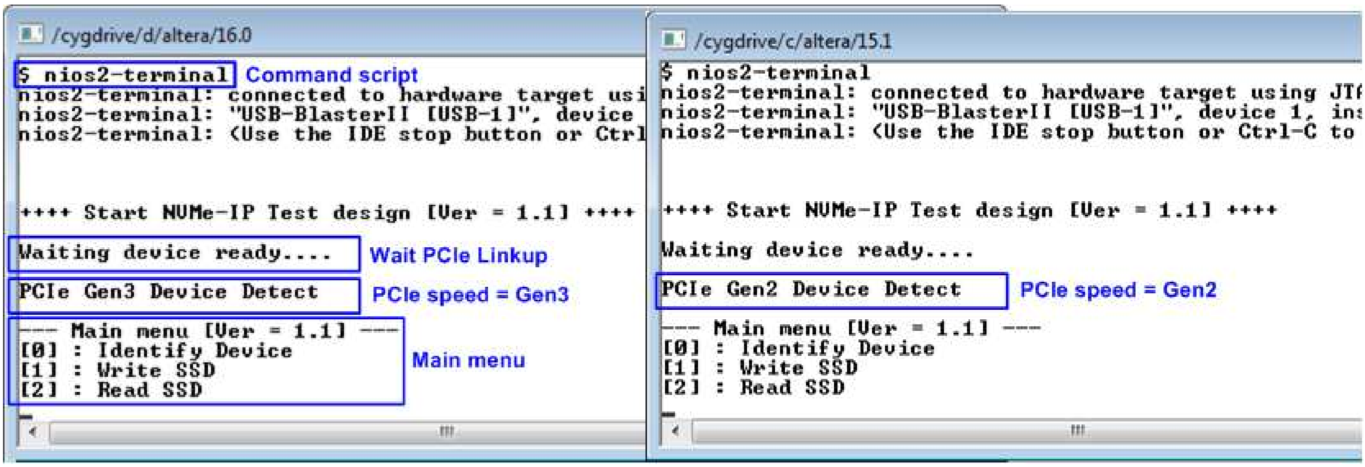
Hardware Setup... USB-BlasterII [USB-1]   Mode: JTAG   Progress: 100% (Successful)

□ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine
D:/nvme/NVMeIPTest.sof	10as066n3f40e2sge2	1D034123	FFFFFFFF	☑	□	□	□
<none>	SOCVHPS	00000000	<none>	□	□	□	□
<none>	5M2210Z	00000000	<none>	□	□	□	□
<none>	5M2210Z	00000000	<none>	□	□	□	□

Figure 2-10 Programmed by QuartusII Programmer

- Open NiosII Command Shell and run nios2-terminal command. Boot message will be displayed.
  “Waiting device ready” message is displayed during system initialization.
  “PCIe Gen3/2/1 Device Detect” shows PCIe speed after PCIe linkup.
  Main menu will be displayed to receive command from user.



/cygdrive/d/altera/16.0

```
$ nios2-terminal
nios2-terminal: connected to hardware target usi
nios2-terminal: "USB-BlasterII [USB-1]", device
nios2-terminal: (Use the IDE stop button or Ctrl


++++ Start NVMe-IP Test design [Ver = 1.1] ++++

Waiting device ready....

PCIe Gen3 Device Detect

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

/cygdrive/c/altera/15.1

```
$ nios2-terminal
nios2-terminal: connected to hardware target using JTA
nios2-terminal: "USB-BlasterII [USB-1]", device 1, ins
nios2-terminal: (Use the IDE stop button or Ctrl-C to


++++ Start NVMe-IP Test design [Ver = 1.1] ++++

Waiting device ready....

PCIe Gen2 Device Detect

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Figure 2-11 NiosII Terminal

- Check LED status on FPGA board. The description of LED is follows.

Table 1 LED Definition

GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1	System is busy	Idle status
2	PCIe Error detect	Normal operation
3	Data verification fail	Normal operation

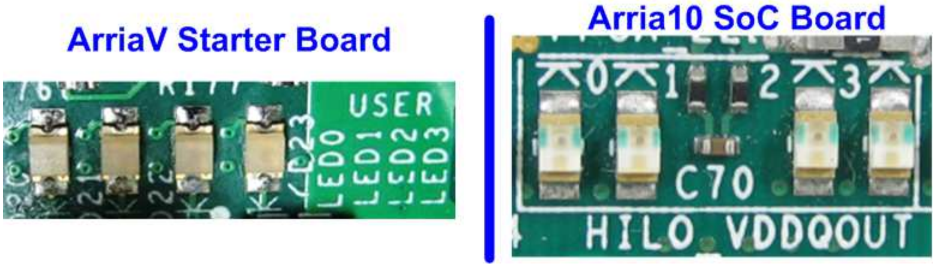


Figure 2-12 4-bit LED Status for user output

- After programming completely, LED[0] and LED[1] will be ON during PCIe initialization process. Then, LED[1] will be OFF to show that PCIe completes initialization process and now system is ready to receive command from user.

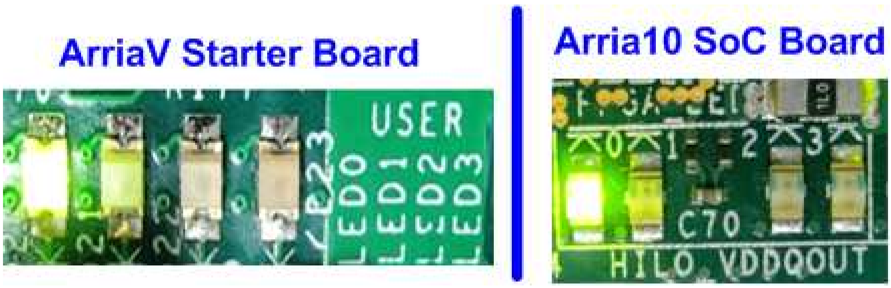
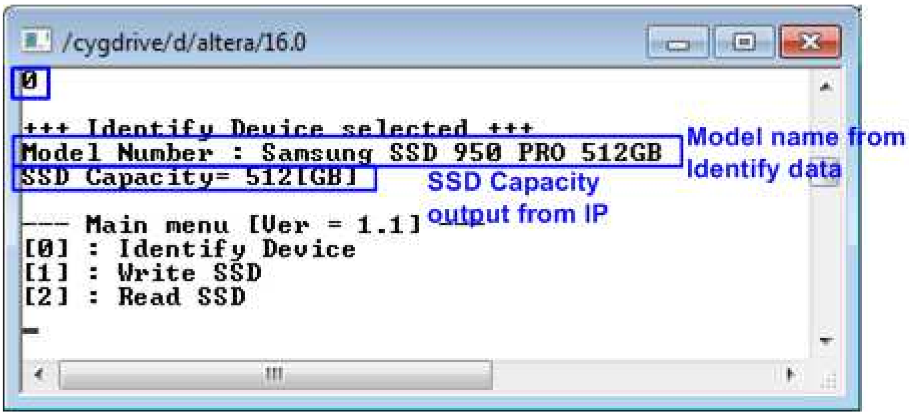


Figure 2-13 LED status after program configuration file and PCIe initialization complete

3 Test Menu

3.1 Identify Device

Select ‘0’ to send Identify device command to NVMe PCIe SSD. When operation is completed, SSD capacity and model name will be displayed on the console.



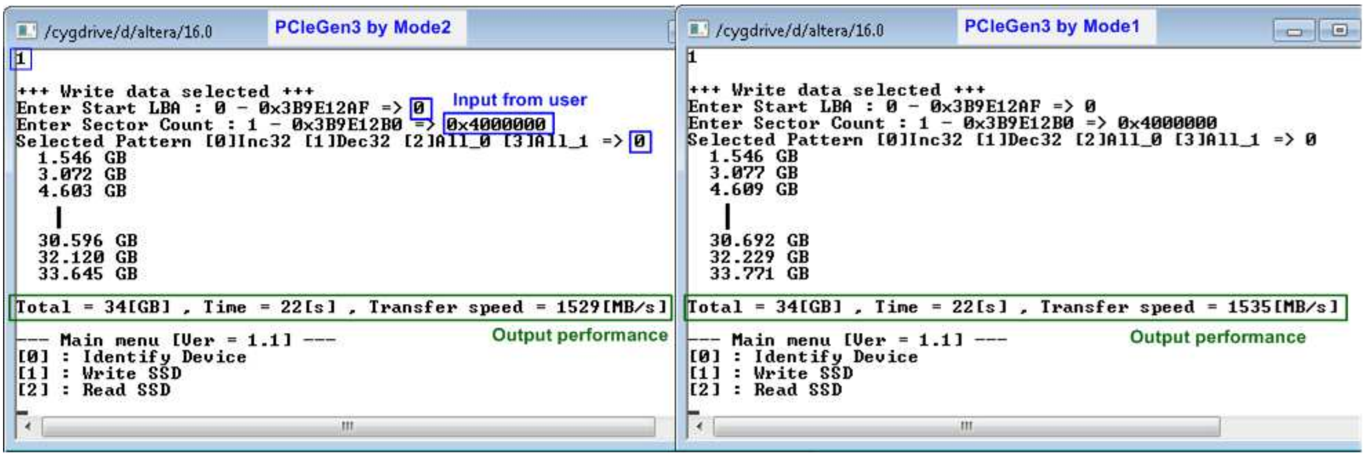
```
0

+++ Identify Device selected +++
Model Number : Samsung SSD 950 PRO 512GB
SSD Capacity= 512[GB]

--- Main menu [Ver = 1.1]
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
_
```

Figure 3-1 Result from Identify Device menu

3.2 Write SSD

Select ‘1’ to send Write command to NVMe PCIe SSD. Three inputs are required for this menu.
1) Start LBA: Input start address of SSD in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
3) Test pattern: Select test pattern of test data for writing to SSD. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

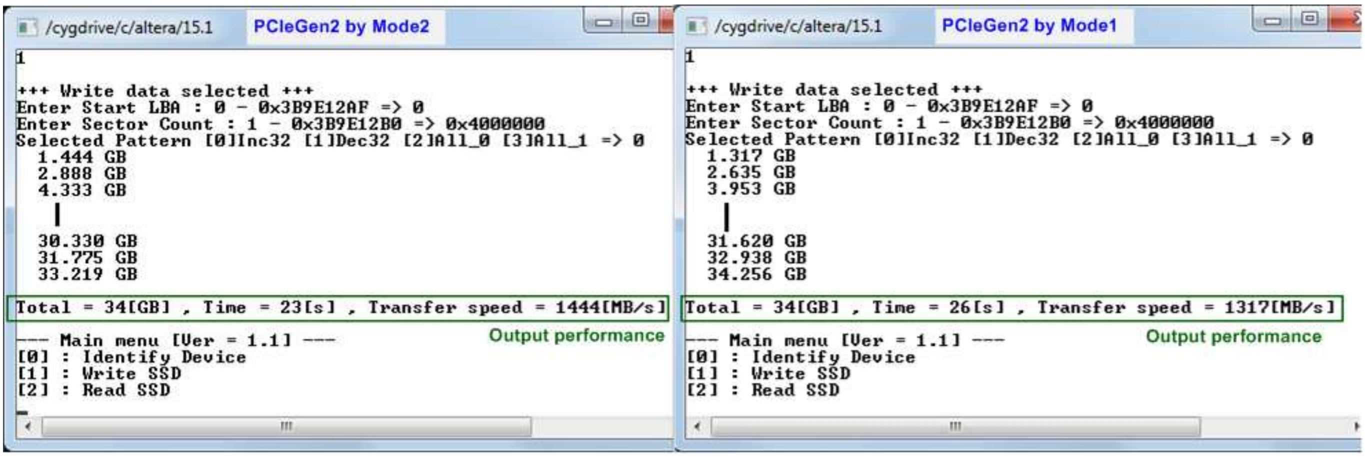
As shown in Figure 3-2 and Figure 3-3, if all inputs are valid, the operation will be started. During writing data, current transfer size will be printed out to the console to show that system still be alive. Finally, test performance with the size and time usage will be displayed on the console.



```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.546 GB
  3.072 GB
  4.603 GB
   |
  30.596 GB
  32.120 GB
  33.645 GB
Total = 34[GB] , Time = 22[s] , Transfer speed = 1529[MB/s]

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.546 GB
  3.077 GB
  4.609 GB
   |
  30.692 GB
  32.229 GB
  33.771 GB
Total = 34[GB] , Time = 22[s] , Transfer speed = 1535[MB/s]

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Figure 3-2 Input and result of Write SSD menu when running on Gen3 speed

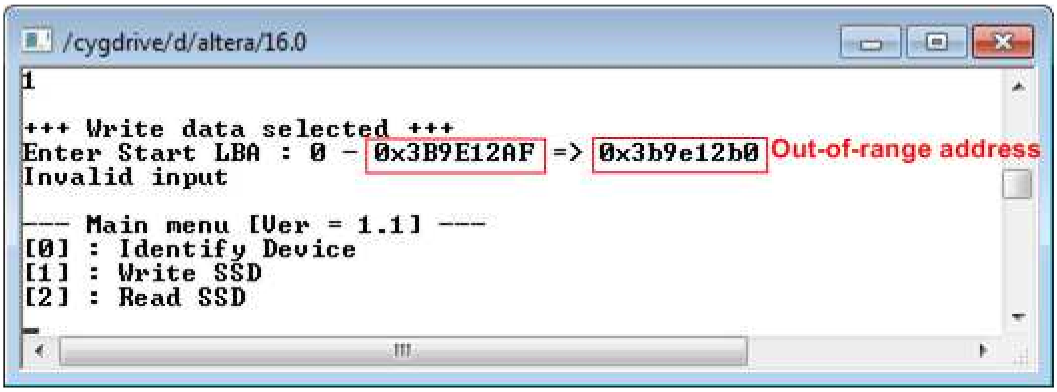


```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.444 GB
  2.888 GB
  4.333 GB
   |
  30.330 GB
  31.775 GB
  33.219 GB
Total = 34[GB] , Time = 23[s] , Transfer speed = 1444[MB/s]

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.317 GB
  2.635 GB
  3.953 GB
   |
  31.620 GB
  32.938 GB
  34.256 GB
Total = 34[GB] , Time = 26[s] , Transfer speed = 1317[MB/s]

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Figure 3-3 Input and result of Write SSD menu when running on Gen2 speed

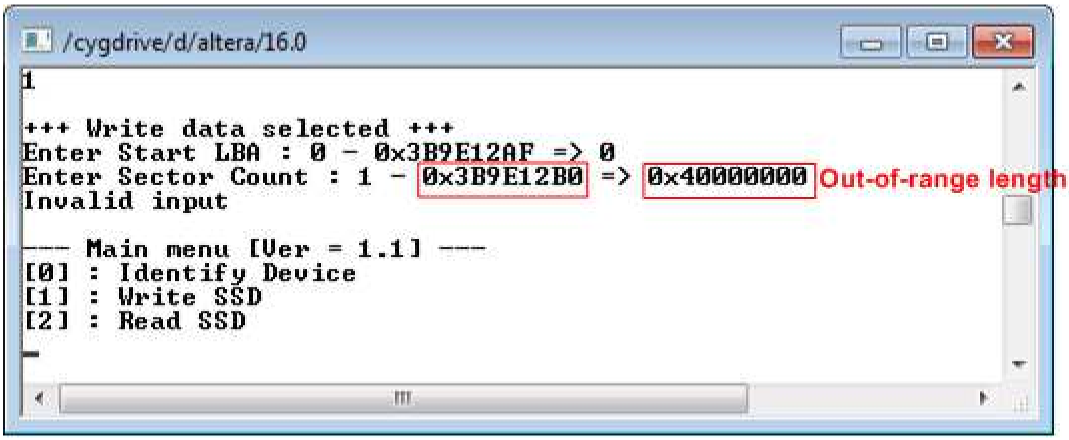
Figure 3-4 – Figure 3-6 shows error message when user input is invalid. “Invalid input” message will be displayed on the console, and then return to main menu to receive new command.



```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0x3b9e12b0
Invalid input

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Out-of-range address

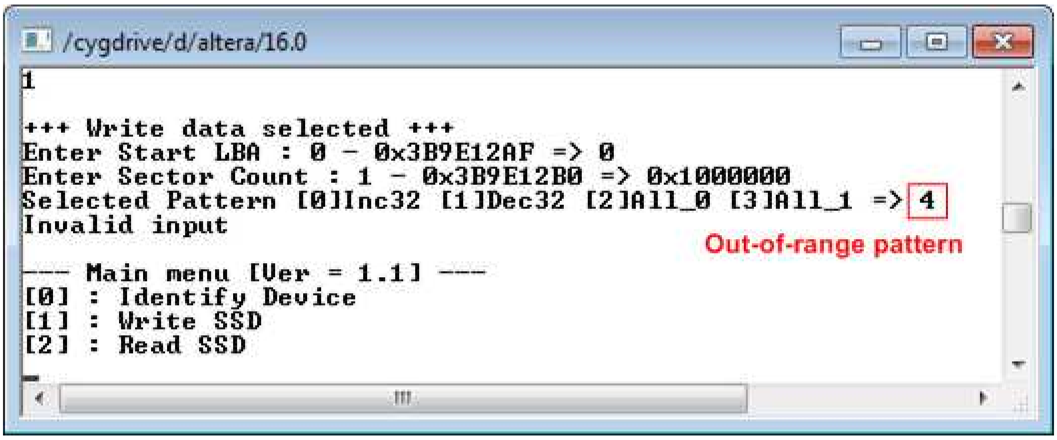
Figure 3-4 Invalid Start LBA input



```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x40000000
Invalid input

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Out-of-range length

Figure 3-5 Invalid Sector count input



```
1

+++ Write data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x1000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 4
Invalid input

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

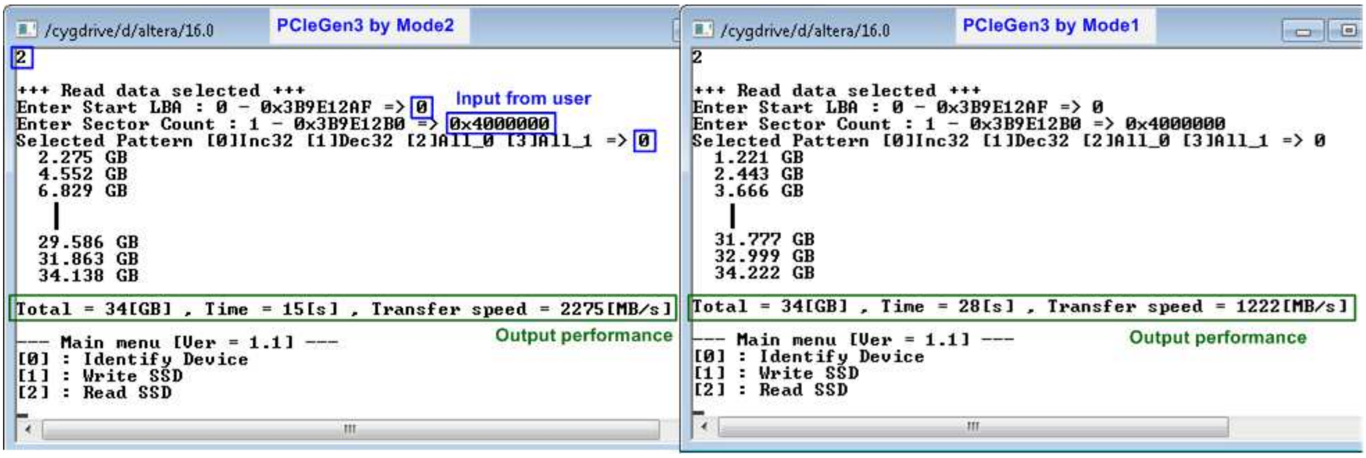
Out-of-range pattern

Figure 3-6 Invalid Test pattern input

3.3 Read SSD

Select ‘2’ to send Read command to NVMe PCIe SSD. Three inputs are required for this menu.
1) Start LBA: Input start address of SSD in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with write test. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

Similar to write test if all inputs are valid, the operation will be started and test performance will be displayed when end of transfer. “Invalid input” will be displayed if any input value is out-of-range.



PCIeGen3 by Mode2

```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  2.275 GB
  4.552 GB
  6.829 GB
   |
  29.586 GB
  31.863 GB
  34.138 GB
Total = 34[GB] , Time = 15[s] , Transfer speed = 2275[MB/s]
--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Input from user

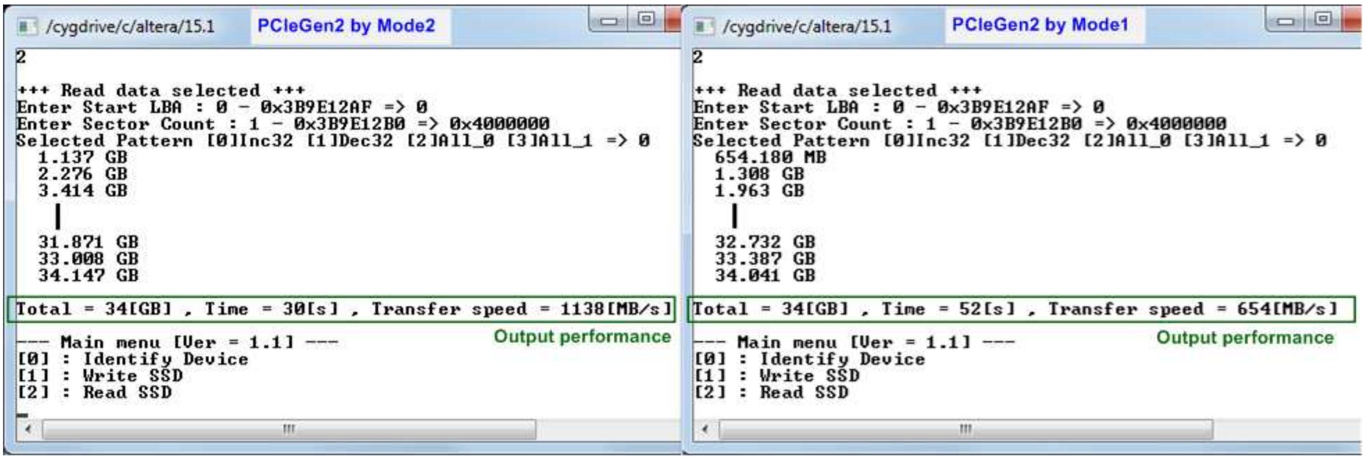
Output performance

PCIeGen3 by Mode1

```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.221 GB
  2.443 GB
  3.666 GB
   |
  31.777 GB
  32.999 GB
  34.222 GB
Total = 34[GB] , Time = 28[s] , Transfer speed = 1222[MB/s]
--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Output performance

Figure 3-7 Input and result of Read SSD menu when running on Gen3 speed



PCIeGen2 by Mode2

```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  1.137 GB
  2.276 GB
  3.414 GB
   |
  31.871 GB
  33.008 GB
  34.147 GB
Total = 34[GB] , Time = 30[s] , Transfer speed = 1138[MB/s]
--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

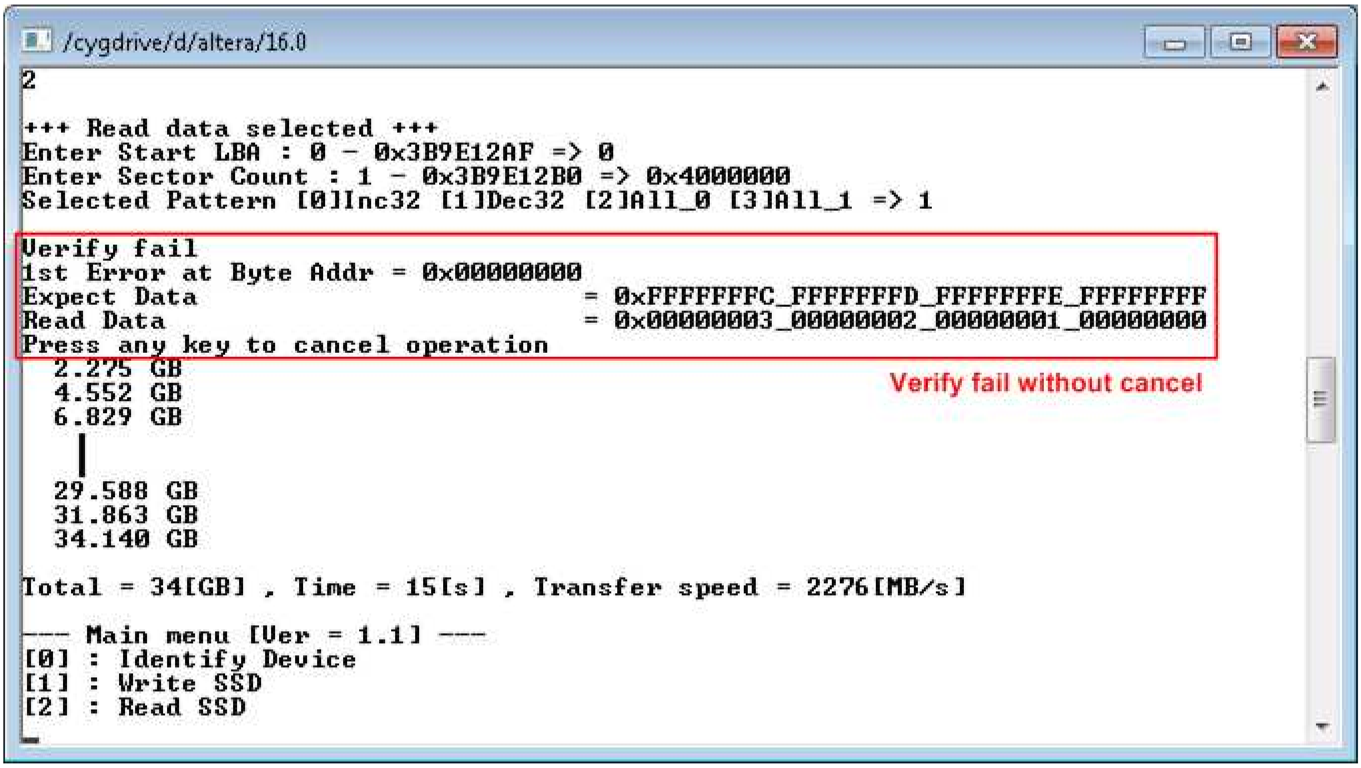
Output performance

PCIeGen2 by Mode1

```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 0
  654.180 MB
  1.308 GB
  1.963 GB
   |
  32.732 GB
  33.387 GB
  34.041 GB
Total = 34[GB] , Time = 52[s] , Transfer speed = 654[MB/s]
--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
```

Output performance

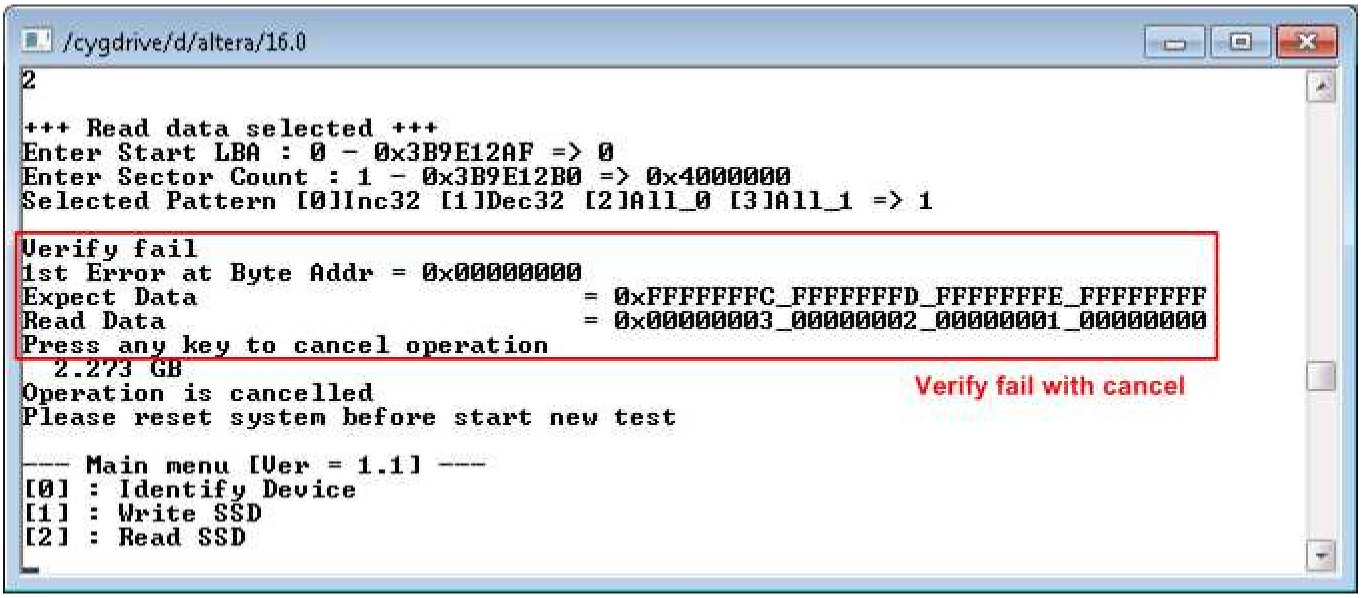
Figure 3-8 Input and result of Read SSD menu when running on Gen2 speed



```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 1

Verify fail
1st Error at Byte Addr = 0x00000000
Expect Data                           = 0xFFFFFFFC_FFFFFFFD_FFFFFFFE_FFFFFFFF
Read Data                             = 0x00000003_00000002_00000001_00000000
Press any key to cancel operation
   2.275 GB
   4.552 GB
   6.829 GB
     |
   29.588 GB
   31.863 GB
   34.140 GB

Total = 34[GB] , Time = 15[s] , Transfer speed = 2276[MB/s]

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
_
```

Verify fail without cancel

Figure 3-9 Data verification is failed, but wait until read complete



```
2

+++ Read data selected +++
Enter Start LBA : 0 - 0x3B9E12AF => 0
Enter Sector Count : 1 - 0x3B9E12B0 => 0x4000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 => 1

Verify fail
1st Error at Byte Addr = 0x00000000
Expect Data                           = 0xFFFFFFFC_FFFFFFFD_FFFFFFFE_FFFFFFFF
Read Data                             = 0x00000003_00000002_00000001_00000000
Press any key to cancel operation
   2.273 GB
Operation is cancelled
Please reset system before start new test

--- Main menu [Ver = 1.1] ---
[0] : Identify Device
[1] : Write SSD
[2] : Read SSD
_
```

Verify fail with cancel

Figure 3-10 Data verification is failed, and press key to cancel operation

Figure 3-9 and Figure 3-10 show the error message when data verification is failed. “Verify fail” message will be displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete. “RESET” button should be pressed to restart the system before starting new test.

4 Revision History

Revision	Date	Description
1.0	9-Aug-16	Initial version release
1.1	17-Aug-16	Update message during write/read command
1.2	19-Dec-16	Update performance result of new buffer system