FPGA set up for NVMeTCP25G-IP

Rev1.0 29-Jun-23

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1 Introduction

This document describes how to setup FPGA board and test environment for running NVMeTCP25G-IP demo. The user can setup the test environment for accessing target NVMe SSD on Test PC across 25Gb Ethernet as shown in Figure 1-1.

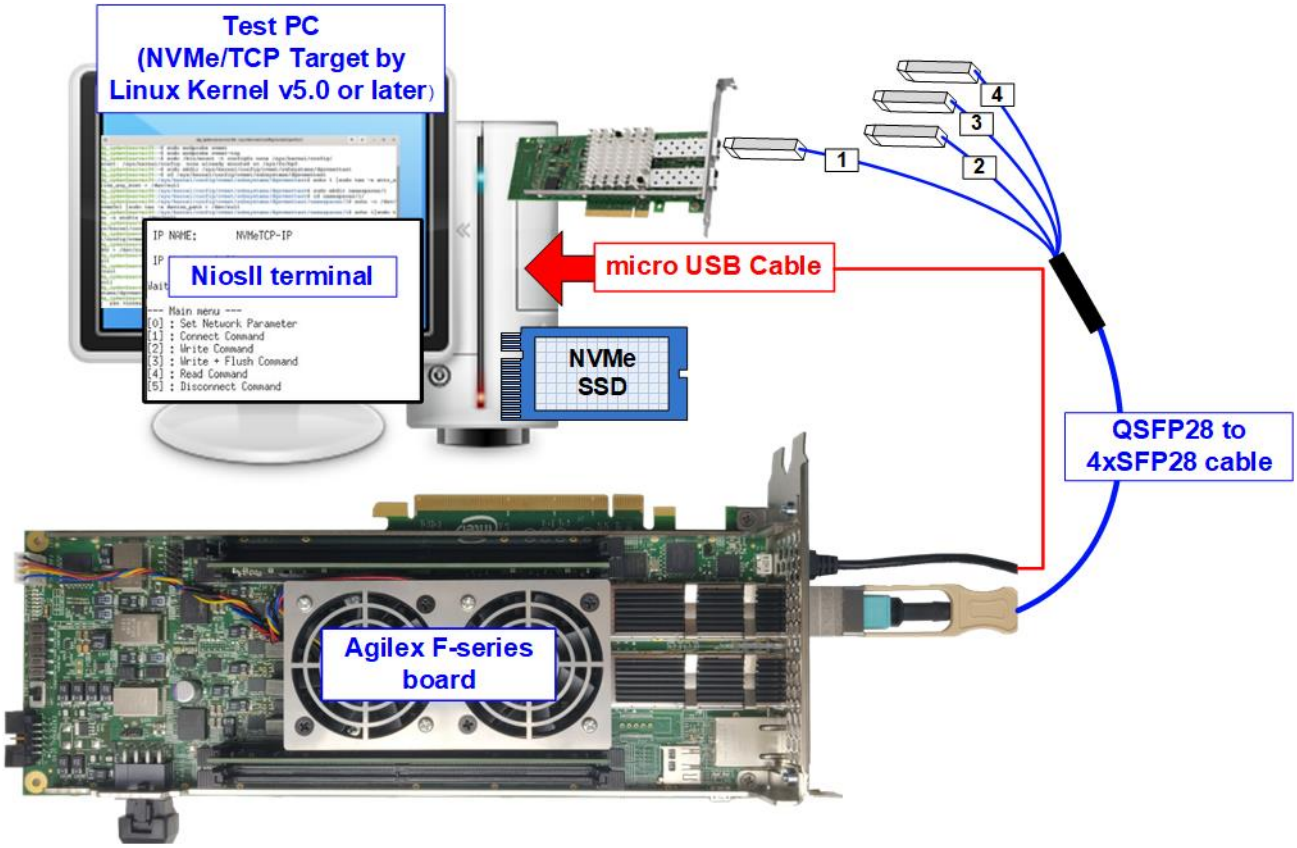

Figure 1-1 Test environment for running the demo

FPGA board runs NVMeTCP25G-IP for the host operation while Test PC integrates 25Gb Ethernet card and one NVMe SSD to be NVMe/TCP target. Test PC installs LinuxOS with the kernel version 5.0 or later to support NVMe/TCP protocol. Also, NiosII terminal is run on Test PC to be user interface console.

Before running the test, please prepare following test environment.

- FPGA development board: Agilex F-Series Development Kit
- Test PC
  i) Installed Linux kernel version 5.0 or later.
  ii) Plug in with one NVMe SSD
  iii) Plug in with 25 Gigabit Ethernet card
- 25 Gb Ethernet cable: QSFP28 to 4xSFP28 cable
- micro USB cable for JTAG connection between FPGA board and PC
- QuartusII Programmer and NiosII command shell, installed on PC

Note: Example hardware for running the demo is listed as follows.
[1] 25G Network Adapter: Nvidia MCX631102AC-ADAT
https://store.nvidia.com/en-us/networking/store/product/MCX631102AC-ADAT/NVIDIAMCX631102ACADATConnectX6LxENAdapterCard25GbECryptoEnabled/
[2] SFP28 to QSFP28 connection
i. QSFP28 Transceiver: AMQ28-SR4-M1
https://www.sfpcables.com/100gb-s-qsfp28-sr4-optical-transceiver-module-1499
ii. SFP28 Transceiver: AZS85-S28-M1
https://www.sfpcables.com/25gb-s-sfp28-sr-transceiver-850nm-up-to-100m-2866
iii. MTP to 4 LC Fiber cable: OM4-MTP-8LC-1M
https://www.fs.com/products/68047.html
[3] Test PC:
Motherboard : Gigabyte Z590 AORUS MASTER (rev. 1.0)
CPU : Intel i7-11700K CPU 3.6 GHz
RAM : 64 GB DDR4
OS : LinuxOS with kernel version 5.4.0-91
[4] Target NVMe SSD: 1 TB WD SN850

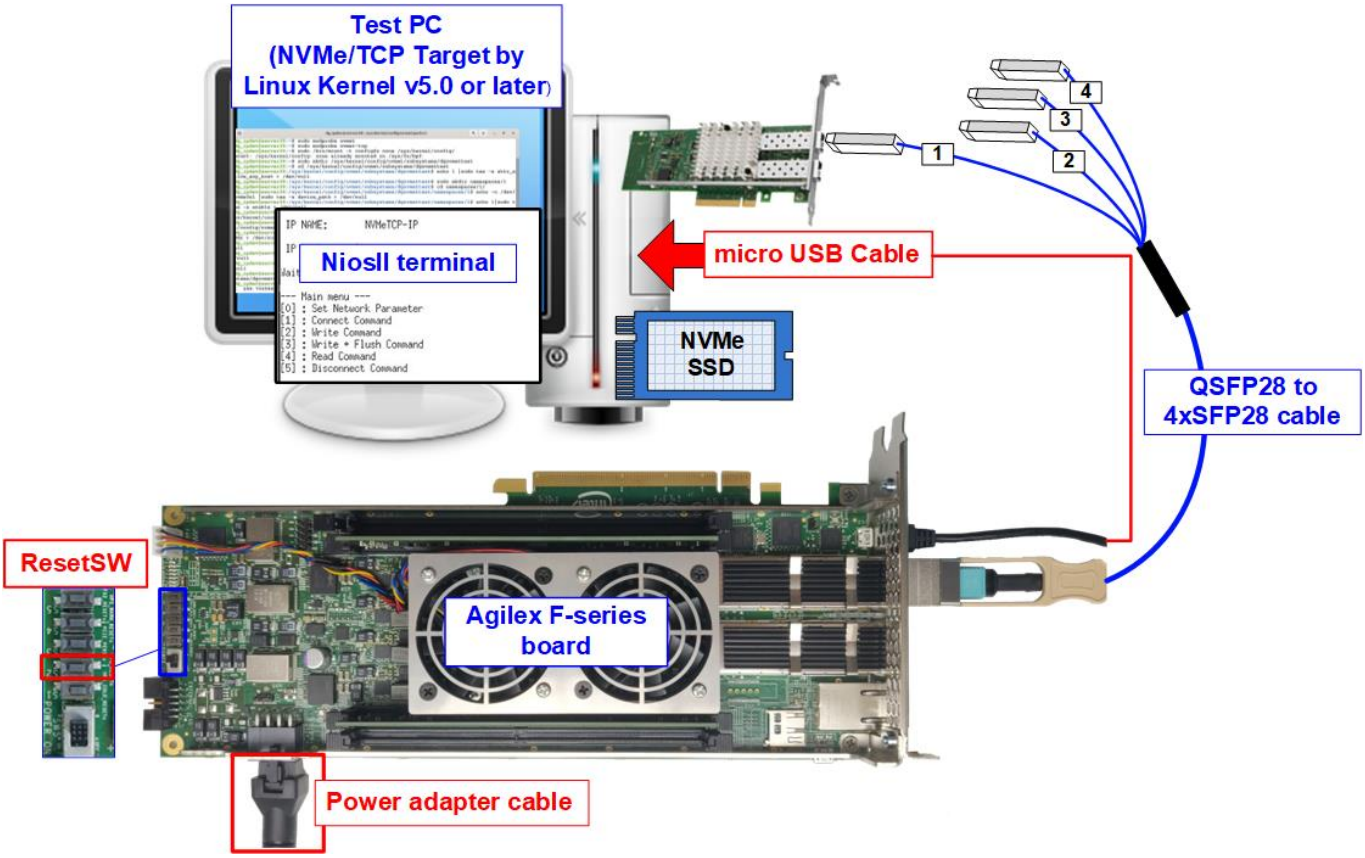

Figure 1-2 NVMeTCP25G-IP demo on Agilex F-Series board

2 Demo setup

This topic describes the details to set up test environment for running the demo.

1) Turn off power switch and connect power supply to FPGA board.
2) Connect micro USB cable from FPGA board to PC for JTAG programming and JTAG UART.

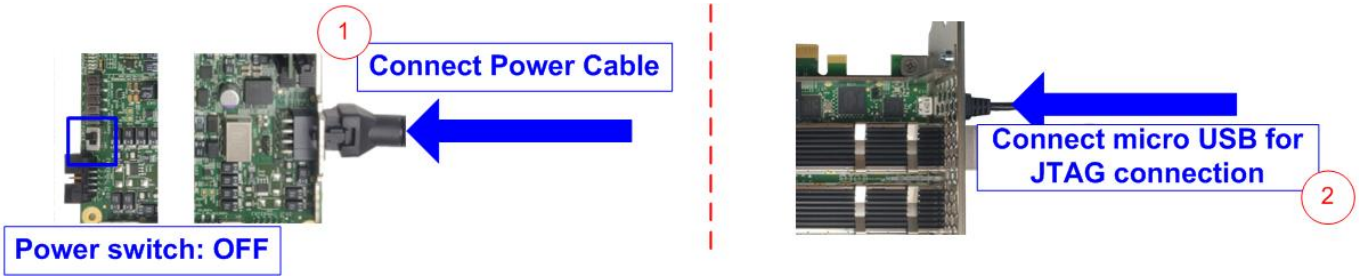

Figure 2-1 Power connection and microUSB connection

3) Connect 25Gb Ethernet cable between FPGA board and PC. Insert QSFP28 to 4xSFP28 cable between FPGA board and PC. Use SFP28 no.1 to connect to QSFP28, as shown in Figure 2-2. On Agilex F-Series board which have two QSFP connectors, use the right connector.

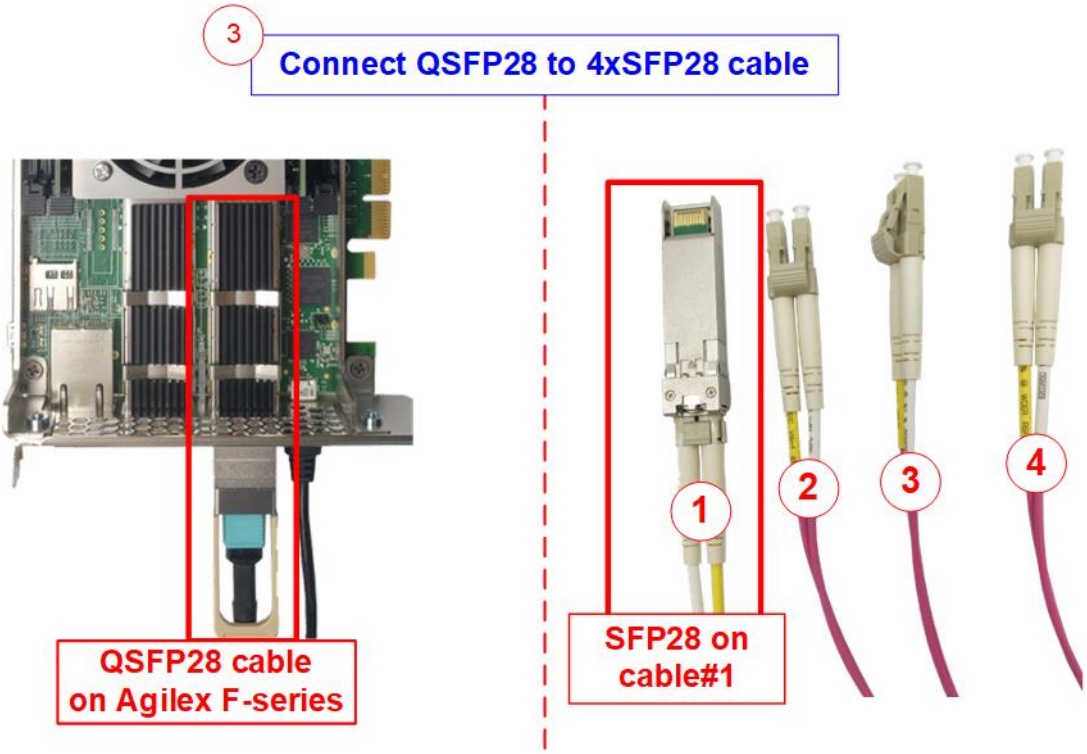

Figure 2-2 25Gb Ethernet connection

4) For Agilex F-series board, please check SW1 which is placed at the bottom side of the board. The setting of bit[1]-[3] must be OFF OFF OFF to configure FPGA by using JTAG only.

Figure 2-3 SW1 setting on Agilex F-series board

5) Turn on power switch on FPGA board.
6) Open QuartusII Programmer to program FPGA through USB-1 by following step.
   i. Click “Hardware Setup…” to select USB-BlasterII[USB-1].
   ii. Click “Auto Detect” and select FPGA number.
   iii. Select FPGA device icon.
   iv. Click “Change File” button, select SOF file in pop-up window, and click “open” button.
   v. Check “program”.
   vi. Click “Start” button to program FPGA.
   vii. Wait until Progress status is equal to 100%.

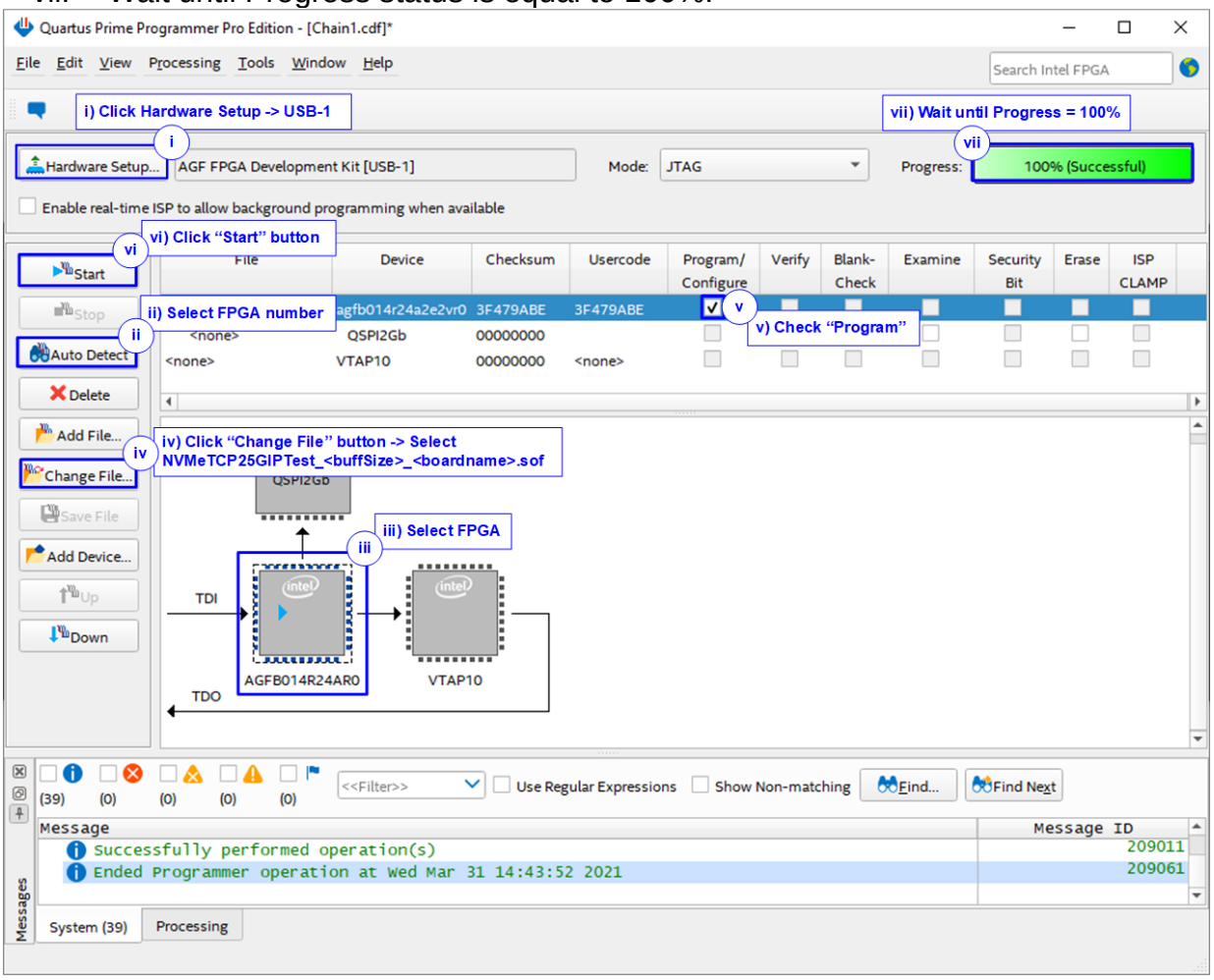

Figure 2-4 FPGA Programmer

7) Open NiosII command shell and type “nios2-terminal” to run the console.

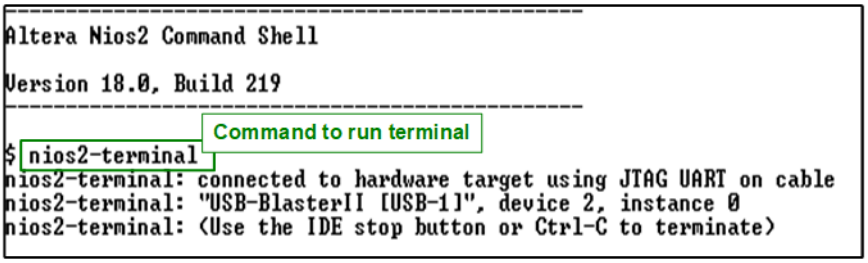

Figure 2-5 Run NiosII terminal

8) After finishing FPGA configuration, welcome message is displayed.

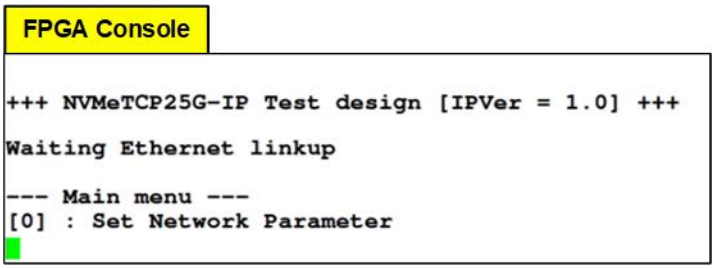

Figure 2-6 Welcome screen

3 Revision History

Revision	Date	Description
1.0	10-Aug-22	Initial version release