

RAID0 Design by using SATA Host-IP Manual

Rev1.1 24-Jan-17

1 Overview

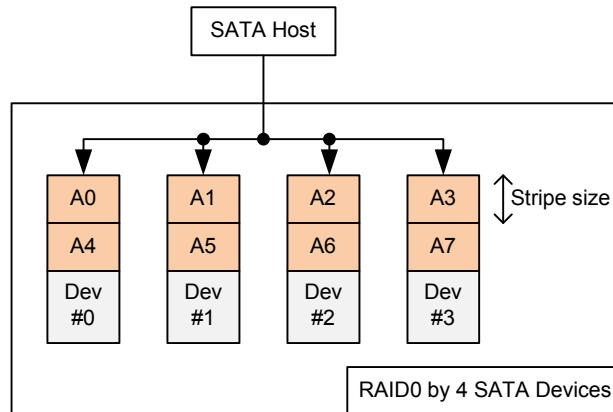


Figure 1 RAID0x4 Data Format

RAID0 system uses multiple storages to extend total storage capacity and increase write/read performance to be N times. Assumed that total number of device is N, data from the host for write command will be split into N stripes, so only one stripe will be stored to one device, as shown in Figure 1. Since minimum transfer size of one SATA device is one sector, the minimum stripe size is equal to 512 byte.

The demo uses 4 SATA devices for RAID0 system and stripe size for one device is equal to one sector. So, total device capacity will be equal to 4 times of one device and the performance will be almost 4 times. Comparing to RAID0 demo implemented by CPU firmware, the overhead time to process each data packet by SATA Host-IP will be less, so total write performance by using SATA Host-IP will be better than using CPU processing.

Note: Write command consists of many packets transferring between the host and the device while read command consists of less packets. So, the overhead from packet processing by CPU not by Host-IP will be much in Write command.

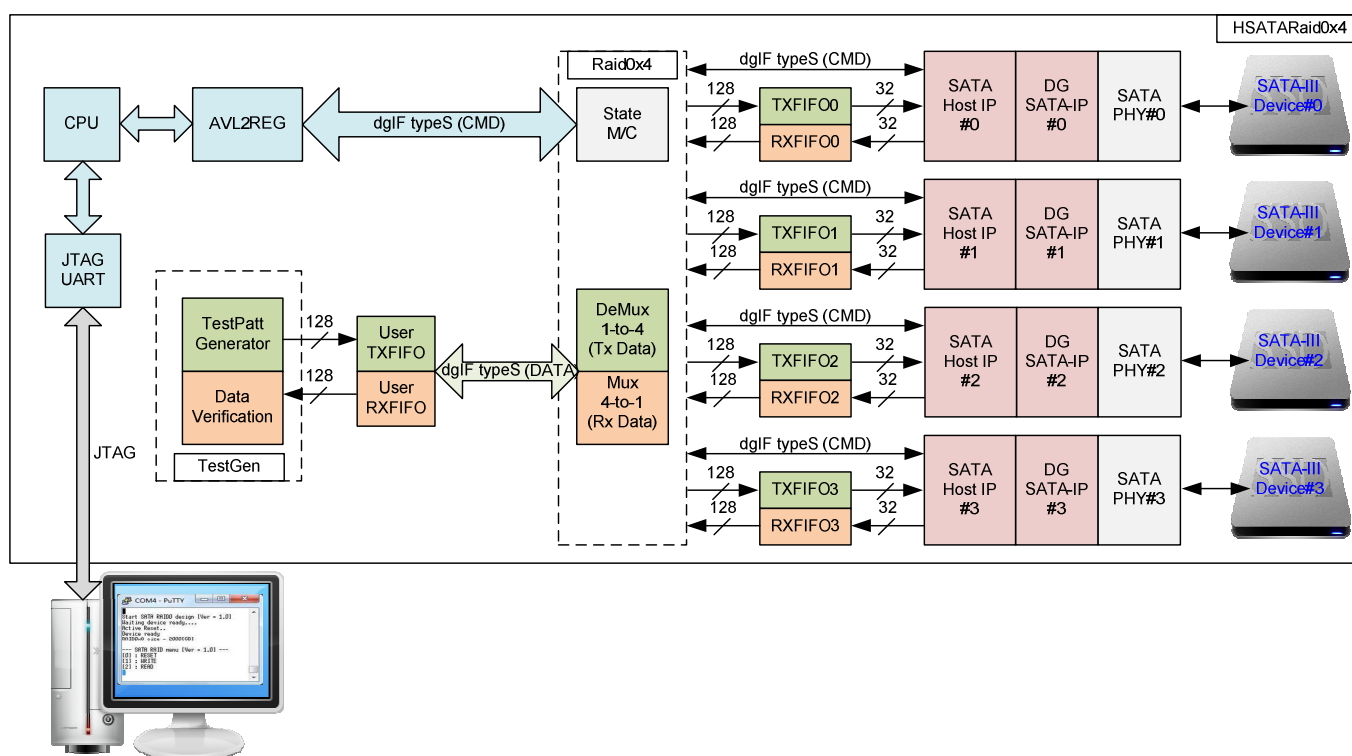


Figure 2 RAID0x4 Demo System by using SATA Host-IP

Comparing to SATA Host-IP demo which runs with one SATA device, the additional part in RAID0 design is Raid0x4 module which is RAID0 controller. To support four-time bandwidth, data bus size of RAID0 will be increased from 32-bit to 128-bit. The interface of Raid0x4 module is designed by using dgIF typeS. Command interface of RAID0x4 module connects with Avl2Reg while data interface connects with User TXFIFO/RXFIFO. UserLogic includes test pattern generator and data verification to test data transfer of RAID0 system.

Before running RAID0 reference design, it is recommended to study SATA Host-IP datasheet and single channel demo firstly from following link.

http://www.dgway.com/products/IP/SATA-IP/Altera/dg_sata_host_ip_datasheet_alt_en.pdf

http://www.dgway.com/products/IP/SATA-IP/Altera/dg_satahostip_refdesign_alt_en.pdf

http://www.dgway.com/products/IP/SATA-IP/Altera/dg_satahostip_instruction_alt_en.pdf

For RAID0 operation, TXFIFO/RXFIFO between Raid0x4 and SATA Host-IP are used to be the buffer and also convert data bus size between 128-bit at Raid0x4 and 32-bit at SATA Host-IP. RAID0 logic design includes state machine for controlling the control and data signals sequence of each SATA channel. To forward data from UserLogic to four SATA Host-IPs, 4-to-1 demux is used to select active SATA Host-IP for the source. To forward data from four SATA Host-IPs to UserLogic, 4-to-1 mux is used to select active SATA Host-IP for UserLogic.

Similar to SATA Host-IP single channel demo, TestGen is designed to generate or verify data. CPU system is designed to interface with user through Serial console, so user ser can set test parameter easily.

2 RAID0x4

Table 1 shows user interface of RAID0 module for both control and data interface. The control signals are designed by using dgIF typeS format. But the different signals from SATA Host-IP are lden port and data bus size.

- lden port is extended from one set to be four sets to map each SATA Host-IP directly.
- Data bus size of FIFO port is extended from 32-bit to be 128-bit.

2.1 Port Description

Table 1 Signal Description of Raid block (only user interface)

Signal	Dir	Description
User Interface		
RstB	In	Reset signal. Active low. Please use same reset signal as SATA Host-IP.
Clk	In	User clock. Must use the same clock as SATA Host-IP.
dgIF typeS		
UserCmd[1:0]	In	User Command. "00": Identify device command, "01": Security erase "10": Write SATA device, "11": Read SATA device.
UserAddr[47:0]	In	Start address of SATA device to write/read in sector unit (512 byte).
UserLen[47:0]	In	Total transfer size in the request. Must not set equal to 0. Note: UserAddr + UserLen must be not more than LBASize value.
UserReq	In	Request the new command. Can be asserted only when the IP is Idle (UserBusy='0'). Asserted with valid value on UserCmd/UserAddr/UserLen signals.
UserBusy	Out	IP Busy status. New request is not allowed if this signal is asserted to '1'.
LBASize[47:0]	Out	Total device capacity in sector unit (512 byte). Default value is 0. This value is equal to four times of LBASize value output from IP#0.
UserError	Out	Error flag. Assert when UserErrorType is not equal to 0. The flag can be reset only by asserting RstB signal.
UserErrorType[31:0]	Out	Error status which are mapped from status in each SATA Host-IP. [7:0] – Mapped from UserErrorType[7:0] of IP#0. [15:8] – Mapped from UserErrorType[7:0] of IP#1. [23:16] – Mapped from UserErrorType[7:0] of IP#2. [31:24] – Mapped from UserErrorType[7:0] of IP#3.
UserFifoWrCnt[15:0]	In	Write data counter of User received FIFO. Used to check FIFO space size. If total size is less than 16-bit, please fill '1' to upper bit. UserFifoWrEn can be asserted when UserFifoWrCnt[15:6] is not equal to all 1.
UserFifoWrEn	Out	Write data valid of User received FIFO
UserFifoWrData[127:0]	Out	Write data bus of User received FIFO. Synchronous to UserFifoWrEn.
UserFifoRdCnt[15:0]	In	Read data counter of User transmit FIFO. Used to check data available size in FIFO. If total FIFO size is less than 16-bit, please fill '0' to upper bit. UserFifoRdEn can be asserted when UserFifoRdCnt[15:5] is not equal to 0.
UserFifoEmpty	In	FIFO empty flag of User transmit FIFO. This signal is unused in the design.
UserFifoRdEn	Out	Read valid of User transmit FIFO
UserFifoRdData[127:0]	In	Read data returned from User transmit FIFO. Valid after UserFifoRdEn asserted about one clock period.

Signal	Dir	Description
Other Interface		
TestPin[0-3][31:0]	Out	Direct mapped from TestPin in each SATA Host-IP. [0]-IP#0, [1]-IP#1, [2]-IP#2, [3]-IP#3.
TimeOutSet[31:0]	Out	Timeout value of all SATA Host-IPs. Time unit is following Clk frequency value.
TrnLinkup[3:0]	Out	Linkup signal from trn_link_up in each SATA-IP. Bit[0]-IP#0, [1]-IP#1, [2]-IP#2, [3]-IP#3.
IdenWrAddr[0-3][6:0]	Out	Direct mapped from IdenWrAddr in each SATA Host- IP. [0]-IP#0, [1]-IP#1, [2]-IP#2, [3]-IP#3.
IdenWrEn[3:0]	Out	Direct mapped from IdenWrEn in each SATA Host- IP. [0]-IP#0, [1]-IP#1, [2]-IP#2, [3]-IP#3.
IdenWrData[0-3][31:0]	Out	Direct mapped from IdenWrData in each SATA Host- IP. [0]-IP#0, [1]-IP#1, [2]-IP#2, [3]-IP#3.

2.2 Timing Diagram

Timing diagram of RAID user interface and Identify device interface are similar to SATA Host-IP, so user can check more details from IP datasheet. For RAID FIFO interface, the details are described as follows.

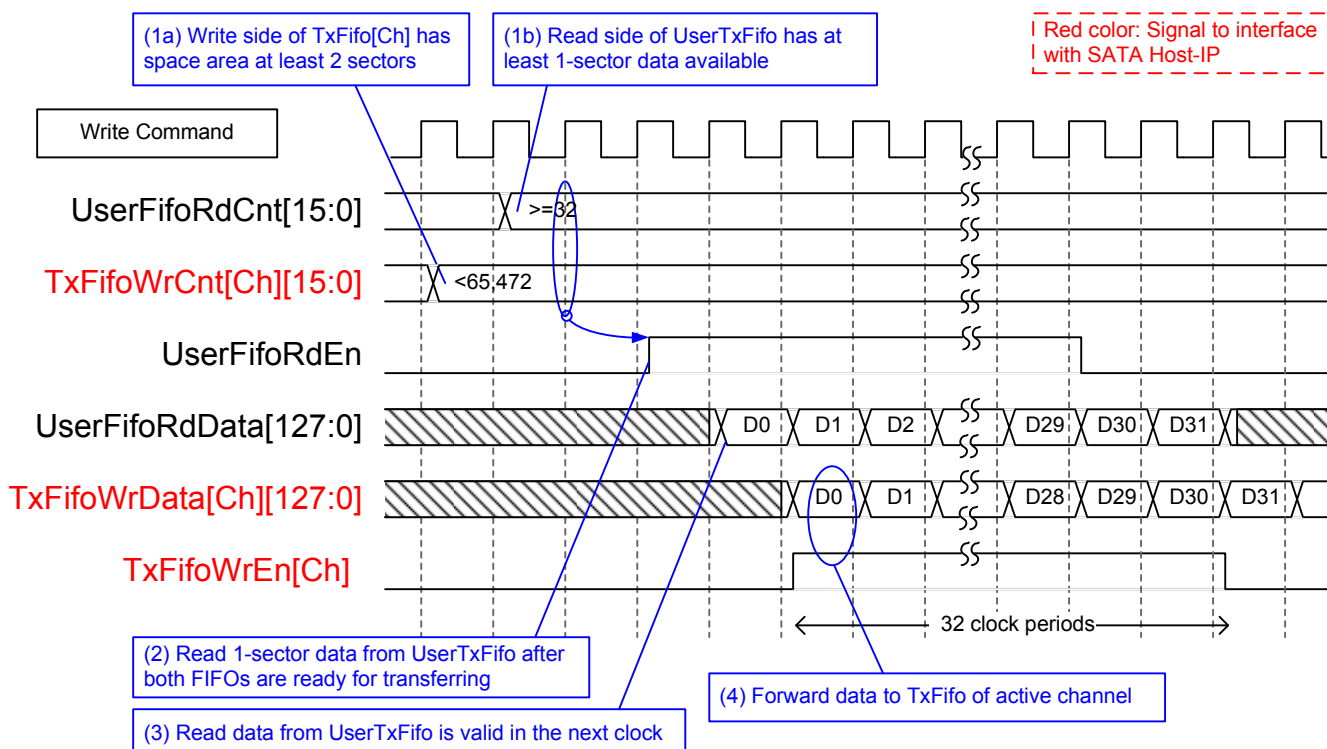


Figure 3 RAID FIFO Timing Diagram of Write Command

When user sends write command to RAID system, data will be forwarded from UserTxFifo to TxFifo[0]-[3]. Only one TxFifo will be active to transfer one sector data and the active SATA channel will be switched for next sector transfer following RAID0 behavior. Before forwarding data, UserFifoRdCnt and TxFifoWrCnt of active channel are monitored to confirm that at least 1 sector data is available in UserTxFifo and at least 2-sector space area is available in TxFifo of active channel. UserFifoRdEn will be asserted for 32 clock periods to transfer 512-byte data.

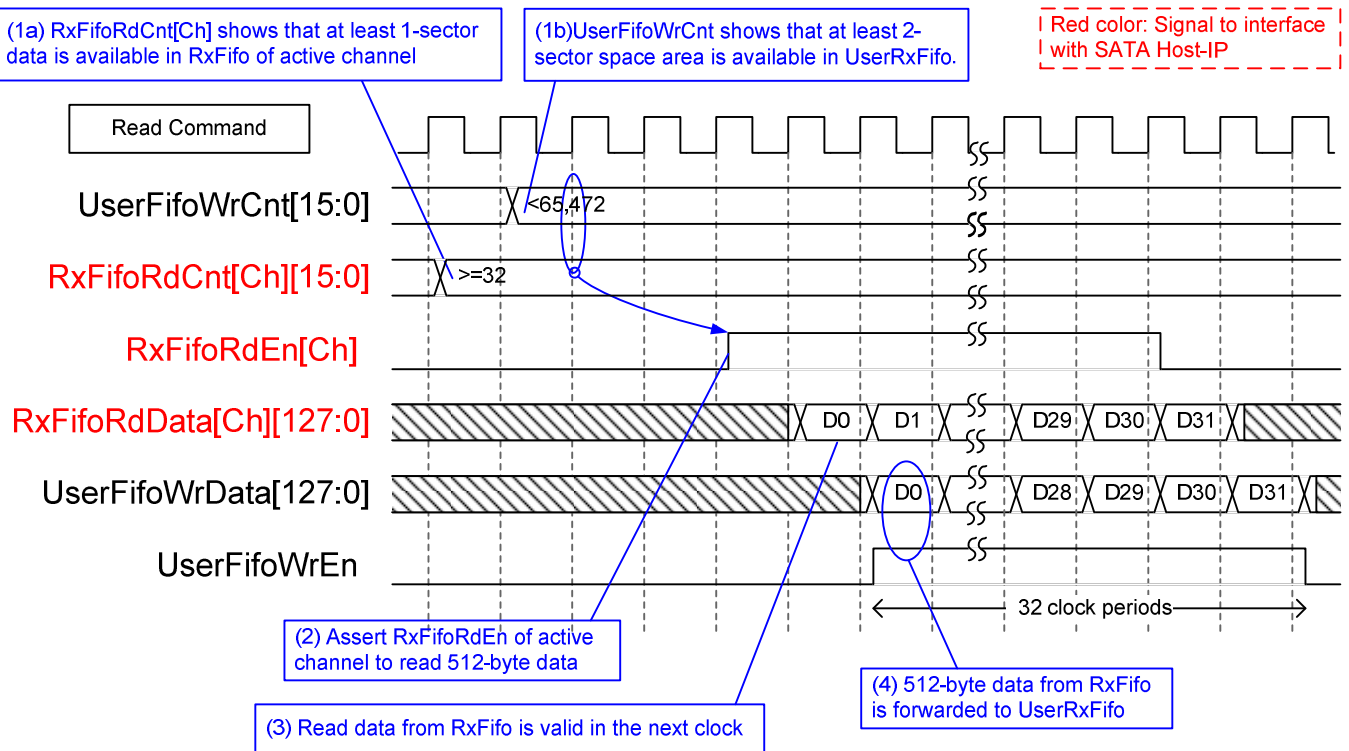


Figure 4 RAID FIFO Timing Diagram of Read Command

When user sends read command to RAID system, data will be forwarded from RxFifo[0]-[3] to UserRxFifo, as shown in Figure 4. Similar to write command, only one RxFifo will be active for each 512-byte transfer and active SATA channel will be switched for next sector transfer. Before forwarding data, UserFifoWrCnt and RxFifoRdCnt of active channel are monitored to confirm that at least 1 sector data is available in RxFifo of active channel and at least 2-sector space area is available in UserRxFifo. UserFifoWrEn will be asserted for 32 clock periods to transfer 512-byte data.

3 CPU

CPU system in RAID0 design is similar to SATA Host-IP single channel demo, but register map for expected pattern and read pattern are extended from 32-bit to 128-bit, as shown in Table 2

Table 2 Register Map

Address Rd/Wr	Register Name (Label in the "hsataraidtest.c")	Description
BA+0x00 Wr	User Address (Low) Reg (USRADRL_REG)	[31:0]: Input to be start sector address (UserAddr[31:0] of dgIF typeS for RAID0)
BA+0x04 Wr	User Address (High) Reg (USRADRH_REG)	[15:0]: Input to be start sector address (UserAddr[47:32] of dgIF typeS for RAID0)
BA+0x08 Wr	User Length (Low) Reg (USRLENL_REG)	[31:0]: Input to be transfer length in sector unit (UserLen[31:0] of dgIF typeS for RAID0)
BA+0x0C Wr	User Length (High) Reg (USRLENH_REG)	[15:0]: Input to be transfer length in sector unit (UserLen[47:32] of dgIF typeS for RAID0)
BA+0x10 Wr	User Command Reg (USRCMD_REG)	[1:0]: Input to be user command (UserCmd f of dgIF typeS for RAID0) "00"-Identify device, "01"-Security erase, "10"-Write SSD, "11"-Read SSD, When this register is written, the design will generate command request to RAID0 to start new command operation.
BA+0x14 Wr	Test Pattern Reg (PATTSEL_REG)	[1:0]: Test pattern select "00"-Increment, "01"-Decrement, "10"-All 0, "11"-All 1
BA+0x100 Rd	User Status Reg (USRSTS_REG)	[0]: UserBusy of dgIF typeS for RAID0 ('0': Idle, '1': Busy) [1]: UserError of dgIF typeS for RAID0 ('0': Normal, '1': Error) [2]: Data verification fail ('0': Normal, '1': Error) [4:3]: SATA speed from IP "00": No linkup, "11": SATA Gen3, "01"/"10": Not supported
BA+0x104 Rd	Total device size (Low) Reg (LBASIZEL_REG)	[31:0]: Total capacity of RAID0 in sector unit (LBASize[31:0] of dgIF typeS for RAID0)
BA+0x108 Rd	Total device size (High) Reg (LBASIZEH_REG)	[15:0]: Total capacity of RAID0 in sector unit (LBASize[47:32] of dgIF typeS for RAID0)
BA+0x10C Rd	User Error Type Reg (USRERRTYPE_REG)	[31:0]: User error status (UserErrorType[31:0] of dgIF typeS for RAID0)
BA+0x120 Rd	Data Failure Address (Low) Reg (RDFAILNOL_REG)	[31:0]: Latch value of failure address[31:0] in byte unit from read command
BA+0x124 Rd	Data Failure Address (High) Reg (RDFAILNOH_REG)	[24:0]: Latch value of failure address [56:32] in byte unit from read command
BA+0x130 Rd	Expected value Word0 Reg (EXPPATW0_REG)	[31:0]: Latch value of expected data [31:0] from read command
BA+0x134 Rd	Expected value Word1 Reg (EXPPATW1_REG)	[31:0]: Latch value of expected data [63:32] from read command
BA+0x138 Rd	Expected value Word2 Reg (EXPPATW2_REG)	[31:0]: Latch value of expected data [95:64] from read command
BA+0x13C Rd	Expected value Word3 Reg (EXPPATW3_REG)	[31:0]: Latch value of expected data [127:96] from read command
BA+0x140 Rd	Read value Word0 Reg (RDPATW0_REG)	[31:0]: Latch value of read data [31:0] from read command
BA+0x144 Rd	Read value Word1 Reg (RDPATW1_REG)	[31:0]: Latch value of read data [63:32] from read command
BA+0x148 Rd	Read value Word2 Reg (RDPATW2_REG)	[31:0]: Latch value of read data [95:64] from read command
BA+0x14C Rd	Read value Word3 Reg (RDPATW3_REG)	[31:0]: Latch value of read data [127:96] from read command

Address Rd/Wr	Register Name (Label in the "hsataiptest.c")	Description
BA+0x150 Rd	Current test byte (Low) Reg (CURTESTSIZEL_REG)	[31:0]: Current test data size of TestGen module in byte unit (bit[31:0])
BA+0x154 Rd	Current test byte (High) Reg (CURTESTSIZEH_REG)	[24:0]: Current test data size of TestGen module in byte unit (bit[56:32])
BA+0x2000 – 0x21FF	Identify Device Command Data (IDENCTRL_REG)	512-byte Identify Device Data from SATA CH#0
BA+0x2200 – 0x23FF		512-byte Identify Device Data from SATA CH#1
BA+0x2400 – 0x25FF		512-byte Identify Device Data from SATA CH#2
BA+0x2600 – 0x27FF		512-byte Identify Device Data from SATA CH#3

4 TestGen

Comparing to SATA Host-IP single channel demo, data bus of test pattern is extended from 32-bit to 128-bit, as shown in Figure 5.

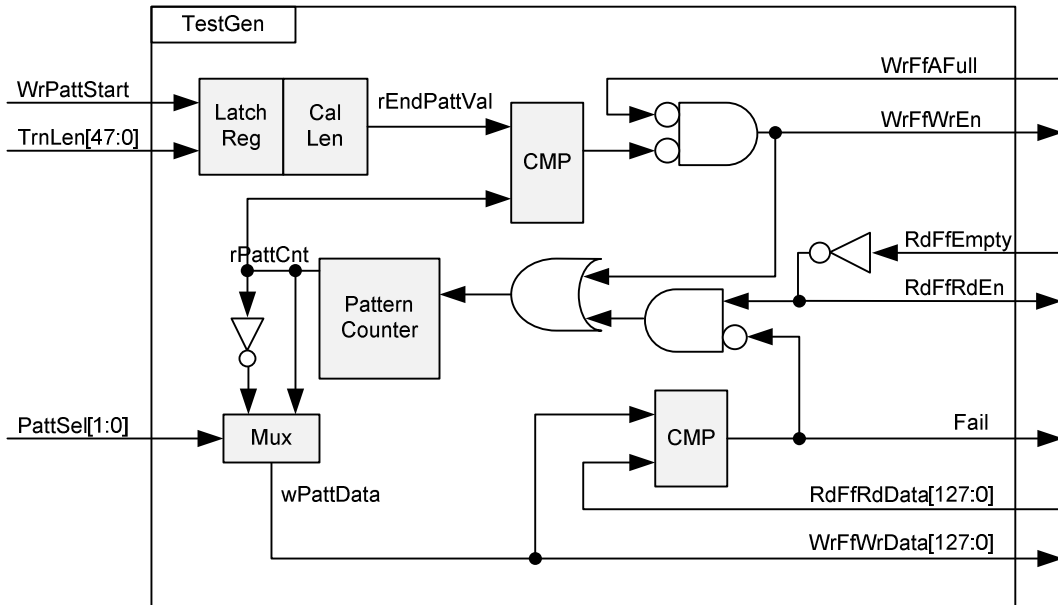


Figure 5 Logic design in TestGen

5 Revision History

Revision	Date	Description
1.0	24-Nov-16	Initial version release
1.1	24-Jan-17	Update signal to dglF typeS

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