8-ch RAID0 by SATA Host-IP Demo Instruction

Rev1.1 24-Jun-15

This document describes the instruction to run 8-ch RAID0, designed by using SATA Host-IP, on Altera development board with HSMCRAID board. The demo is designed to write and verify test data with 8 SATA-III devices. User can select test pattern, test speed, and test data size by using DIPSW. User can start write or verify data by press push-button switch.

1 Environment Setup

To demo 8-ch SATA Host RAID0 on Altera development board, please prepare following hardware.

1) Supported FPGA Development board (StratixV board)
2) QuartusII programmer
3) "Clock Control" Test application for FPGA board, provided by Altera
4) 2xAB12-HSMCRAID board, connecting with Power cable at power connector and eight SATA-III devices at CN0–CN2@PortA, CN4-CN6@PortA, and CN0-CN1@PortB
5) micro USB cable for programming FPGA between FPGA Development board and PC

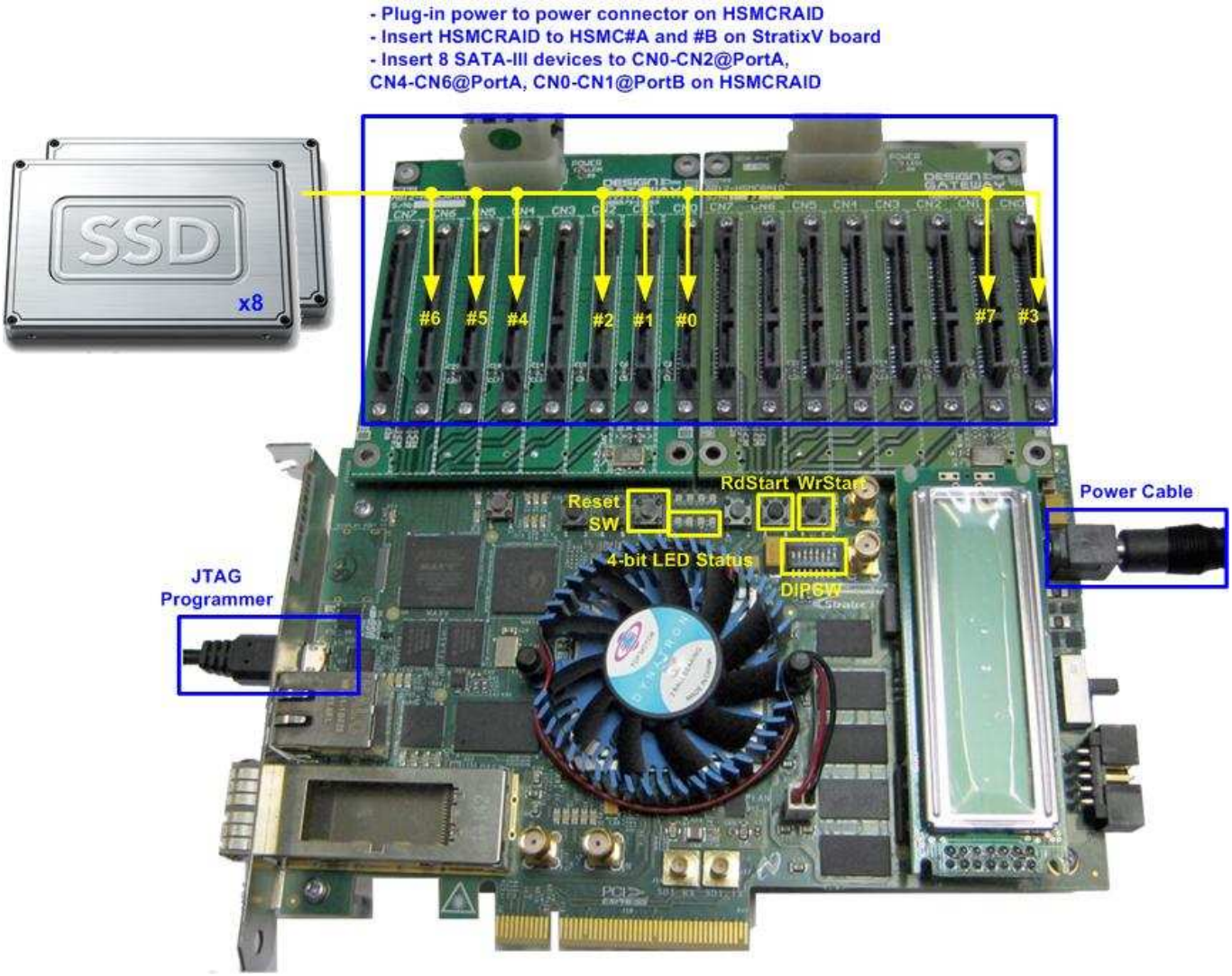

Figure 1 8-ch SATA Host RAID0 Demo Environment Setup on StratixV board

2 Demo description

User inputs in the demo are 6-bit of DIPSW, PB0 SW, and PB1 SW which are available on Altera development boards.

6-bit DIPSW is used for selecting test pattern, test speed, and test size for write/read test. All DIPSWs can be changed before pressing PB0/1 SW. DIPSW definition is shown in Table 1 – Table 3.

- PB0 SW: Press to start write test data to all SATA devices
- PB1 SW: Press to start read and verify test data from all SATA devices

Both write and read test transfer data starting from address=0.

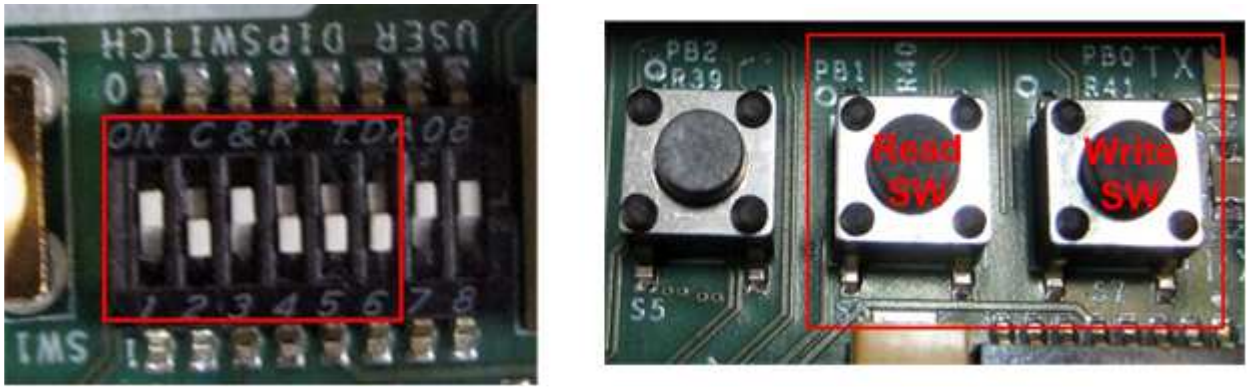

Figure 2 User input

Table 1 DIPSW Setting Definition

DIPSW	ON (Logic='0')	OFF (Logic = '1')
Bit 1	32-bit increment test pattern	32-bit decrement test pattern
Bit [4:2]	Select Test size (See more details in Table 2)	
Bit [6:5]	Select Test speed (See more details in Table 3)	

Table 2 DIPSW[4:2] Setting Definition

Bit4	Bit3	Bit2	Test Size
ON	ON	ON	128 Gbytes
ON	ON	OFF	256 Gbytes
ON	OFF	ON	512 Gbytes
ON	OFF	OFF	1024 Gbytes
OFF	ON	ON	2048 Gbytes
OFF	ON	OFF	4096 Gbytes
OFF	OFF	ON	8192 Gbytes
OFF	OFF	OFF	32 Tbytes

Table 3 DIPSW[6:5] Setting Definition

Bit6	Bit5	Test Speed
ON	ON	2400 Mbyte/sec
ON	OFF	2800 Mbyte/sec
OFF	ON	3200 Mbyte/sec
OFF	OFF	3600 Mbyte/sec

For user output, 4-bit LED is used to show current test status. SATA device detection and current process running of test demo are monitored by LED.

Table 4 LED Definition

USER LED	ON	OFF	BLINK
0	DDR3 Error	DDR3 and SATA LINKUP	Some SATA channel cannot detect
1	User module busy	User module Idle	Data verification error
2	N/A	N/A	Buffer overflow, underflow, or not empty when end of transfer
3	RAID0 busy (write, read, or initialize)	RAID0 Idle	Error from RAID0

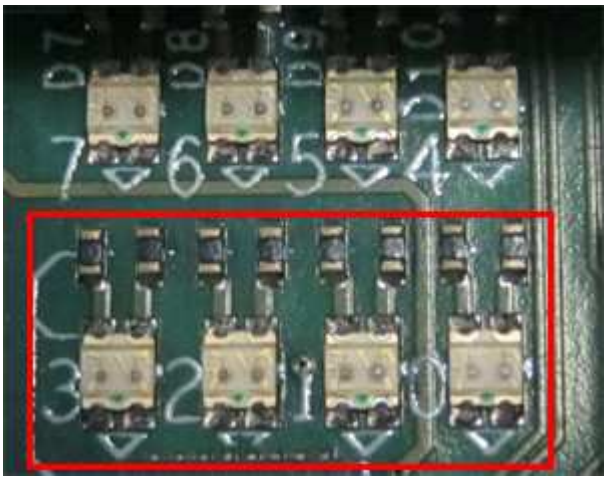

Figure 3 4-bit LED Status for user output

Refer to test sequence, LED status will be shown as follows.

1) DDR3 controller initialize completed. (LED[0] not ON).
2) SATAPHY detects all SATA-III devices. LED[0] will change status from BLINK to be OFF.
3) All SATA Host-Ips send IDENTIFY DEVICE command to check disk capacity. After receiving the status from all SATA devices, RAID0 controller changes busy status to idle. So, LED[3] will change status from ON to OFF.
4) When press WrStart, test data will be written to RAID0. Test pattern, size, and speed are selected by 6-bit DIPSW.
   - During write process, LED[1] and LED[3] will be ON and OFF when end of operation.
   - LED[1] will be blinked if data verification is failed. In this case, please check test pattern, and test size selection which should be matched with the previous write transfer.
   - LED[2] will be blinked during write/read operation, if the buffer is overflow/underflow. In this case, user should reduce test speed setting. The error can be cleared by RESET SW only.
   - LED[3] will be blinked if RAID0 is error. In this case, SATA-IP detects error from SATA device. The error can be cleared by RESET SW only.

LED4 – LED7 are used to be test point to check system performance. 4-bit LED is used to show current test status. SATA device detection and current process running of test demo are monitored by LED.

Table 5 LED Definition

USER LED	Signal Name (All are active low)	ON	OFF
4	UserBusy	UserModule is operating	UserModule is idle
5	RaidBusy	Raid0 is operating	Raid0 is idle
6	RaidTxFfRdEn	Read enable to RaidTxFf	Idle
7	RaidRxFfWrEn	Write enable RaidRxFf	Idle

3 How to run demo

- Power off system.
- Connect eight SATA-III devices to CN0–CN2@PortA, CN4-CN6@PortA, and CN0-CN1@PortB, as shown in Figure 4.

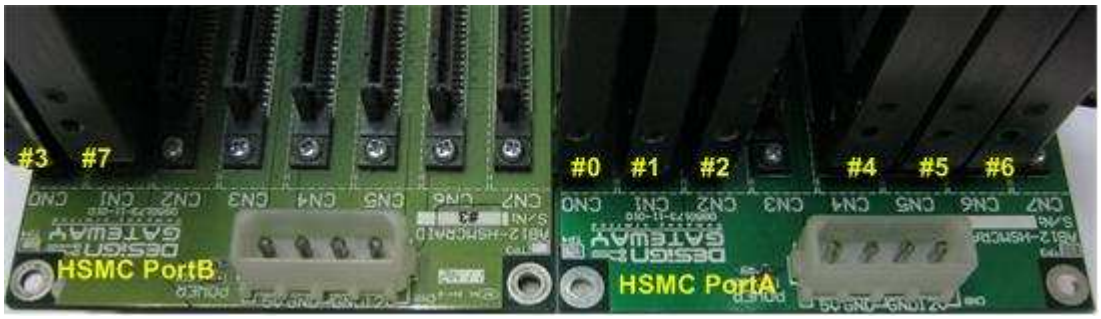

Figure 4 SATA-III device connection on two HSMCRAID boards

- Connect power to power connector on HSMCRAID board.
- Connect 2xHSMCRAID board to HSMC#A and HSMC#B connector on FPGA development board.
- Connect micro USB cable from FPGA development board to PC and connect power supply to the board.
- Power on FPGA development board.
- Open “Clock Control” application which is provided by Altera for each FPGA board, and set CLK0 value to be 150 MHz. Press “set new Frequency” button, and then wait until clock programmable complete.

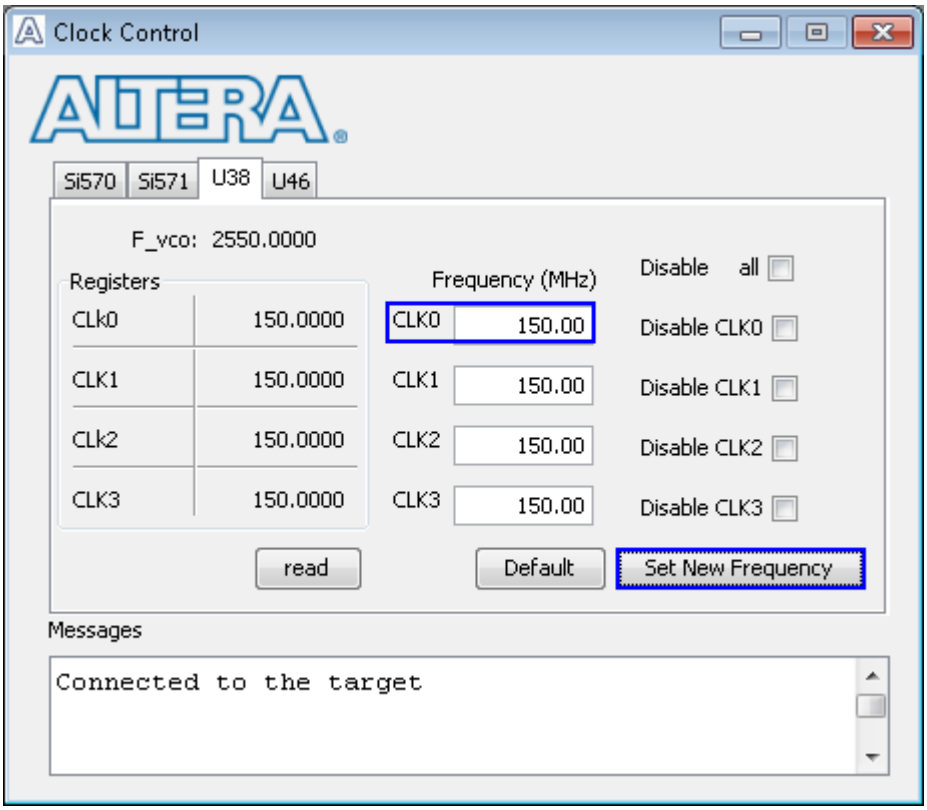

Figure 5 Set programmable clock = 150 MHz by Clock Control Application

- Open QuartusII Programmer and download “SATARaid0x8Ddr.sof” to FPGA board, as shown in Figure 6.

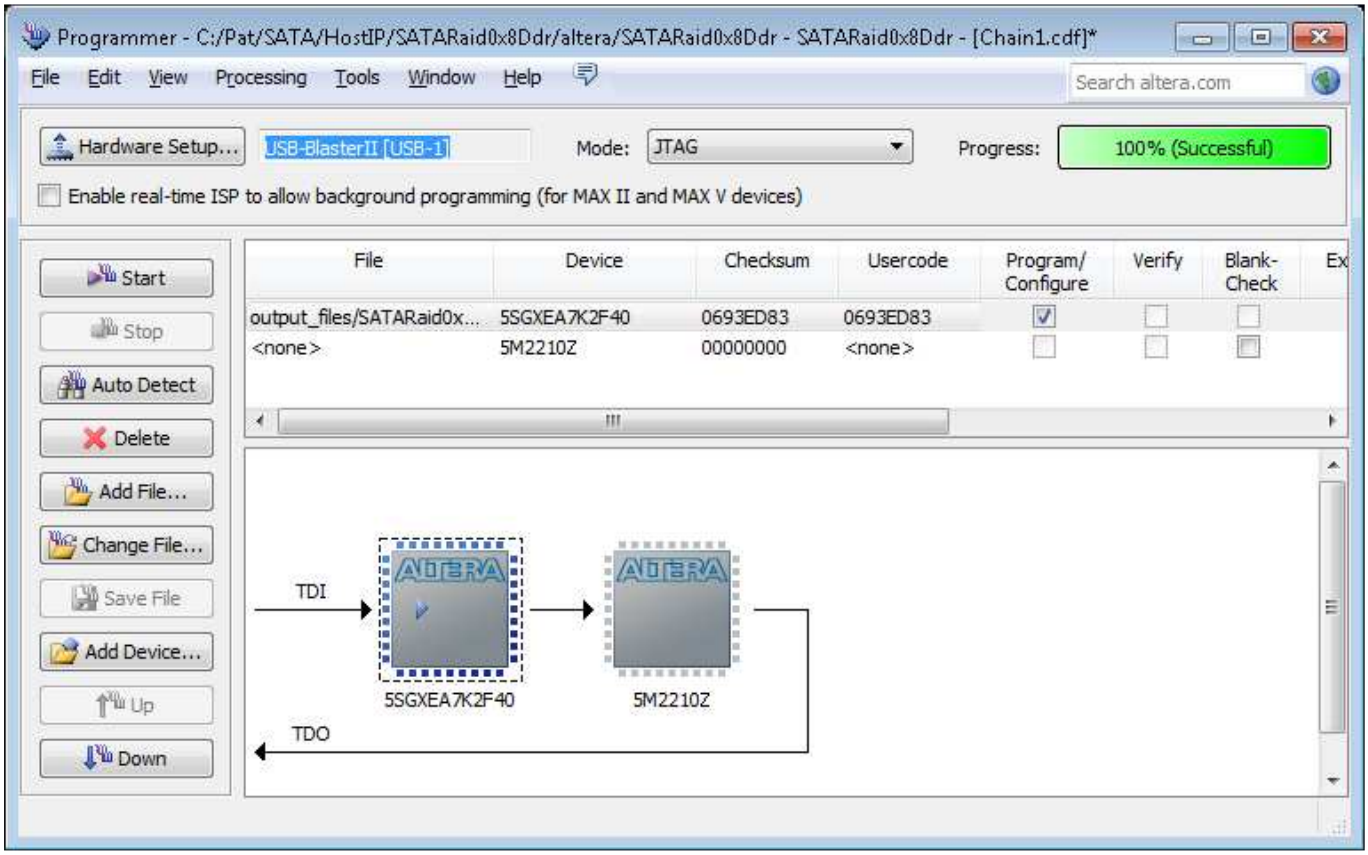

Figure 6 Programmer Environment

- Check LED status on FPGA board, and all 4-bit LED status must be OFF, as shown in Figure 7.
- LED[0] and [3] are ON if some SATA channels cannot be detected, as shown in Figure 8.

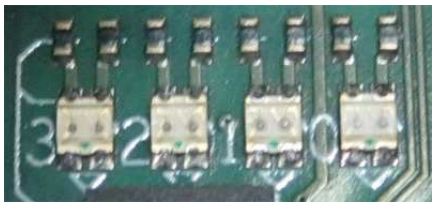

Figure 7 LED Status when all SATA devices LINKUP and system is in Idle

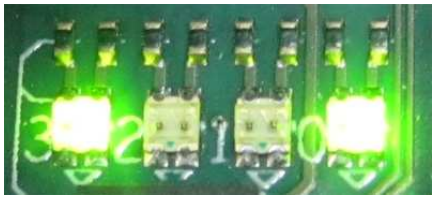

Figure 8 LED Status when some SATA devices cannot detect

- Set 6-bit DIPSW to select test pattern, test size, and test speed. Then, press WrStart for recording test data to RAID0. LED[1]-LED[3] will be ON during write transfer, as shown in Figure 9. Wait until write operation complete by monitoring all LEDs OFF.
- User can change test speed to faster rate if RAID0 has read performance better than write performance. Then, press RdStart for verifying test data from RAID0.

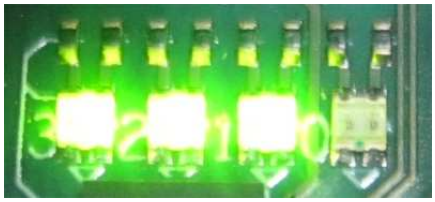

Figure 9 LED Status during Write/Read processing

- LED[1] will be blink, if test data verification is failed, as shown in Figure 10. In this case, please check DIPSW[1] that test pattern setting is same as previous write test), and check DIPSW[4:2] that test size setting is not more than test size in previous write test.

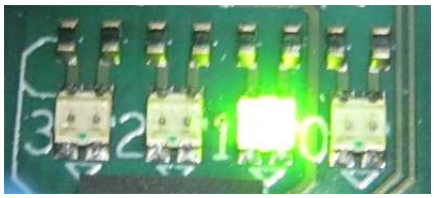

Figure 10 LED[1] Blink when data verification is failed

- LED[2] will be blink as shown in Figure 11, if test speed is too much (faster than SATA device performance). In this case, please change DIPSW[6:5] to reduce speed value.

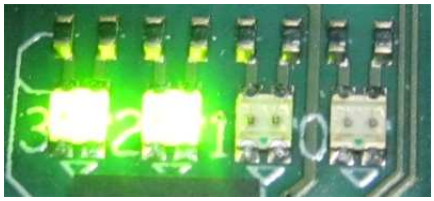

Figure 11 LED[2] Blink when test speed is too much

- When connecting SATA device to the PC and open by test application such as WinHex, user can check test data filled in the disk, as shown in Figure 12 and Figure 13. 32-bit increment pattern is split to store in each disk sector by sector. In this example,
  - Test data byte 0-511 is stored in the 1st sector at SATA CH#0
  - Test data byte 512-1023 is stored in the 1st sector at SATA CH#1
  - Test data byte 3072-3583 is stored in the 1st sector at SATA CH#6
  - Test data byte 3584-4095 is stored in the 1st sector at SATA CH#7

The 1st sector at SATA CH#0 when filled by 32-bit increment pattern

Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000000000	00	00	00	00	01	00	00	00	02	00	00	00	03	00	00	00
0000000010	04	00	00	00	05	00	00	00	06	00	00	00	07	00	00	00
0000000020	08	00	00	00	09	00	00	00	0A	00	00	00	0B	00	00	00
0000000030	0C	00	00	00	0D	00	00	00	0E	00	00	00	0F	00	00	00
0000000040	10	00	00	00	11	00	00	00	12	00	00	00	13	00	00	00
0000000050	14	00	00	00	15	00	00	00	16	00	00	00	17	00	00	00
0000000060	18	00	00	00	19	00	00	00	1A	00	00	00	1B	00	00	00
0000000070	1C	00	00	00	1D	00	00	00	1E	00	00	00	1F	00	00	00
0000000080	20	00	00	00	21	00	00	00	22	00	00	00	23	00	00	00
0000000090	24	00	00	00	25	00	00	00	26	00	00	00	27	00	00	00
00000000A0	28	00	00	00	29	00	00	00	2A	00	00	00	2B	00	00	00
00000000B0	2C	00	00	00	2D	00	00	00	2E	00	00	00	2F	00	00	00
00000000C0	30	00	00	00	31	00	00	00	32	00	00	00	33	00	00	00
00000000D0	34	00	00	00	35	00	00	00	36	00	00	00	37	00	00	00
00000000E0	38	00	00	00	39	00	00	00	3A	00	00	00	3B	00	00	00
00000000F0	3C	00	00	00	3D	00	00	00	3E	00	00	00	3F	00	00	00
0000000100	40	00	00	00	41	00	00	00	42	00	00	00	43	00	00	00
0000000110	44	00	00	00	45	00	00	00	46	00	00	00	47	00	00	00
0000000120	48	00	00	00	49	00	00	00	4A	00	00	00	4B	00	00	00
0000000130	4C	00	00	00	4D	00	00	00	4E	00	00	00	4F	00	00	00
0000000140	50	00	00	00	51	00	00	00	52	00	00	00	53	00	00	00
0000000150	54	00	00	00	55	00	00	00	56	00	00	00	57	00	00	00
0000000160	58	00	00	00	59	00	00	00	5A	00	00	00	5B	00	00	00
0000000170	5C	00	00	00	5D	00	00	00	5E	00	00	00	5F	00	00	00
0000000180	60	00	00	00	61	00	00	00	62	00	00	00	63	00	00	00
0000000190	64	00	00	00	65	00	00	00	66	00	00	00	67	00	00	00
00000001A0	68	00	00	00	69	00	00	00	6A	00	00	00	6B	00	00	00
00000001B0	6C	00	00	00	6D	00	00	00	6E	00	00	00	6F	00	00	00
00000001C0	70	00	00	00	71	00	00	00	72	00	00	00	73	00	00	00
00000001D0	74	00	00	00	75	00	00	00	76	00	00	00	77	00	00	00
00000001E0	78	00	00	00	79	00	00	00	7A	00	00	00	7B	00	00	00
00000001F0	7C	00	00	00	7D	00	00	00	7E	00	00	00	7F	00	00	00
0000000200	00	04	00	00	01	04	00	00	02	04	00	00	03	04	00	00
0000000210	04	04	00	00	05	04	00	00	06	04	00	00	07	04	00	00

The 1st sector at SATA CH#1 when filled by 32-bit increment pattern

Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000000000	80	00	00	00	81	00	00	00	82	00	00	00	83	00	00	00
0000000010	84	00	00	00	85	00	00	00	86	00	00	00	87	00	00	00
0000000020	88	00	00	00	89	00	00	00	8A	00	00	00	8B	00	00	00
0000000030	8C	00	00	00	8D	00	00	00	8E	00	00	00	8F	00	00	00
0000000040	90	00	00	00	91	00	00	00	92	00	00	00	93	00	00	00
0000000050	94	00	00	00	95	00	00	00	96	00	00	00	97	00	00	00
0000000060	98	00	00	00	99	00	00	00	9A	00	00	00	9B	00	00	00
0000000070	9C	00	00	00	9D	00	00	00	9E	00	00	00	9F	00	00	00
0000000080	A0	00	00	00	A1	00	00	00	A2	00	00	00	A3	00	00	00
0000000090	A4	00	00	00	A5	00	00	00	A6	00	00	00	A7	00	00	00
00000000A0	A8	00	00	00	A9	00	00	00	AA	00	00	00	AB	00	00	00
00000000B0	AC	00	00	00	AD	00	00	00	AE	00	00	00	AF	00	00	00
00000000C0	B0	00	00	00	B1	00	00	00	B2	00	00	00	B3	00	00	00
00000000D0	B4	00	00	00	B5	00	00	00	B6	00	00	00	B7	00	00	00
00000000E0	B8	00	00	00	B9	00	00	00	BA	00	00	00	BB	00	00	00
00000000F0	BC	00	00	00	BD	00	00	00	BE	00	00	00	BF	00	00	00
0000000100	C0	00	00	00	C1	00	00	00	C2	00	00	00	C3	00	00	00
0000000110	C4	00	00	00	C5	00	00	00	C6	00	00	00	C7	00	00	00
0000000120	C8	00	00	00	C9	00	00	00	CA	00	00	00	CB	00	00	00
0000000130	CC	00	00	00	CD	00	00	00	CE	00	00	00	CF	00	00	00
0000000140	D0	00	00	00	D1	00	00	00	D2	00	00	00	D3	00	00	00
0000000150	D4	00	00	00	D5	00	00	00	D6	00	00	00	D7	00	00	00
0000000160	D8	00	00	00	D9	00	00	00	DA	00	00	00	DB	00	00	00
0000000170	DC	00	00	00	DD	00	00	00	DE	00	00	00	DF	00	00	00
0000000180	E0	00	00	00	E1	00	00	00	E2	00	00	00	E3	00	00	00
0000000190	E4	00	00	00	E5	00	00	00	E6	00	00	00	E7	00	00	00
00000001A0	E8	00	00	00	E9	00	00	00	EA	00	00	00	EB	00	00	00
00000001B0	EC	00	00	00	ED	00	00	00	EE	00	00	00	EF	00	00	00
00000001C0	F0	00	00	00	F1	00	00	00	F2	00	00	00	F3	00	00	00
00000001D0	F4	00	00	00	F5	00	00	00	F6	00	00	00	F7	00	00	00
00000001E0	F8	00	00	00	F9	00	00	00	FA	00	00	00	FB	00	00	00
00000001F0	FC	00	00	00	FD	00	00	00	FE	00	00	00	FF	00	00	00
0000000200	80	04	00	00	81	04	00	00	82	04	00	00	83	04	00	00
0000000210	84	04	00	00	85	04	00	00	86	04	00	00	87	04	00	00

Figure 12 Example of Test data within SATA device at CH#0/CH#1

The 1st sector at SATA CH#6 when filled by 32-bit increment pattern

Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000000000	00	03	00	00	01	03	00	00	02	03	00	00	03	03	00	00
0000000010	04	03	00	00	05	03	00	00	06	03	00	00	07	03	00	00
0000000020	08	03	00	00	09	03	00	00	0A	03	00	00	0B	03	00	00
0000000030	0C	03	00	00	0D	03	00	00	0E	03	00	00	0F	03	00	00
0000000040	10	03	00	00	11	03	00	00	12	03	00	00	13	03	00	00
0000000050	14	03	00	00	15	03	00	00	16	03	00	00	17	03	00	00
0000000060	18	03	00	00	19	03	00	00	1A	03	00	00	1B	03	00	00
0000000070	1C	03	00	00	1D	03	00	00	1E	03	00	00	1F	03	00	00
0000000080	20	03	00	00	21	03	00	00	22	03	00	00	23	03	00	00
0000000090	24	03	00	00	25	03	00	00	26	03	00	00	27	03	00	00
00000000A0	28	03	00	00	29	03	00	00	2A	03	00	00	2B	03	00	00
00000000B0	2C	03	00	00	2D	03	00	00	2E	03	00	00	2F	03	00	00
00000000C0	30	03	00	00	31	03	00	00	32	03	00	00	33	03	00	00
00000000D0	34	03	00	00	35	03	00	00	36	03	00	00	37	03	00	00
00000000E0	38	03	00	00	39	03	00	00	3A	03	00	00	3B	03	00	00
00000000F0	3C	03	00	00	3D	03	00	00	3E	03	00	00	3F	03	00	00
0000000100	40	03	00	00	41	03	00	00	42	03	00	00	43	03	00	00
0000000110	44	03	00	00	45	03	00	00	46	03	00	00	47	03	00	00
0000000120	48	03	00	00	49	03	00	00	4A	03	00	00	4B	03	00	00
0000000130	4C	03	00	00	4D	03	00	00	4E	03	00	00	4F	03	00	00
0000000140	50	03	00	00	51	03	00	00	52	03	00	00	53	03	00	00
0000000150	54	03	00	00	55	03	00	00	56	03	00	00	57	03	00	00
0000000160	58	03	00	00	59	03	00	00	5A	03	00	00	5B	03	00	00
0000000170	5C	03	00	00	5D	03	00	00	5E	03	00	00	5F	03	00	00
0000000180	60	03	00	00	61	03	00	00	62	03	00	00	63	03	00	00
0000000190	64	03	00	00	65	03	00	00	66	03	00	00	67	03	00	00
00000001A0	68	03	00	00	69	03	00	00	6A	03	00	00	6B	03	00	00
00000001B0	6C	03	00	00	6D	03	00	00	6E	03	00	00	6F	03	00	00
00000001C0	70	03	00	00	71	03	00	00	72	03	00	00	73	03	00	00
00000001D0	74	03	00	00	75	03	00	00	76	03	00	00	77	03	00	00
00000001E0	78	03	00	00	79	03	00	00	7A	03	00	00	7B	03	00	00
00000001F0	7C	03	00	00	7D	03	00	00	7E	03	00	00	7F	03	00	00
0000000200	00	07	00	00	01	07	00	00	02	07	00	00	03	07	00	00
0000000210	04	07	00	00	05	07	00	00	06	07	00	00	07	07	00	00

The 1st sector at SATA CH#7 when filled by 32-bit increment pattern

Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000000000	80	03	00	00	81	03	00	00	82	03	00	00	83	03	00	00
0000000010	84	03	00	00	85	03	00	00	86	03	00	00	87	03	00	00
0000000020	88	03	00	00	89	03	00	00	8A	03	00	00	8B	03	00	00
0000000030	8C	03	00	00	8D	03	00	00	8E	03	00	00	8F	03	00	00
0000000040	90	03	00	00	91	03	00	00	92	03	00	00	93	03	00	00
0000000050	94	03	00	00	95	03	00	00	96	03	00	00	97	03	00	00
0000000060	98	03	00	00	99	03	00	00	9A	03	00	00	9B	03	00	00
0000000070	9C	03	00	00	9D	03	00	00	9E	03	00	00	9F	03	00	00
0000000080	A0	03	00	00	A1	03	00	00	A2	03	00	00	A3	03	00	00
0000000090	A4	03	00	00	A5	03	00	00	A6	03	00	00	A7	03	00	00
00000000A0	A8	03	00	00	A9	03	00	00	AA	03	00	00	AB	03	00	00
00000000B0	AC	03	00	00	AD	03	00	00	AE	03	00	00	AF	03	00	00
00000000C0	B0	03	00	00	B1	03	00	00	B2	03	00	00	B3	03	00	00
00000000D0	B4	03	00	00	B5	03	00	00	B6	03	00	00	B7	03	00	00
00000000E0	B8	03	00	00	B9	03	00	00	BA	03	00	00	BB	03	00	00
00000000F0	BC	03	00	00	BD	03	00	00	BE	03	00	00	BF	03	00	00
0000000100	C0	03	00	00	C1	03	00	00	C2	03	00	00	C3	03	00	00
0000000110	C4	03	00	00	C5	03	00	00	C6	03	00	00	C7	03	00	00
0000000120	C8	03	00	00	C9	03	00	00	CA	03	00	00	CB	03	00	00
0000000130	CC	03	00	00	CD	03	00	00	CE	03	00	00	CF	03	00	00
0000000140	D0	03	00	00	D1	03	00	00	D2	03	00	00	D3	03	00	00
0000000150	D4	03	00	00	D5	03	00	00	D6	03	00	00	D7	03	00	00
0000000160	D8	03	00	00	D9	03	00	00	DA	03	00	00	DB	03	00	00
0000000170	DC	03	00	00	DD	03	00	00	DE	03	00	00	DF	03	00	00
0000000180	E0	03	00	00	E1	03	00	00	E2	03	00	00	E3	03	00	00
0000000190	E4	03	00	00	E5	03	00	00	E6	03	00	00	E7	03	00	00
00000001A0	E8	03	00	00	E9	03	00	00	EA	03	00	00	EB	03	00	00
00000001B0	EC	03	00	00	ED	03	00	00	EE	03	00	00	EF	03	00	00
00000001C0	F0	03	00	00	F1	03	00	00	F2	03	00	00	F3	03	00	00
00000001D0	F4	03	00	00	F5	03	00	00	F6	03	00	00	F7	03	00	00
00000001E0	F8	03	00	00	F9	03	00	00	FA	03	00	00	FB	03	00	00
00000001F0	FC	03	00	00	FD	03	00	00	FE	03	00	00	FF	03	00	00
0000000200	80	07	00	00	81	07	00	00	82	07	00	00	83	07	00	00
0000000210	84	07	00	00	85	07	00	00	86	07	00	00	87	07	00	00

Figure 13 Example of Test data within SATA device at CH#6/CH#7

4 Revision History

Revision	Date	Description
1.0	10-Jun-15	Initial version release
1.1	24-Jun-15	Update test size, and add LED4-7 description to be test point