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Core Facts

Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	Encrypted Netlist File
Constraints Files	User constraint file
Instantiation Templates	VHDL
Reference Designs & Application Notes	Vivado Project, See Reference Design Manual
Additional Items	Demo on AC701/KC705/ ZC706/VC707/VC709/KCU105/ Zynq Mini-ITX/ZCU102
Support	
Support Provided by Design Gateway Co., Ltd.	

Features

- Simple user interface by dgIF typeS
- Pin compatible to DG SATA-IP
- Small logic resource without BlockRAM utilization
- Suitable for system without CPU and external memory (DDR)
- Support four ATA commands for application layer, i.e. IDENTIFY DEVICE, SECURITY ERASE UNIT, WRITE DMA (EXT), and READ DMA (EXT)
- Reference design with DG SATA-IP by using AB09-FMCRAID adapter board on AC701/KC705/ ZC706/VC707/VC709/KCU105/Zynq Mini-ITX/ZCU102 board

Table 1: Example Implementation Statistics for Ultrascale device

Family	Example Device	Fmax (MHz)	CLB Regs	CLB LUTs	CLB[1]	IOB	BUFG	RAMB18	PLL	GTH	Design Tools
Kintex-Ultrascale	XCKU040FFVA1156-2E	476	563	704	161	-	-	-	-	-	Vivado2015.4
Zynq-Ultrascale+	XCZU9EG-FFVB1156-2-I	>500	559	473	135	-	-	-	-	-	Vivado2017.3

Notes:
1) Actual slice count dependent on percentage of unrelated logic. The example is the report from utilization_placed.rpt file.
2) Assuming clocks are routed off-chip

Table 2: Example Implementation Statistics for 7-Series device

Family	Example Device	Fmax (MHz)	Slice Regs	Slice LUTs	Slices [1]	IOB	BUFG	RAMB18	PLL	GTP/GTX	Design Tools
Artix-7	XC7A200TFBG676-2	263	563	578	238	-	-	-	-	-	Vivado2015.4
Kintex-7	XC7K325TFFG900-2	370	563	704	278	-	-	-	-	-	Vivado2015.4
Zynq-7000	XC7Z045FFG900-2	400	563	708	275	-	-	-	-	-	Vivado2015.4
Virtex-7	XC7VX485TFFG1761-2	357	563	703	271	-	-	-	-	-	Vivado2015.4

Notes:
1) Actual slice count dependent on percentage of unrelated logic. The example is the report from utilization_placed.rpt file.
2) Assuming clocks are routed off-chip

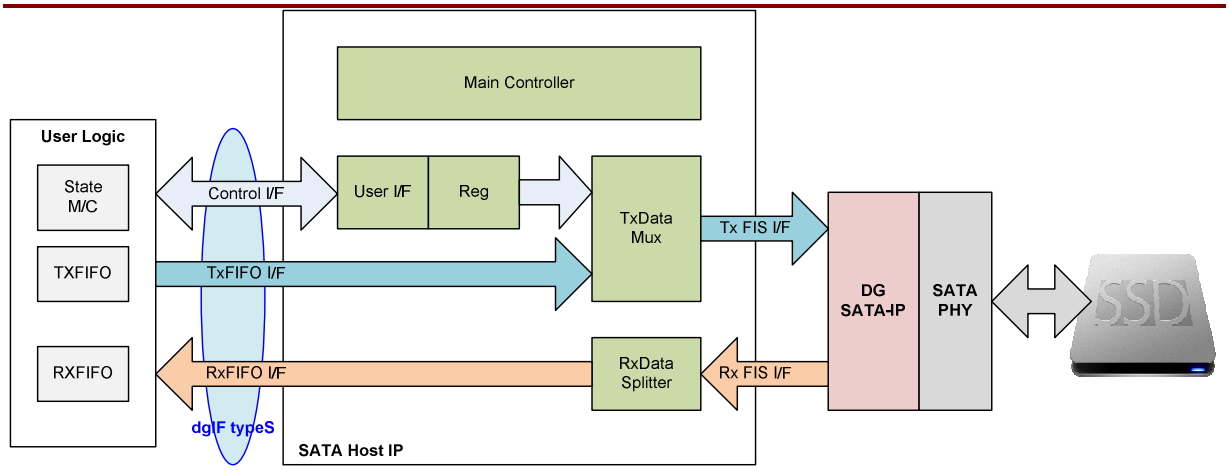

Figure 1: SATA Host IP Block Diagram

Applications

SATA Host IP Core operating with DG SATA-IP and SATA PHY is ideal to access SATA device without using both CPU and external memory. The resource utilization of the IP is less, but it can achieve very high performance. Using multiple IP for RAID0 can increase total performance of storage system. So, it is recommended to use the IP in very high-speed data recording system or big-data storage.

General Description

SATA Host IP Core implements the application layer and remaining part of transport layer which is not implemented in DG SATA-IP. So, user can simply write/read data to SATA device by designing the logic to interface SATA Host IP through dgIF typeS interface. dgIF typeS interface is DG interface standard for all storage IPs and it consists of command value, start address, and transfer length for command interface and general FIFO signal for data interface. Four ATA commands are supported, i.e. IDENTIFY DEVICE to check SATA device capacity, SECURITY ERASE UNIT to erase data in SATA device, WRITE DMA (EXT) to record data to SATA device, and READ DMA (EXT) to read data back from SATA device. Clock domain for SATA Host IP must be same as user clock at DG SATA-IP because there is no asynchronous circuit inside the IP. Error signal will be asserted if the FIS packet sequence from SATA device is not correct.

The reference design to test write/read data with SATA-II/III device on Xilinx evaluation board are available to download for evaluation before purchasing.

Functional Description

SATA Host IP Core is designed to create/decode SATA FIS interface with DG SATA-IP. The IP consists of two logic blocks, i.e. Data FIS control to process Data FIS type and Control/Status FIS control to process other FIS types. Data FIS is the interface between User FIFO and SATA-IP while Control/Status FIS is the interface between User control I/F and SATA-IP.

Control/Status

After system power-on, Host IP will wait FIS returned from SATA device to confirm that all initialization process are completed. After that, user can send new command request to IP. Command FIS will be created by using parameter from user input and forwards to SATA-IP. If total transfer size is more than maximum size in one command (32 MB), the IP will create multiple commands to SATA-IP until total size equal to set value from user. Two submodules are included in this blocks as follows.

- **Main Controller**

  Control FIS packet sequence for each command and select source of data path for SATA-IP that should be control FIS type or data FIS type for each sequence.

- **User I/F and Reg**

  Command, Address, and transfer size from user request are latched into the register, and then convert the information to build Command FIS of Identify Device, Erase, Write, or Read for SATA device. Also, status returned from SATA device is decoded to confirm that the operation of the command is completely.

Data

To create data FIS for write command, data from TxFIFO is fed and combined to the header value to form FIS packet. If transfer data size is more than one FIS packet size, data stream from TxFIFO will be splitted into many packets before forwarding to SATA-IP. For read command, header in Data FIS packet will be checked and removed. Only raw data will be stored to RxFIFO. Data output from Identify device command will not be stored to UserFIFO, but will be forwarded to Iden port instead.

- **TxData Mux**

  Data Multiplexer to select Command FIS from User I/F and Reg, or Data FIS from TXFIFO for write command

- **RxData Splitter**

  Received FIS returned from SATA-IP will be decoded to check the type. Data FIS with removing the header will be stored to RxFIFO I/F, while other FISes will be monitored by Main Controller to confirm that operation is in correct sequence and no error detected.

User Logic

Simple logic to send command, address, and size can be designed. FIFO size is flexible depending on the resource and performance requirement of user system.

DG SATA-IP

Details of DG SATA-IP are described in the datasheet and can be downloaded from our website.
http://www.dgway.com/products/IP/SATA-IP/dg_sata_ip_data_sheet_7series_en.pdf

Core I/O Signals

Descriptions of all signal I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Dir	Description
User Interface		
RstB	In	Reset signal. Active low. Release this signal when Clk signal input is stable.
Clk	In	User clock. Must use the same clock as trn_clk of SATA-IP. (At least 150 MHz for SATA3 operation or at least 75 MHz for SATA2 operation)
dgIF typeS		
UserCmd[1:0]	In	User Command. “00”: Identify device command, “01”: Security erase unit command, “10”: Write SATA device, “11”: Read SATA device. Note: 1) Security erase unit operation time depends on SATA device characteristic. It may take long time to complete the operation. So, timeout counter in IP will be disabled for Security erase unit command. 2) Security erase unit is not mandatory command, so user should check SATA device specification firstly that the device can support this command before using it.
UserAddr[47:0]	In	Start address of SATA device to write/read in sector unit (512 byte).
UserLen[47:0]	In	Total transfer size in the request. Must not set equal to 0. Valid from 1 to (LBASize-UserAddr).
UserReq	In	Request the new command. Can be asserted only when the IP is Idle (UserBusy=’0’). Asserted with valid value on UserCmd/UserAddr/UserLen signals.
UserBusy	Out	IP Busy status. New request is not allowed if this signal is asserted to ‘1’.
LBASize[47:0]	Out	Total SATA device capacity in sector unit (512 byte). Default value is 0. This value will be updated after user sends Identify device command.
UserError	Out	Error flag. Assert when UserErrorType is not equal to 0. The flag can be reset only by asserting RstB signal.
UserErrorType[31:0]	Out	Error status. Details of the error flag. [0] – Error from SATA-IP such as CRC error, wrong primitives sequence. [1] – Error from Data FIS header [2] – Error from returned Status FIS [3] – Error from DMA active FIS. Write operation cannot complete. [4] – Error from PIO Setup FIS. Failure during SATA device identification process. [5] – Timeout error. No FIS returned from SATA device in time. [31:6] - Reserved
UserFifoWrCnt[15:0]	In	Write data counter of received FIFO. Used to check full status. If total FIFO size is less than 16-bit, please fill ‘1’ to upper bit. UserFifoWrEn will be asserted when UserFifoWrCnt[15:3] is not equal to all 1.
UserFifoWrEn	Out	Write data valid of received FIFO.
UserFifoWrData[31:0]	Out	Write data bus of received FIFO. Synchronous to UserFifoWrEn.
UserFifoRdCnt[15:0]	In	Read data counter of transmit FIFO. Used to check data available size in FIFO. If total FIFO size is less than 16-bit, please fill ‘0’ to upper bit. This signal is unused for this IP.
UserFifoEmpty	In	FIFO empty flag of transmit FIFO to check data available status.
UserFifoRdEn	Out	Read valid of transmit FIFO.
UserFifoRdData[31:0]	In	Read data returned from transmit FIFO. Valid after UserFifoRdEn asserted about one clock period.

Signal	Dir	Description
Other Interface		
TestPin[31:0]	Out	Reserved to be IP test point.
TimeOutSet[31:0]	Out	Timeout value to wait FIS returned from SATA device. Time unit is following Clk frequency value.
IdenWrEn	Out	Valid signal of IdenWrAddr and IdenWrData.
IdenWrAddr[6:0]	Out	Index of IdenWrData in 32-bit unit. Synchronous to IdenWrEn
IdenWrData[31:0]	Out	512-byte data from Identify device command. Synchronous to IdenWrEn.
SATA-IP Interface		
trn_rd[31:0]	In	Receive data bus from SATA-IP.
trn_rsof_n	In	Receive start-of-frame. Indicates start of SATA FIS packet. Active low.
trn_reof_n	In	Receive end-of-frame. Indicates end of SATA FIS packet. Active low.
trn_rsrc_rdy_n	In	Receive source ready. Indicates that trn_rd is valid. Active low.
trn_rsrc_dsc_n	In	Receive disconnect from SATA-IP. Active low.
trn_rdst_rdy_n	Out	Receive ready. Indicate that the IP is ready to accept data. Active low.
trn_rdst_dsc_n	Out	Receive disconnect from the IP. Active low. This value is always set to ‘1’.
trn_td[31:0]	Out	Transmit data bus to SATA-IP.
trn_teof_n	Out	Transmit end-of-frame. Indicates end of SATA FIS packet. Active low.
trn_tsrc_rdy_n	Out	Transmit source ready. Indicates that trn_td is valid. Active low.
trn_tsrc_dsc_n	Out	Transmit abort from the IP. Active low. This value is always set to ‘1’.
trn_tdst_rdy_n	In	Transmit ready. Indicates that SATA-IP is ready to accept data. Active low.
trn_tdst_dsc_n	In	Transmit abort from SATA-IP. Active low.

Timing Diagram

Initialization

After RstB is released, UserBusy flag will be set to '1' until device initialization complete. After that, UserBusy will be deasserted and IP will be ready to receive new command, as shown in Figure 2.

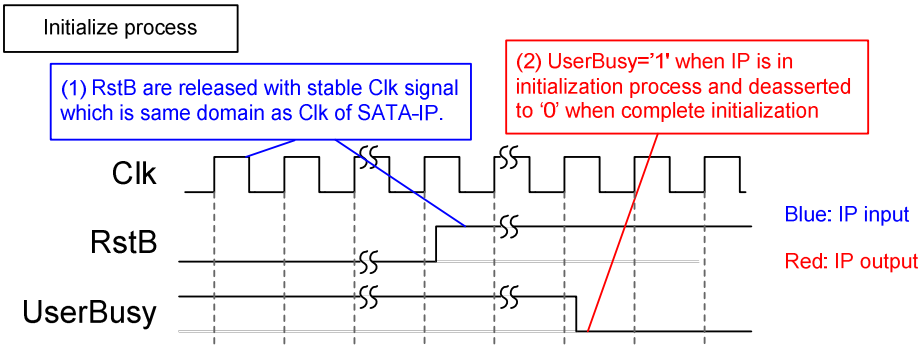

Figure 2: RstB and UserBusy during IP intialization

dgIF typeS

dgIF typeS signal can be split into two interfaces, i.e. command interface and data interface. Figure 3 shows timing diagram of command interface of dgIF typeS. Before sending new command to the IP, UserBusy must be always monitored to confirm that IP is Idle. UserCmd, UserAddr, and UserLen must be valid and latched during asserting UserReq='1'. UserBusy will change status from '0' to '1' after start the command operation. So, UserReq can be cleared and user logic can prepare the next command to the command bus.
Note: UserAddr and UserLen value may be ignored in some commands such as Identify command.

For data interface, transmit FIFO will be read for Write command while received FIFO will be written for Read command. Timing diagram of data interface is shown in Figure 4 and Figure 5.

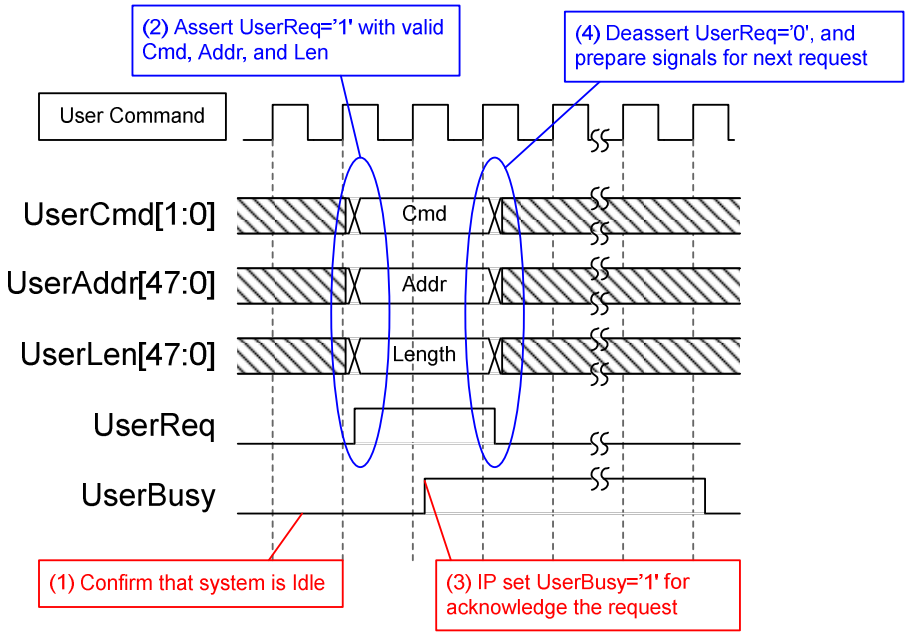

Figure 3: User Command Interface Timing diagram

For write command, UserFifoEmpty will be monitored to check data available status of transmit FIFO. When data is ready, UserFifoRdEn is asserted to forward data from transmit FIFO to SATA-IP until total numbers of data is equal to user request size. Similar to typical FIFO, UserFifoRdData is valid after UserFifoRdEn is asserted about 1 clock period, as shown in Figure 4.

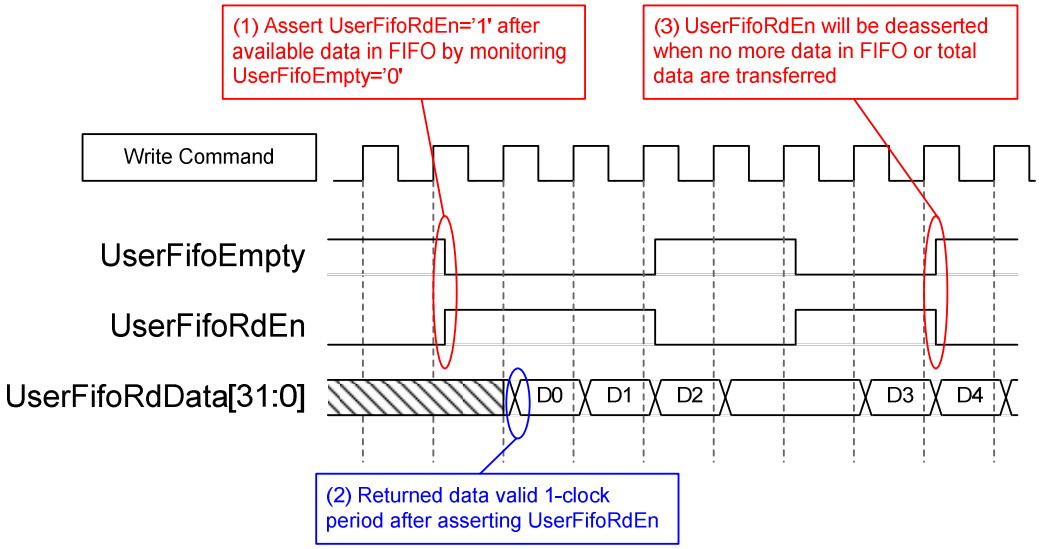

Figure 4: Transmit FIFO Interface for Write command

For read command, UserFifoWrEn will be asserted with the valid value of UserFifoWrData to store received data in Received FIFO until total numbers of data is equal to user request size. UserFifoWrCnt is monitored to check the remaining space area in the FIFO that still be more than 7. If UserFifoWrCnt is more than or equal to 65528 (0xFFF8), UserFifoWrEn will be deasserted within 7 clock to pause data transferring.

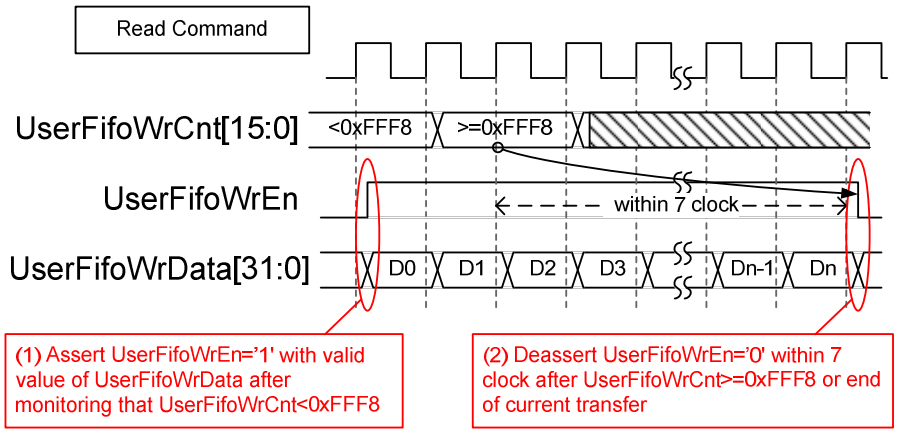

Figure 5: Received FIFO Interface for Read command

Identify Device

The first command sending to IP must be Identify Device command for updating LBASize signal. LBASize value is used in User Logic to confirm that the sum of address and length in write/read command is not out-of-range. All 512-byte data from Identify device command will be sent out through Iden port. User can read SATA device information such as model number, supported feature from this data.

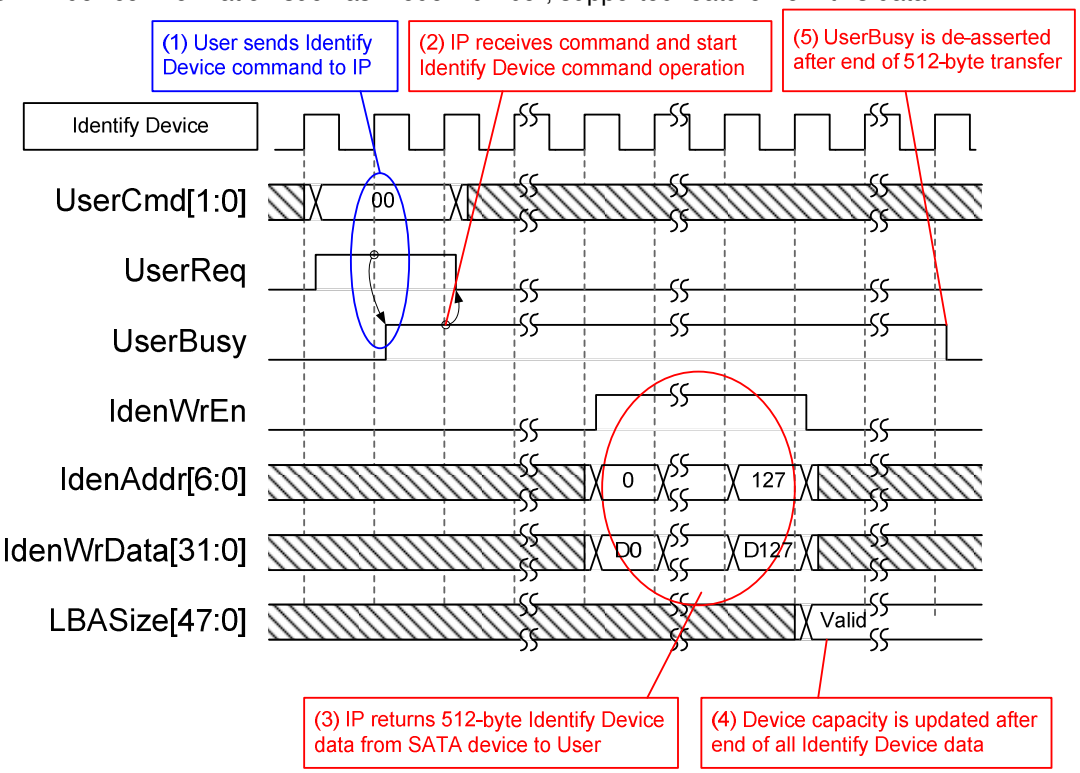

Figure 6: LBASize is updated after Identify Device command

Security Erase

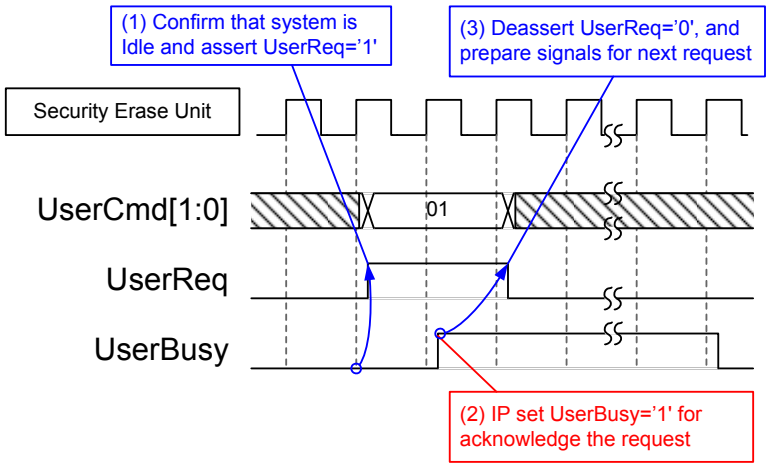

Figure 7: User interface for Security Erase Unit command

Similar to Identify Device command, UserAddr and UserLen input are not used for Security Erase Unit command. User should confirm from SATA device specficiation or from Identify device data firstly that the device can support this command. Erase time of each device is different and may be rather long. User can check the estimation erase time from Identify device data. UserBusy is asserted to '1' until the device complete erase operation.

Error

During normal operation, UserError and all bits of UserErrorType signal will be always 0. UserError is generated by OR condition of each-bit of UserErrorType. If any bit of UserErrorType is set to '1', UserError will be asserted and latched until RstB is asserted to '0', as shown in Figure 8.

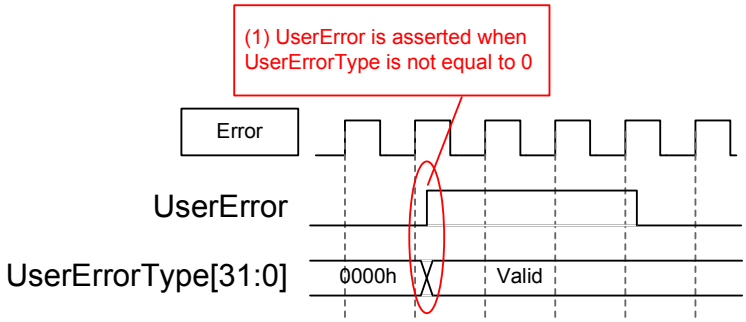

Figure 8: Error condition Timing diagram

Verification Methods

The SATA Host IP Core functionality was verified by simulation and also proved on real board design by using AC701/KC705/ZC706/VC707/VC709/KCU105/Zynq Mini-ITX/ZCU102 evaluation board.

Recommended Design Experience

Experience design engineers with a knowledge of Vivado Tools should easily integrate this IP into their design.

Ordering Information

This product is available directly from Design Gateway Co., Ltd. Please contact Design Gatway Co., Ltd. For pricing and additional information about this product using the contact information on the front page of this datasheet.

Revision History

Revision	Date	Description
1.0	Oct-9-2014	New release
1.1	Aug-29-2016	Update I/O signal and support Kintex Ultrascale device
1.2	Nov-9-2016	Add security erase command and support Mini-ITX/VC709 board
1.3	Jan-30-2017	Update interface to dgIF typeS
1.4	Jan-9-2018	Support ZCU102 board