SATA Host-IP reference design manual

Rev1.3 1-Aug-17

1. Overview

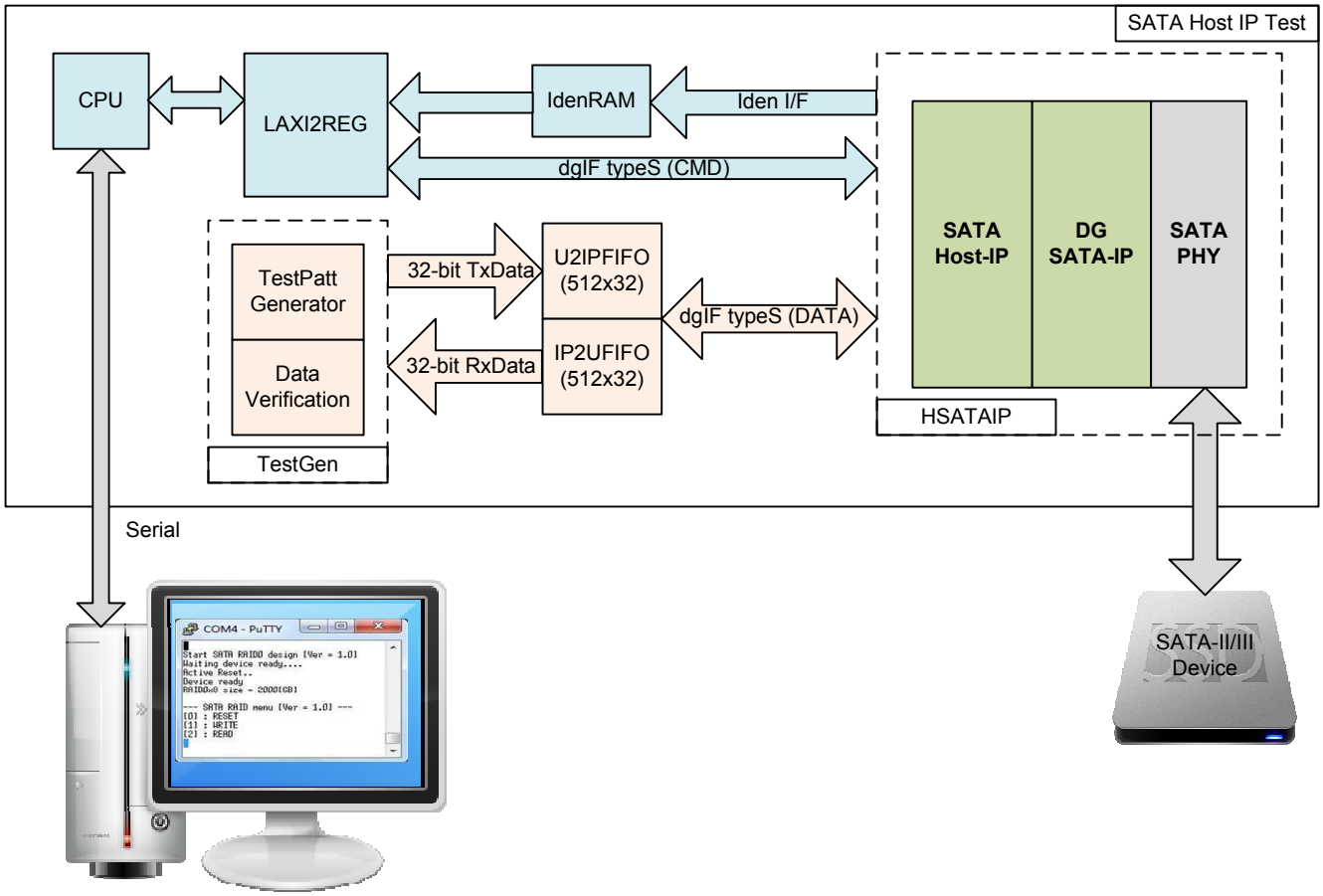

Figure 1 SATA Host IP Demo System

The reference design integrates SATA Host-IP, DG SATA-IP, and SATA-PHY to be SATA host standard platform. Simple logic is designed to show write/read data with SATA-II/III device at high-speed rate. CPU is additional designed from user interface through Serial Console.

For simple test, user can input the parameters such as start address, transfer size, and command to Serial console. The logic decodes all inputs and converts to be input value for SATA Host-IP. When the command is completed, CPU checks time usage and then calculates write/read performance of SATA-III device to be user output. To interface with CPU bus, LAXI2REG module is used to decode the address and data from CPU bus to be command interface of dgIF typeS for connecting with SATA Host-IP. Two external FIFOs are used to be buffer between SATA Host-IP and TestGen module.

User clock frequency in the reference design is 200 MHz while CPU System runs at 100 MHz. Asynchronous circuit is required within LAXI2REG.

User can download SATA Host-IP datasheet and send the request to evaluate our IP from the website: http://www.dgway.com/SATA-IP_X_E.html .
The real transfer performance in the demo depends on SATA device specification.

2. CPU

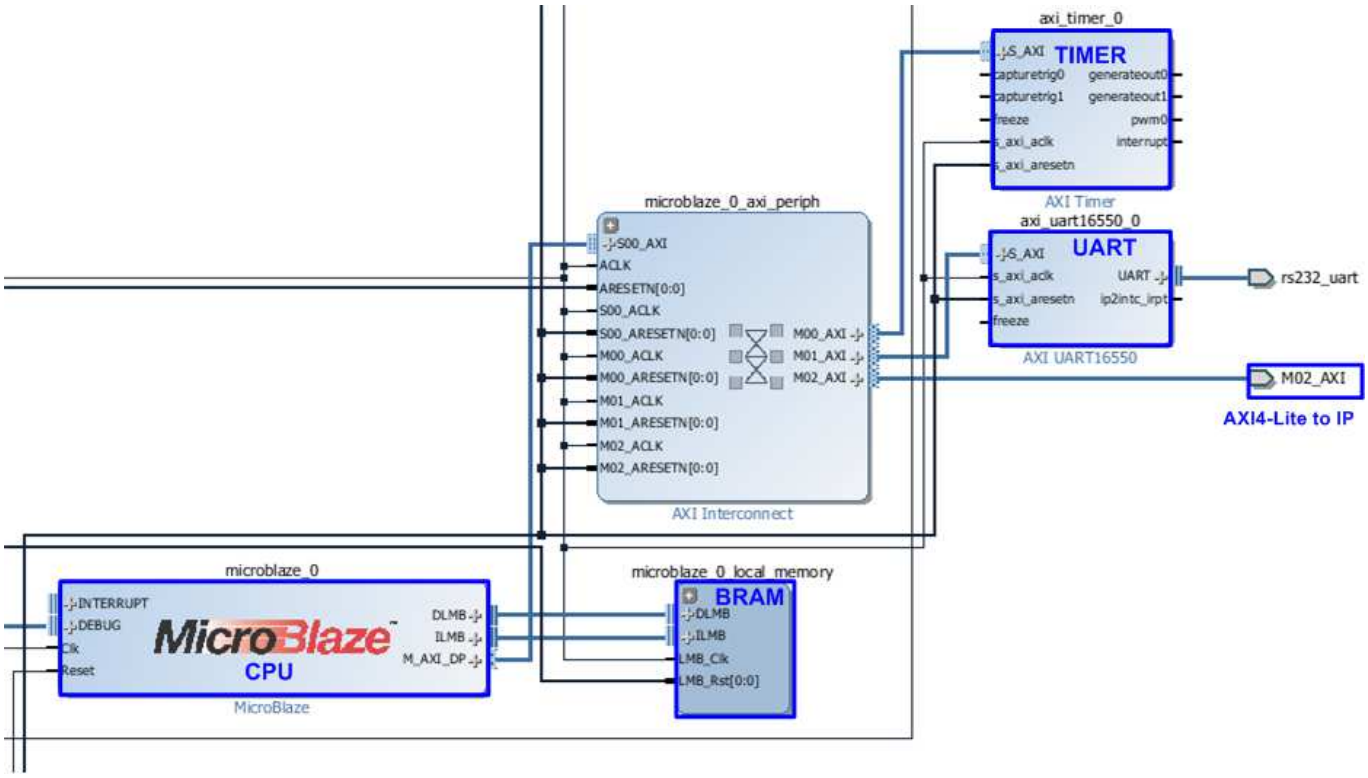

Figure 2 CPU system in reference design

In reference design, CPU peripherals are UART for user interface, Timer for performance measurement, and BRAM for CPU firmware. AXI-interconnect is used for CPU interface with its peripherals including the interface for controlling/monitoring SATA Host-IP which is 32-bit AXI4-Lite bus. More details about memory map of this AXI4-Lite are follows.

Table 1 Register Map

Address Rd/Wr	Register Name (Label in the “hsataiptest.c”)	Description
BA+0x00 Wr	User Address (Low) Reg (USRADRL_REG)	[31:0]: Input to be start sector address (UserAddr[31:0] of dgIF typeS)
BA+0x04 Wr	User Address (High) Reg (USRADRH_REG)	[15:0]: Input to be start sector address (UserAddr[47:32] of dgIF typeS)
BA+0x08 Wr	User Length (Low) Reg (USRLENL_REG)	[31:0]: Input to be transfer length in sector unit (UserLen[31:0] of dgIF typeS)
BA+0x0C Wr	User Length (High) Reg (USRLENH_REG)	[15:0]: Input to be transfer length in sector unit (UserLen[47:32] of dgIF typeS)
BA+0x10 Wr	User Command Reg (USRCMD_REG)	[1:0]: Input to be user command (UserCmd of dgIF typeS) “00”-Identify device, “01”-Security erase, “10”-Write SSD, “11”-Read SSD. When this register is written, the design generates command request to SATA Host-IP to start new command operation.
BA+0x14 Wr	Test Pattern Reg (PATTSEL_REG)	[2:0]: Test pattern select “000”-Increment, “001”-Decrement, “010”-All 0, “011”-All 1, “100”-LFSR

Address Rd/Wr	Register Name (Label in the “hsataiptest.c”)	Description
BA+0x100 Rd	User Status Reg (USRSTS_REG)	[0]: UserBusy of dgIF typeS (‘0’: Idle, ‘1’: Busy) [1]: UserError of dgIF typeS (‘0’: Normal, ‘1’: Error) [2]: Data verification fail (‘0’: Normal, ‘1’: Error) [4:3]: SATA speed from IP “00”: No linkup, “01”: SATA Gen1 (Not supported for all designs), “10”: SATA Gen2 (Not supported for KCU105), “11”: SATA Gen3
BA+0x104 Rd	Total disk size (Low) Reg (LBASIZEL_REG)	[31:0]: Total capacity of SATA device in sector unit (LBASize[31:0] of dgIF typeS)
BA+0x108 Rd	Total disk size (High) Reg (LBASIZEH_REG)	[15:0]: Total capacity of SATA device in sector unit (LBASize[47:32] of dgIF typeS)
BA+0x10C Rd	User Error Type Reg (USRERRTYPE_REG)	[31:0]: User error status (UserErrorType[31:0] of dgIF typeS)
BA+0x11C Rd	SATA Host IP Test pin Reg (TESTPIN_REG)	[31:0]: TestPin[31:0] output from SATA Host-IP
BA+0x120 Rd	Data Failure Address (Low) Reg (RDFAILNOL_REG)	[31:0]: Latch value of failure address[31:0] in byte unit from read command
BA+0x124 Rd	Data Failure Address (High) Reg (RDFAILNOH_REG)	[24:0]: Latch value of failure address [56:32] in byte unit from read command
BA+0x130 Rd	Expected value Word0 Reg (EXPPATW0_REG)	[31:0]: Latch value of expected data [31:0] from read command
BA+0x140 Rd	Read value Word0 Reg (RDPATW0_REG)	[31:0]: Latch value of read data [31:0] from read command
BA+0x150 Rd	Current test byte (Low) Reg (CURTESTSIZEL_REG)	[31:0]: Current test data size of TestGen module in byte unit (bit[31:0])
BA+0x154 Rd	Current test byte (High) Reg (CURTESTSIZEH_REG)	[24:0]: Current test data size of TestGen module in byte unit (bit[56:32])
BA+0x2000 – 0x21FF	Identify Device Command Data (IDENCTRL_REG)	512-byte Identify Device Data

After initialization complete, CPU firmware in the demo will be in idle state to wait user command input through Serial console. The command can be Identify device, Security erase, Write, or Read command. The sequence of each command is follows.

For Identify device command,

1) Set USRCMD_REG=”00”. Next, Test logic generates command and request to SATA Host-IP. Then, busy flag (USRSTS_REG[0]) changes from ‘0’ to ‘1’.
2) CPU waits until command complete or any error found by monitoring USRSTS_REG value. Bit[0] is cleared to ‘0’ when command is completed. Bit[1] is asserted to ‘1’ when any error is detected. If any error is detected, error message will be displayed.
3) To be test result, SATA device model name, security feature set supported, and erase time value decoded from IDENCTRL_REG are displayed to the command shell. Also, SATA device capacity read from LBASIZEL/H_REG is displayed.

For Security erase command,

1) Set USRCMD_REG=”01”. Test logic generates command and request to SATA Host-IP. Next, Busy flag (USRSTS_REG[0]) changes from ‘0’ to ‘1’.
2) CPU waits until command complete by monitoring USRSTS_REG value. Bit[0] is cleared to ‘0’ when command is completed. This operation may use long time to operate, so there is dummy message displayed on the console every second to show system alive status. Finally, total time usage is printed on the command shell when command is completed.

For write/read command,

1) Receive start address, transfer length, and test pattern value from user through command shell. If any input is invalid, the operation will be cancelled.
2) Get all inputs and set the value to USRADRL/H_REG, USRLENL/H_REG, and USRCMD_REG (USRCMD_REG=”10” for write transfer, and “11” for read transfer).
3) Similar to step 2) in Identify device command. But USRSTS_REG[2] is also monitored for read command to confirm that read data is correct.
4) During running command, current transfer size from CURTESTSIZE_REG is printed to console during operating. Finally, test performance is displayed on the command shell when command is completed.

3. LAXI2REG

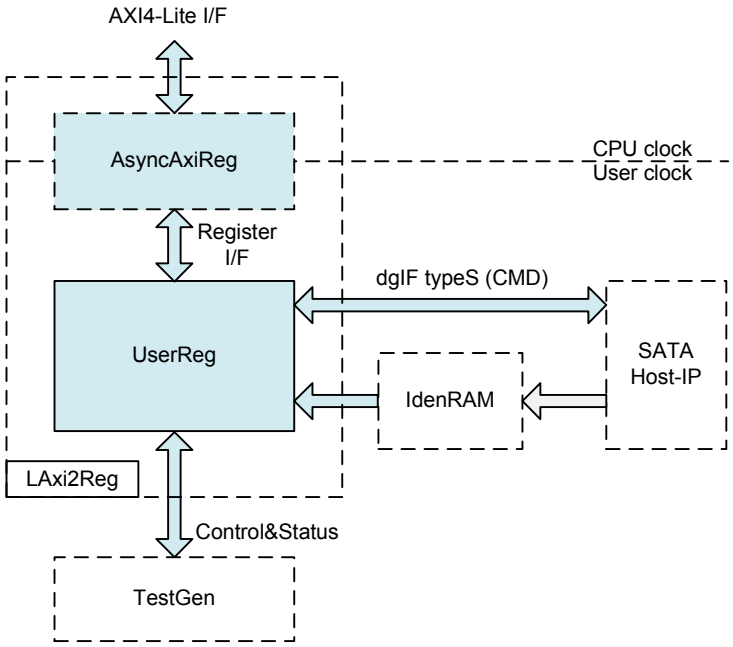

Figure 3 LAXI2REG interface

This module consists of two submodules, i.e. AsyncAXIReg and UserReg. AsyncAXIReg is designed to convert AXI4-Lite bus to be register interface and to convert clock domain from CPU clock to user clock system. UserReg module includes the logic to decode Write/Read address to select the register for current access. The address is decoded following Table 1. Transfer parameters such as transfer direction, size, and address from user are converted to be command interface of dgIF typeS for SATA Host-IP and converted to be control signal for TestGen module. During transferring, CPU reads the register to check SATA Host-IP status, TestGen result, or Identify device data.

4. TestGen

In this module, there are two operations, i.e. generating test data to WrFf port when user selects write command, or verifying received data from RdFf port when user selects read command. The details of logic design inside this module are displayed in Figure 4.

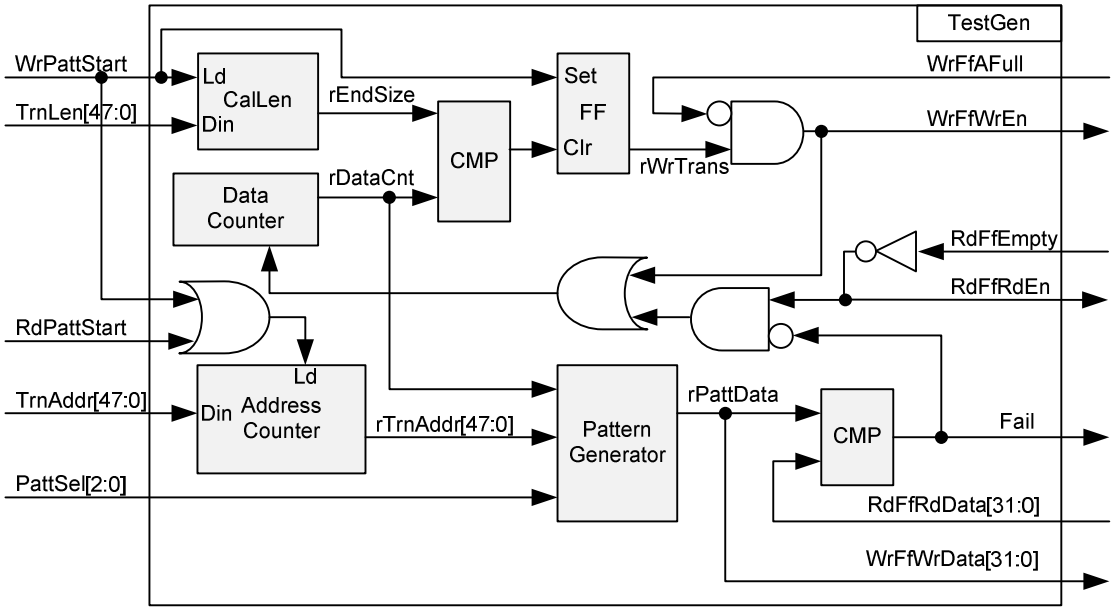

Figure 4 Logic design in TestGen

To start write transfer, WrPattStart is asserted to '1' with valid signal on TrnLen and TrnAddr. TrnLen is used to calculate the end position of write transfer. rWrTrans which is designed to be write enable signal for WrFf port is controlled by WrPattStart and end position signal (rEndSize). WrFfAFull is used to be flow control for write transfer. If this signal is asserted to '1', WrFfWrEn will be de-asserted to '0' to pause data generating.

There are two counters inside this module, i.e. Data counter which is used to count total transfer size to monitor end transfer timing. Another is current address counter in sector unit (512-byte). The address counter loads the start value from TrnAddr signal. The address counter is increment when end of each 512-byte transfer. Pattern Generator reads the current address from rTrnAddr to be 64-bit header value of each sector. Also, this value is used to be start test pattern for 32-bit increment, 32-bit decrement, and 32-bit LFSR counter. rPattData is applied to be WrFfWrData for write transfer and applied to be expect value for read command.

For read transfer, RdPattStart is used to be load signal for Address counter only. RdFfRdEn is controlled by RdFfEmpty. It is simple design of RdFfRdEn by using not logic of RdFfEmpty signal. Fail flag will be asserted to '1' if RdFfRdData from RdFf port is not equal to test pattern.

5. Example Test Result

The example test result when running demo system by using 256 GB Samsung 850 Pro is shown in Figure 5.

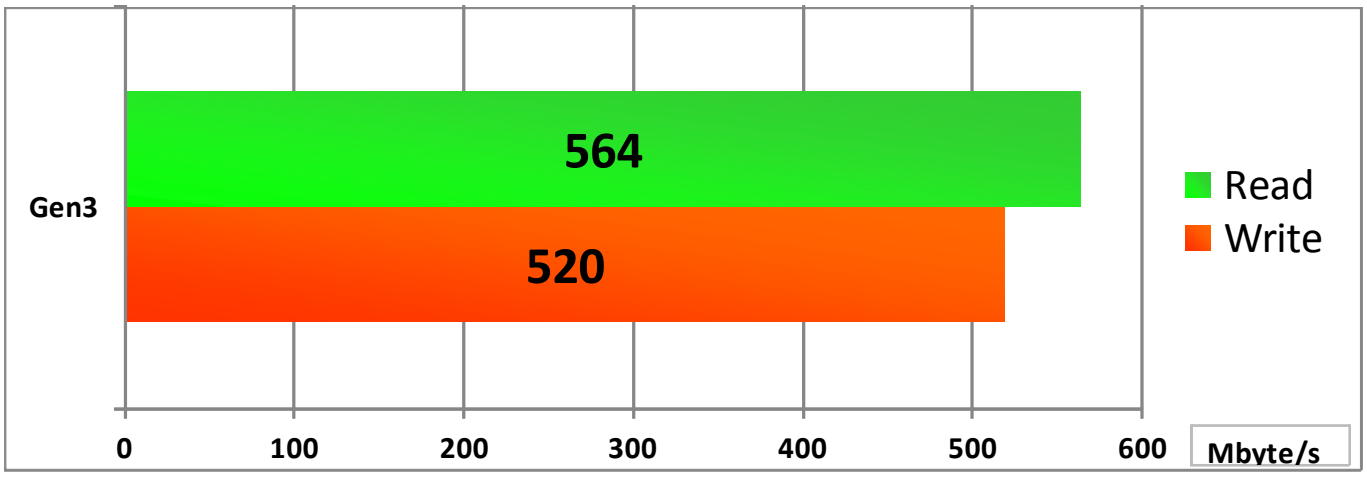

Figure 5 Test Performance of SATA Host IP demo by using Samsung 850 Pro SSD

By using SATA Gen3 on KCU105 board, write performance is about 520 Mbyte/sec and read performance is about 564 Mbyte/sec.

6. Revision History

Revision	Date	Description
1.0	13-Oct-14	Initial Release
1.1	29-Aug-16	Add CPU system for Serial console interface
1.2	9-Nov-16	Add Security erase command
1.3	30-Jan-17	Update signal to dgIF typeS
1.4	1-Aug-17	Add LFSR pattern