



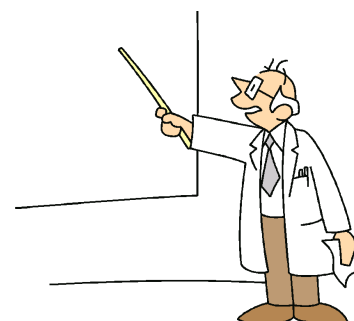
**TOE10G**  
IPcore  
TCP Offloading Engine IP Core

## Ultimate 10GbE network solution!

## Agenda

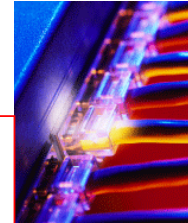
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- **10GbE&TCP/IP Overview**
  - Advantage and Disadvantage of TCP on 10GbE
- **TOE10G-IP core overview**
- **TOE10G-IP core description**
  - Initialization
  - High-speed transmit
  - High-speed reception
- **User I/F, Buffer size parameterization**
- **Reference design**
- **Resource usage and real performance**



# 10GbE Overview

- **What is 10GbE (10Giga-bit Ethernet)?**
  - Industrial standard high-speed network
  - 10Gbps transfer speed
  - Many connection type



**TOE10G-IP is applicable to both Optical Cable and Direct Attach**

Connection Type	Merit	Demerit	Note
Optical Cable	Low latency (100ns) Long distance	Expensive	Needs optical module and cable
Direct Attach	Low cost	Short distance (5-7m maximum)	Direct insertion to SFP+ socket
10GBASE-T	Low cost Popular (RJ-45)	High latency (2us)	Special coding (LDPC)

## 10GbE connection type

# Advantage of TCP/IP on 10GbE

- **Advantage of TCP/IP**
  - Standard Ethernet protocol
  - Guaranteed data reliability
  - Major OS provides protocol stack



- **Disadvantage of TCP/IP**

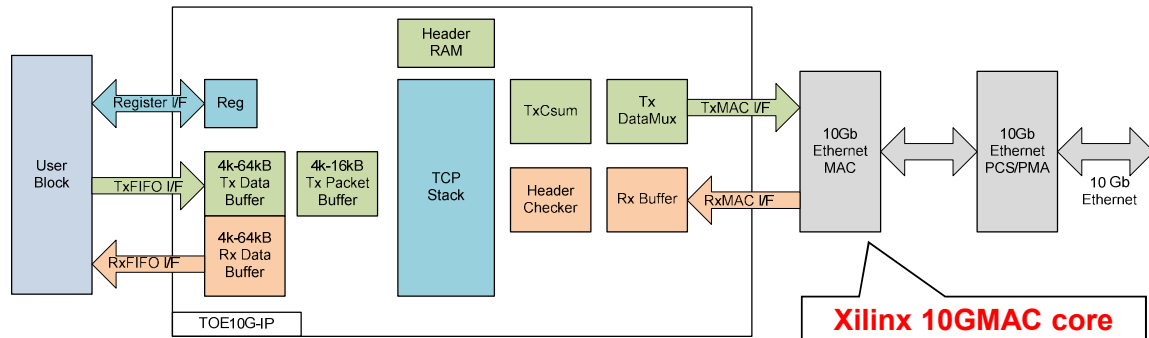
- Heavy CPU load due to complicated TCP process
- Difficult to raise performance(30-40% efficiency)
- Needs expensive high performance CPU



**➡ TOE10G-IP core can provide ideal solution!**

# TOE10G-IP core Overview

- TCP/IP off-loading engine for 10GbE
- Inserts between user logic and Xilinx 10GMAC module
- **Fully hard-wired TCP control for both Tx and Rx**
- **Supports Full Duplex communication**



**TOE10G-IP core block diagram**

# TOE10G-IP core Advantage 1

- **Fully hard-wired TCP/IP protocol control**
  - Possible to build CPU-less network system
  - Zero load for CPU
- **Support all of Tx only, Rx only, and full-duplex**
  - 1200MByte/sec real transfer speed for half-duplex
  - 920MByte/sec real transfer speed for full-duplex
- **Guarantee transfer data reliability**
  - Tx: Automatic retry when No-ACK, Duplicate-ACK, timeout
  - Rx: Automatic ACK control by Sequence number calculation



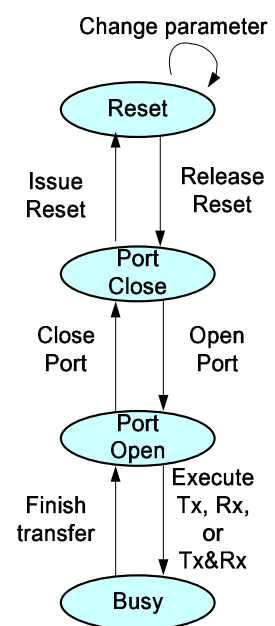
# TOE10G-IP core Advantage 2

- **Selectable data buffer size**
  - Selectable buffer size of memory usage vs. performance
- **Compatible with Xilinx MAC core (EF-DI-10GEMAC)**
  - Direct connection between TOE10G-IP and Xilinx MAC core
- **Many reference design on Xilinx evaluation board**
  - Full Vivado project for standard Xilinx board
  - Free bit-file for evaluation before purchase
  - All source code (except IP-core) in design project



# TOE10G-IP core Operation

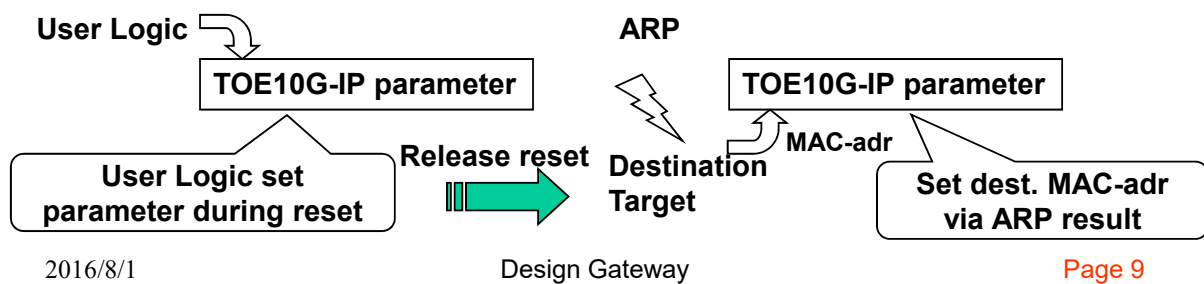
- **Set parameter (IP-adr&MAC-adr, etc) during Reset**
- **Release Reset then initialize including ARP**
- **Idle state after initialization finish, wait command**
- **Port open by either of Active (Client) or Passive (Server) mode**
- **Tx and Rx operates individually (**full-duplex**)**
- **If want change parameter, move to Reset state (transfer/packet length can change except Busy)**



**State Diagram**

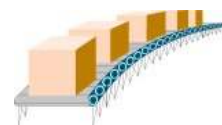
## TOE10G-IP Initialization

- **Set parameter to TOE10G-IP**
  - User logic can set parameter during TOE10G-IP reset
  - Set IP address, MAC address, and Port number
  - Release reset after parameter setting finish
- **TOE10G-IP executes ARP after reset release**
  - Issue ARP to destination target
  - Get MAC-adr of the target via ARP result



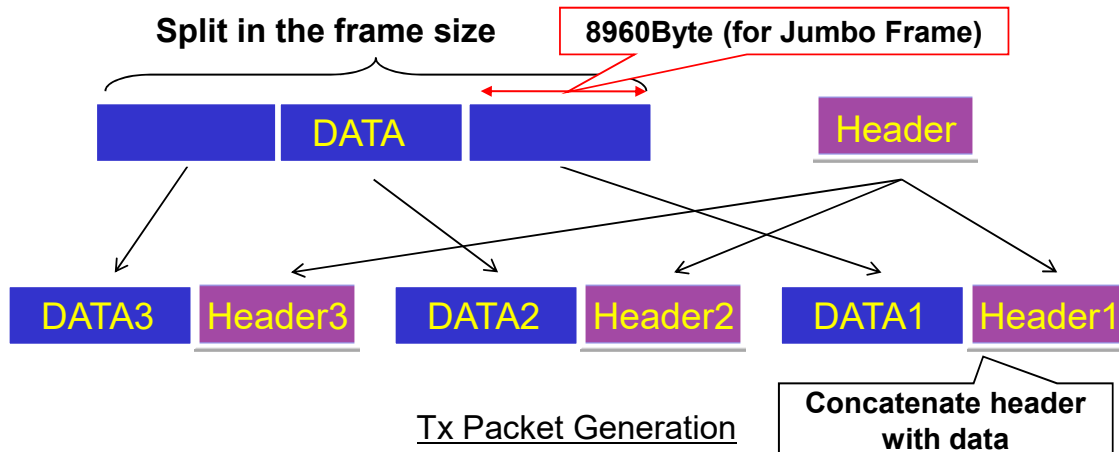
## High-Speed Tx

- **Tx packet generation**
  - User Logic writes Tx data to Tx FIFO
  - Split Tx data in the frame size
  - Concatenate header with Tx data
- **Automatic retransmit function**
  - Check ACK reply from destination
  - Detect No-ACK, Duplicate-ACK, and Timeout
  - Resend same packet by such ACK error detection



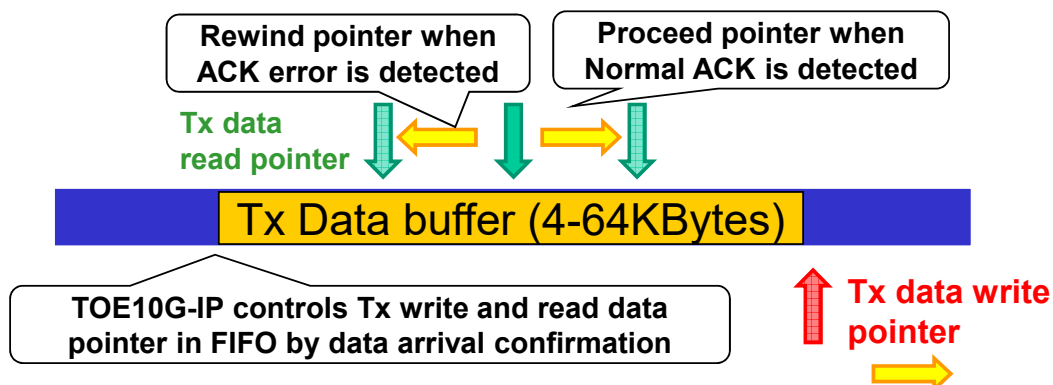
# Tx Packet Generation

- Generate header and concatenate it with Tx data
  - TOE10G-IP splits Tx data in the frame size
  - Generate checksum and sequence number in TOE10G-IP






# Automatic retransmit

- Retransmit function by dedicated FIFO
  - Proceed pointer by normal ACK reception
  - Rewind pointer by illegal ACK reception
  - TOE10G-IP controls pointer and retransmit operation



# High-Speed Rx

- **Rx packet header check** 
  - Ignore packet if destination is not TOE10G-IP or if checksum is wrong
- **Data reordering** 
  - Reorder when sequence number skip is detected
  - Avoid retransmit request for transfer efficiency
  - If reordering is not possible, then send duplicate ACK
- **Duplicate data management** 
  - Check duplicate data in Rx packet
  - Retrieve original data by trimming duplicate data part

# Rx Packet Header Check

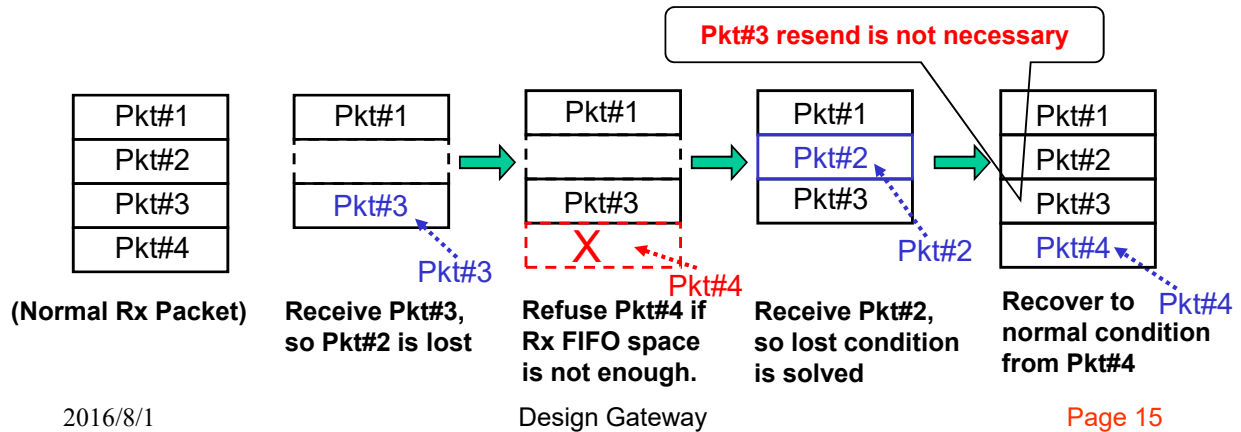
- **Verify header check sum in Rx packet**
  - Also check following condition in TOE10G-IP

Byte Offset	Protocol	Description	Check condition
0-5	ICMP	Destination MAC adr	Match with MAC adr set by SML/SMH register
6-11	ICMP	Source MAC adr	Match with target MAC adr set by ARP
12-13	ICMP	Type	= 0x0800 (IP packet)
14	IP	Version/Header	= 0x45 ( IPv4, IP header len=20 )
20	IP	Flag/Fragment OFS	= b"000000" (no fragment)
23	IP	Protocol Number	= 0x06(TCP packet )
26-29	IP	Source IP adr	Match with IP adr set by DIP register
30-33	IP	Destination IP adr	Match with IP adr set by SIP register
34-35	TCP	Source port number	Match with DPN register or extracted target port number in Passive Open
36-37	TCP	Destination port number	Match with port number set by SPN register
38-41	TCP	Sequence number	Possible value within TOE2-IP core can process this packet

Header check condition in Rx packet

# Data Reordering

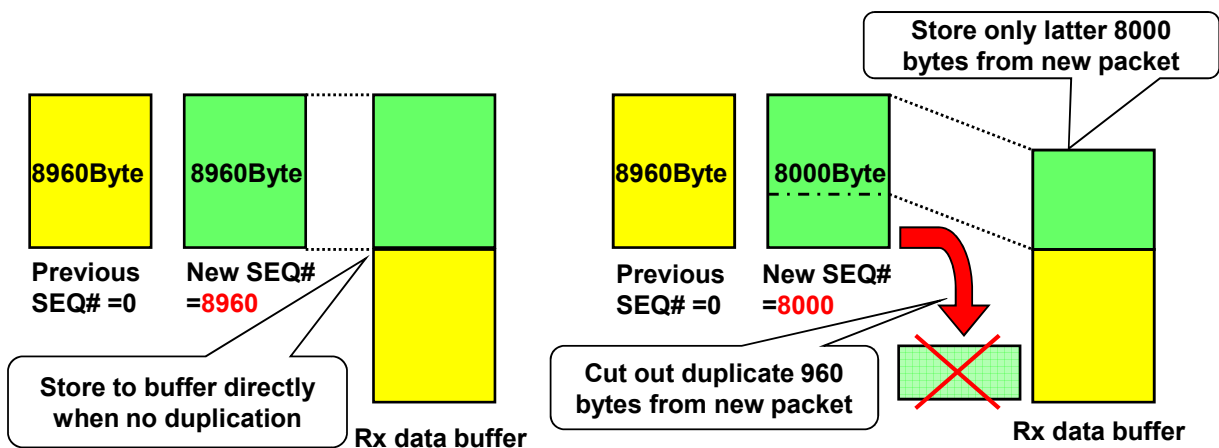
- **Function when SEQ number skip is detected**
  - Not accept any packet other than that can solve lost condition
- **Data reordering function**
  - Recover data contiguous from lost-solved packet
  - Keep performance by suppress resend request



Design Gateway

# Duplicate data trimming

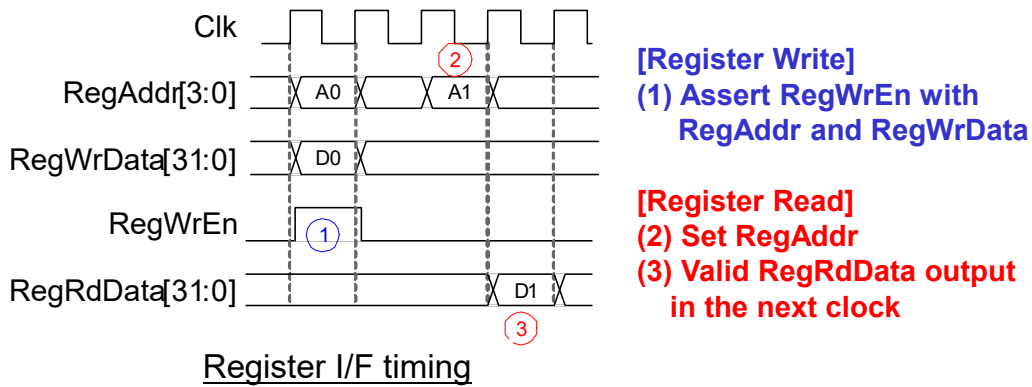
- **Detect data duplication and correct automatically**
  - Detect Rx data duplication by checking sequence number
  - Trim duplicate block and retrieve contiguous data



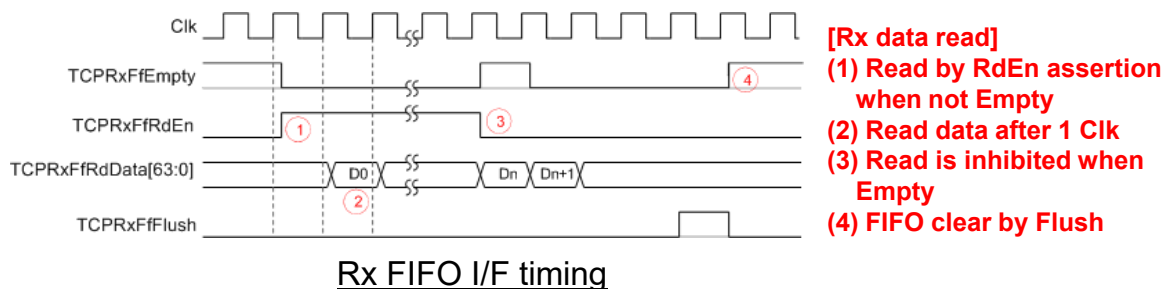
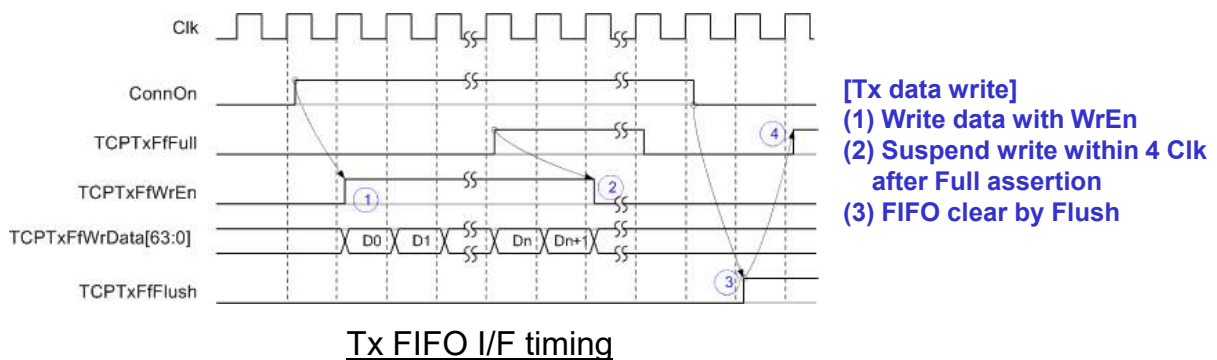


# User Interface (Control)

- 3 types of Register I/F, Tx FIFO I/F, and Rx FIFO I/F
  - Register I/F for initial parameter setting and Tx/Rx command
  - Tx FIFO I/F and Rx FIFO I/F is standard FIFO interface



# User Interface (Data)



# Buffer Capacity

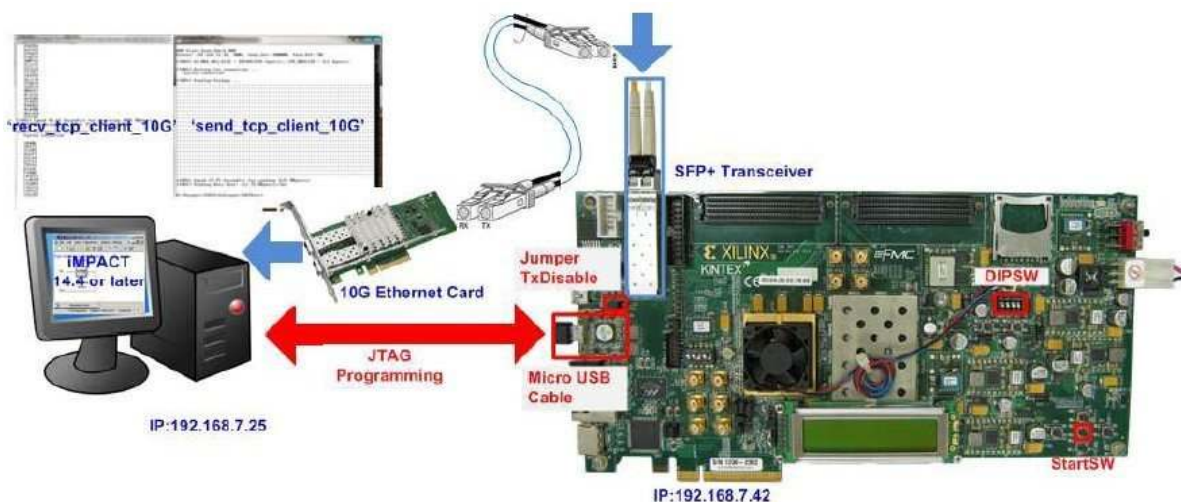
- Parameterized 3 types of data buffer
  - (1) Tx Data Buffer: 4KBytes - 64KBytes
  - (2) Tx Packet Buffer: 4KBytes - 16KBytes
  - (3) Rx Data Buffer: 4KBytes - 64KBytes
- User can optimize resource usage and performance

Generic Name	Range	Description
TxBufBitWidth	9-13	Set Tx data buffer size in address bit width When set to 9, size is 4KBytes, when 13, 64Kbytes for example.
TxPacBitWidth	9-11	Set Tx packet buffer size in address bit width When set to 9, size is 4Kbytes, when 11, 16KBytes for example
RxBufBitWidth	9-13	Set Rx data buffer size in address bit width When set to 9, size is 4KBytes, when 13, 64KBytes for example.

Buffer size is selectable by parameterization

# Free Bit File for Evaluation

- Bit file for evaluation with Xilinx standard board
  - Ready for VC707/KC705
  - Support both Half-Duplex and Full-Duplex operation
  - Measure transfer speed performance and data reliability

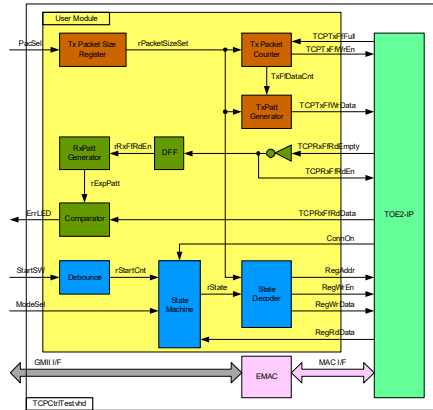


# Reference Design Overview

- **Vivado design project for real operation**
  - All source code (except IP-core) included in full project
  - Both half-duplex and full-duplex design in IP-core package



Vivado/EDK project in package



Reference design block diagram

# Effective Development on Ref. Design

- **Vivado project is attached to the package**
- **Full source code (VHDL) except IP core**
- **Can save user system development duration**
  - Confirm real board operation by original reference design.
  - Then modify a little to approach final user product
  - Check real operation in each modification step.



**Short-term development is possible without big turn back**

# Resource Usage

- TOE10G-IP core standalone resource usage
  - Condition = Maximum buffer setting  
(TxDataBuf=RxDataBuf=64KB, TxPacketBuf=16KB)



Family	Target Device	Fmax (MHz)	Slice Regs	Slice LUTs	Slices <sup>1</sup>	IOB <sup>2</sup>	RAMB36E1	Design Tools
Kintex-7	XC7K325T-2FFG900	156.25	3009	3287	1227	363	38	Vivado2014.1
Virtex-7	XC7VX485T-2FFG1761	156.25	3009	3287	1219	363	38	Vivado2014.1

## TOE10G-IP core standalone compilation result

This result is based on maximum buffer size setting.  
User can save memory resource by smaller buffer size setting

# Transmission Performance

```

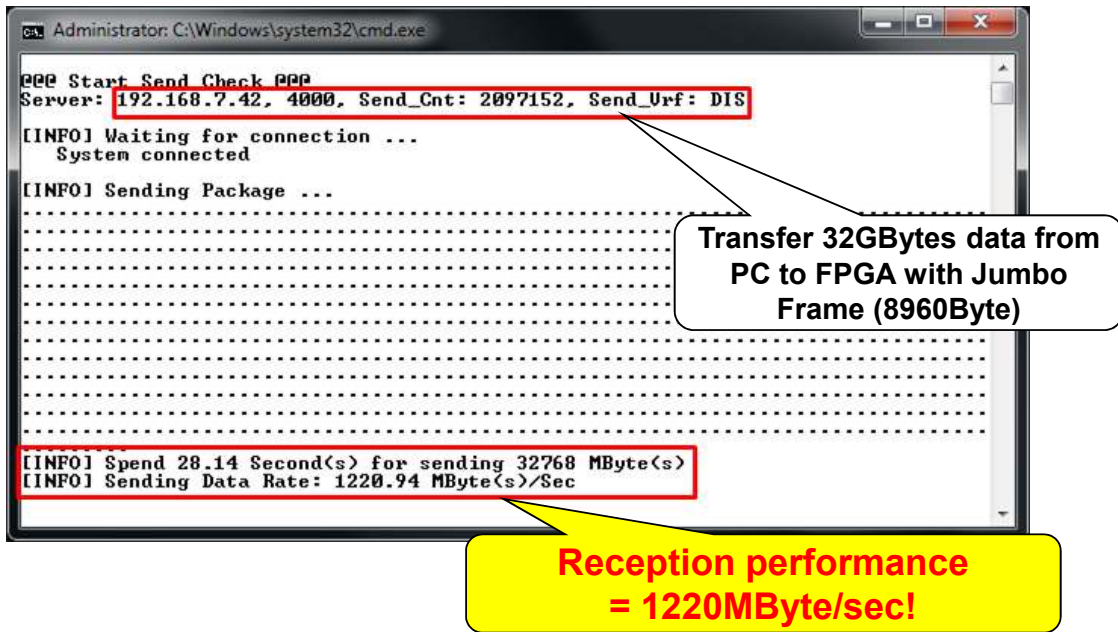
Administrator: C:\Windows\system32\cmd.exe - recv_tcp_client_10G 192.168.7.42 4000 8960
C:\SW>recv_tcp_client_10G 192.168.7.42 4000 8960
@@@ Start Receive Check @@@
Server: 192.168.7.42, 4000, Recv_Len: 8960
[INFO] Waiting for connection ...
System connected
1152384 kByte(s)
2368581 kByte(s)
3584385 kByte(s)
4794379 kByte(s)
|
28141 MByte(s)
29082 MByte(s)
30275 MByte(s)
31464 MByte(s)
32657 MByte(s)
[INFO] Spend 28.63 Second(s) for receiving 32767 MByte(s)
[INFO] Receiving Data Rate: 1200.30 MByte(s)/Sec
[INFO] Waiting for connection ...
System connected
1216285 kByte(s)
2433620 kByte(s)
    
```

Transfer 32GBytes data from  
FPGA to PC with Jumbo  
Frame (8960Byte)

**Transmission performance  
= 1200MByte/sec!**

## Transmission (FPGA to PC) performance result using KC705

# Reception Performance



Reception (PC to FPGA) performance result using KC705

# TOE10G-IP Application Market

- Data transfer in FA market
  - Medical video processing system
  - Sensor data logger measurement instrument
- Storage system using TCP such as NAS, iSCSI
  - TOE10G-IP replaces CPU for hard TCP processing
- Network product
  - Network printer for high speed print data download
  - Network camera for high speed video data upload



## Low-cost Solution

- SFP+ Direct Attach Cable
  - FPGA transceiver directly connects with 10GbE bus
  - Copper cable provides low cost solution
  - Cable length is limited (about 7m at maximum)



10Gtek® for Netgear AXC763, 10Gb/s SFP+ DAC  
Passive, 3m

by 10Gtek

★★★★★ 17 customer reviews | 6 answered questions

Price: \$57.99

Sale: \$36.99 & FREE Shipping on orders over \$49. Details

You Save: \$21.00 (36%)

Want it Tuesday, Aug. 2? Order within 15 hrs 31 mins and choose One-Day Shipping at checkout. Details

In Stock.

Sold by 10Gtek and Fulfilled by Amazon.

Length: 3-Meter(10ft)

Market Price example (3m cable at Amazon.com)

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## For more detail

- Detailed documents available on the web site.
  - [http://www.dgway.com/TOE10G-IP\\_X\\_E.html](http://www.dgway.com/TOE10G-IP_X_E.html)
- Contact
  - Design Gateway Co., Ltd.
  - E-mail : [ip-sales@design-gateway.com](mailto:ip-sales@design-gateway.com)
  - FAX : +66-2-261-2290



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# Revision History

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Rev.	Date	Description
1.0E	March 11, 2016	English version initial release
1.1E	March 13, 2016	Added direct attach cable information
1.2E	August 1, 2016	Corrected some wrong description