# TOE1G-IP two-port (HW) Instruction

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# TOE1G-IP two-port (HW) Instruction

Rev1.0 4-Jul-23

This document describes the instruction to run two-port demo by using TOE1G-IP and CPU. The data is transferred by using TCP/IP protocol on high speed session or low speed session via 1 Gb Ethernet. User sets test mode and test parameters for TOE1G-IP through NiosII command shell. Similar to TOE1G-IP demo, high speed session is run with the test applications on PC, named "tcpdatatest.exe" and "tcp_client_txrx_40G.exe". Low speed session is run with "Ping" command. More details of high-speed session are described in TOE1G-IP demo document.

https://dgway.com/products/IP/TOE1G-IP/dg_toe1gip_cpu_refdesign_intel_en.pdf
https://dgway.com/products/IP/TOE1G-IP/dg_toe1gip_cpu_instruction_intel_en.pdf

## 1 Environment Setup

As shown in Figure 1-1, please prepare following test environment for running two-port demo.

1) FPGA Development board (Cyclone10GX board)
2) PC with 1 Gigabit Ethernet support
3) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
4) Micro USB cable for programming FPGA between FPGA Development board and PC
5) QuartusII Programmer for programming FPGA and NiosII command shell, installed on PC
6) "tcpdatatest.exe" and "tcp_client_txrx_40G.exe" which are test application provided by Design Gateway, installed on PC

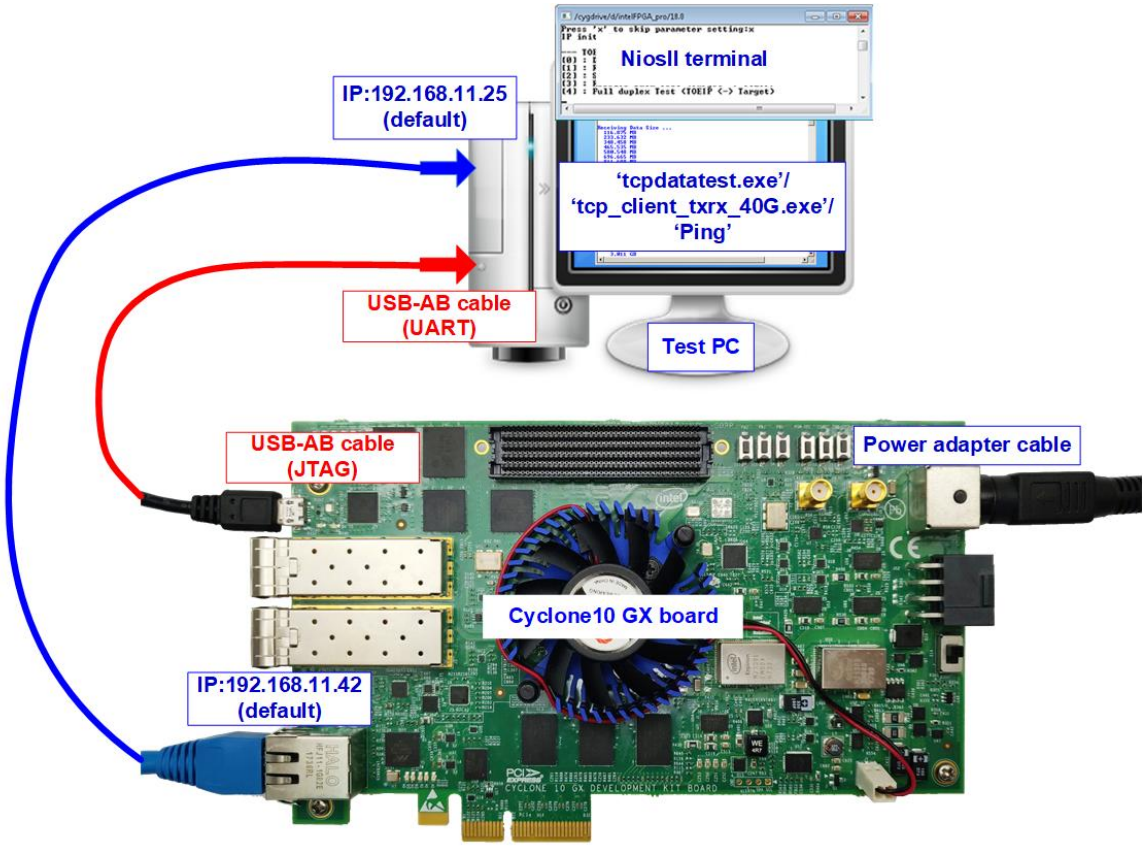



Figure 1-1 Demo Environment Setup on Cyclone10 Gx board

# 2 PC Setup

Before running demo, network setting on PC is required. The example to set the network is described as follows.

## 2.1 IP Setting

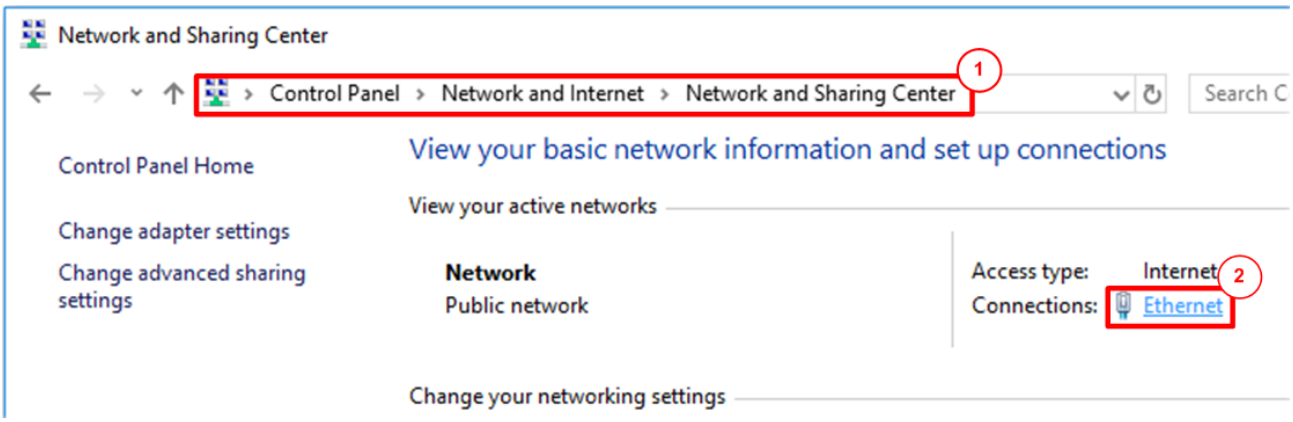



Figure 2-1 IPv4 setting

1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
2) Click Gigabit Ethernet icon which is used to connect with FPGA board.

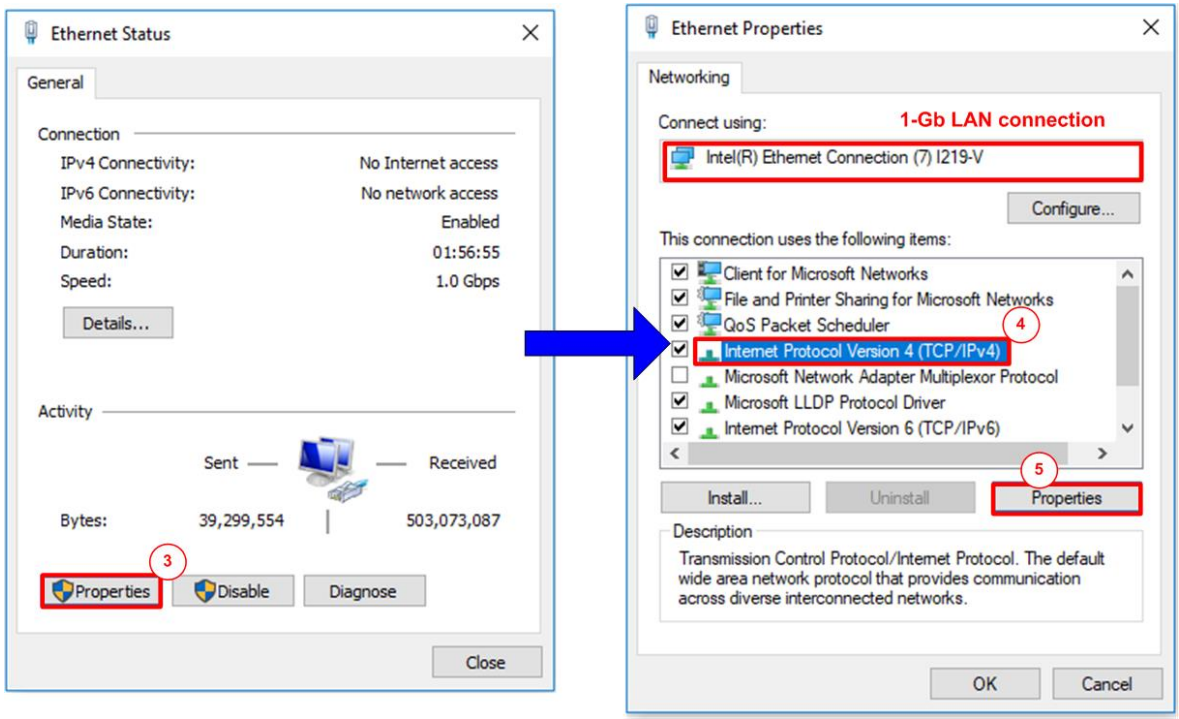



Figure 2-2 Select IP address setting menu

3) Click Properties button in Ethernet Status window.
4) Select “TCP/IPv4”.
5) Click Properties button in Ethernet Properties.

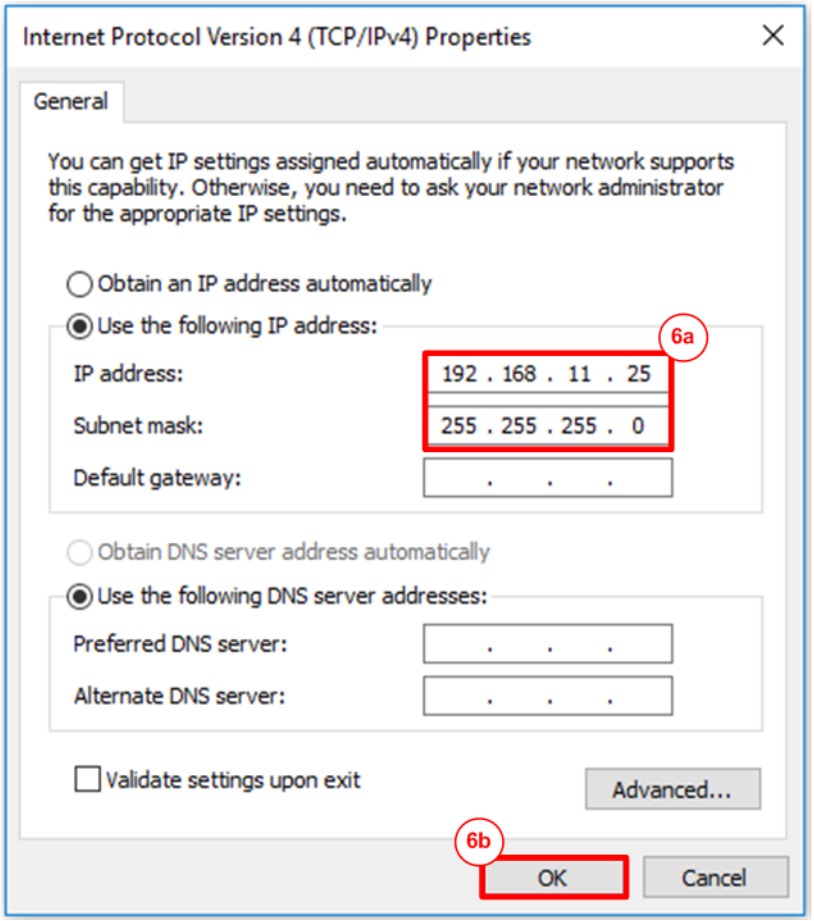



Figure 2-3 Set IP address

6) Set IP address = 192.168.11.25 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.

## 2.2 Speed and Frame Setting

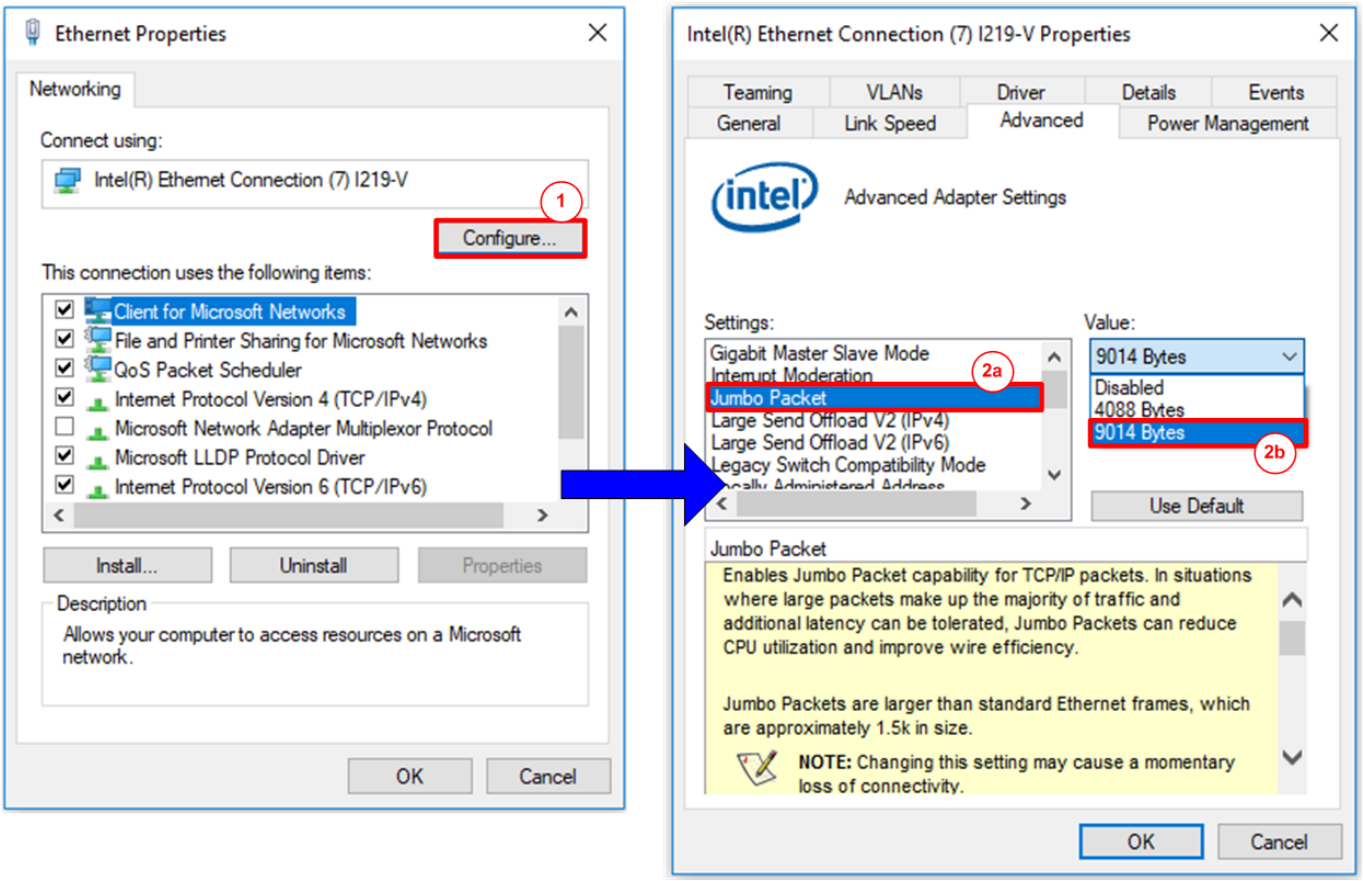



Figure 2-4 Jumbo frame setting

1) Click Configure button in Ethernet Properties window.
2) On Advanced Tab, select “Jumbo Packet” and then set Value to “9014 Bytes” for Jumbo Frame support.

3) On Link Speed, select “1 Gbps Full Duplex” and click OK button, as shown in Figure 2-5.

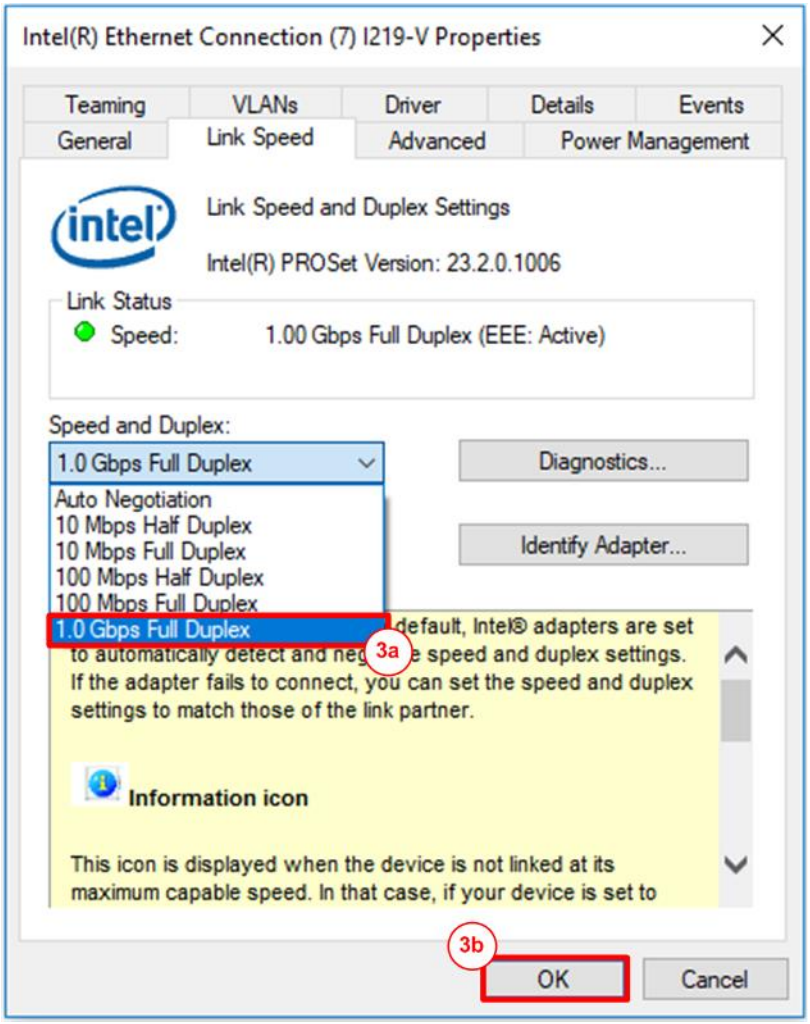



Figure 2-5 Set link speed = 1 Gbps

## 2.3 Power Option Setting

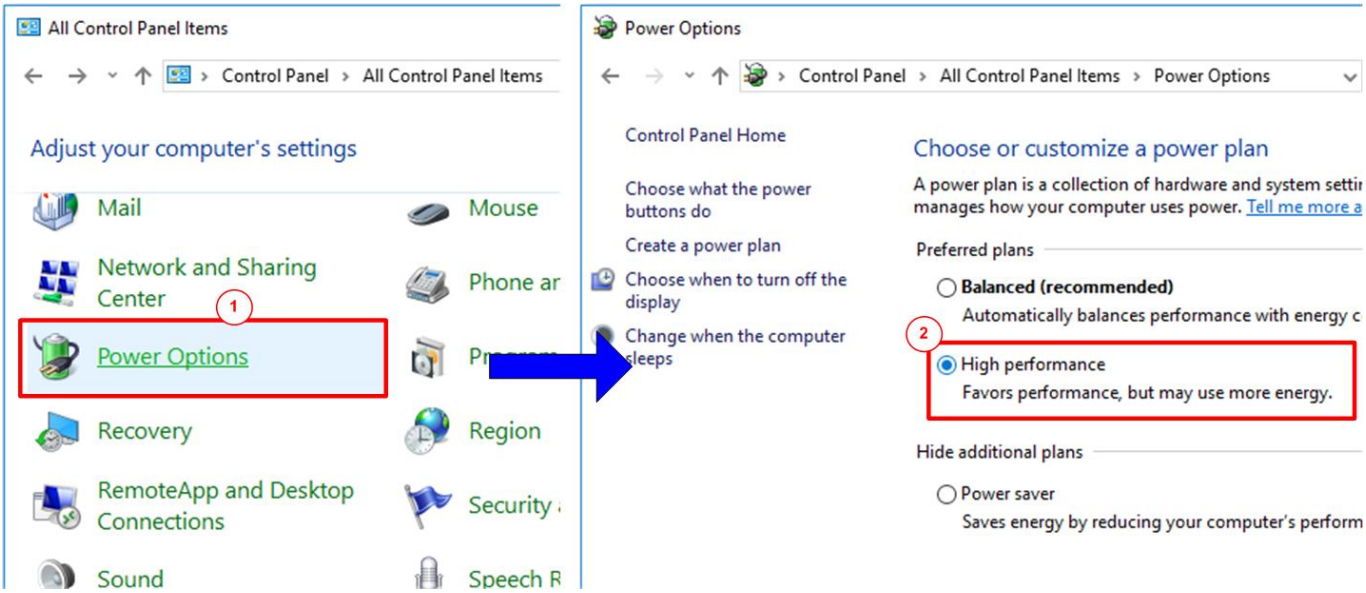



Figure 2-6 Power options

1) Open Control Panel and select Power Options.
2) Select High performance plan.

# 3 FPGA board setup

1) Power off system and connect power supply to FPGA development board
2) Connect micro USB cable from FPGA board to PC.
3) Connect CAT5e or CAT6 cable between RJ45 on FPGA board to PC.
4) Power on system.

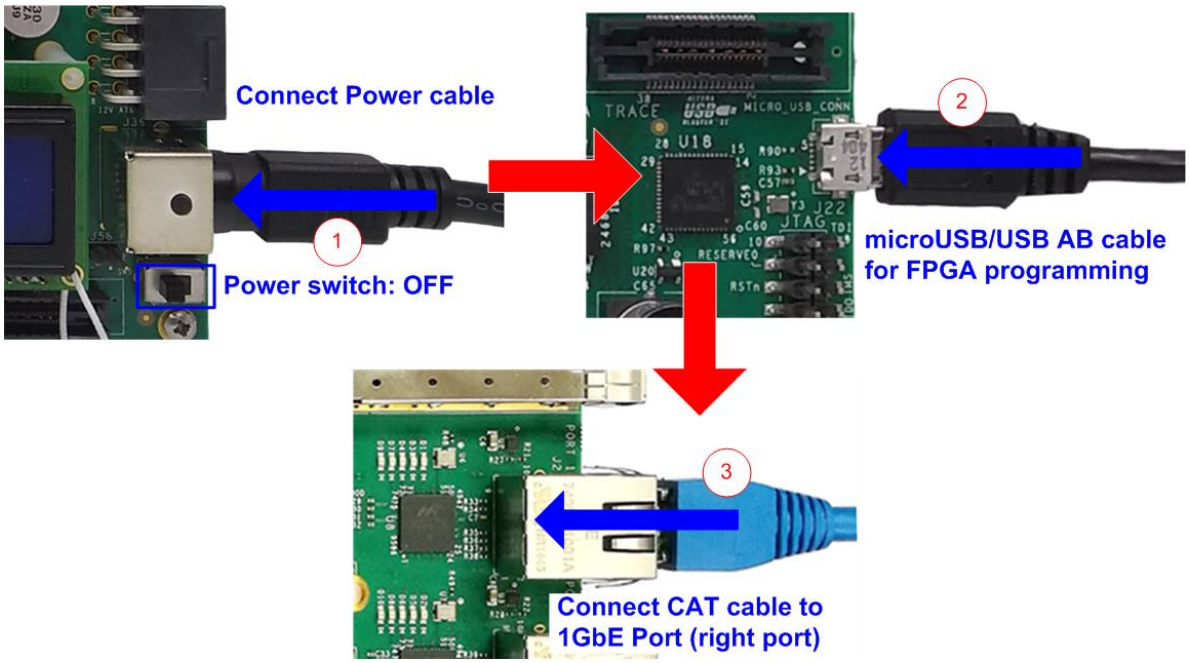



Figure 3-1 Power cable, USB cable, and Ethernet connection

5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
   a) Click “Hardware Setup…” to select USB-BlasterII [USB-1].
   b) Click “Auto Detect” and select FPGA device.
   c) Select FPGA device icon.
   d) Click “Change File” button, select SOF file in pop-up window, and click “open” button
   e) Check “program”
   f) Click “Start” button to program FPGA
   g) Wait until Progress status is equal to 100%

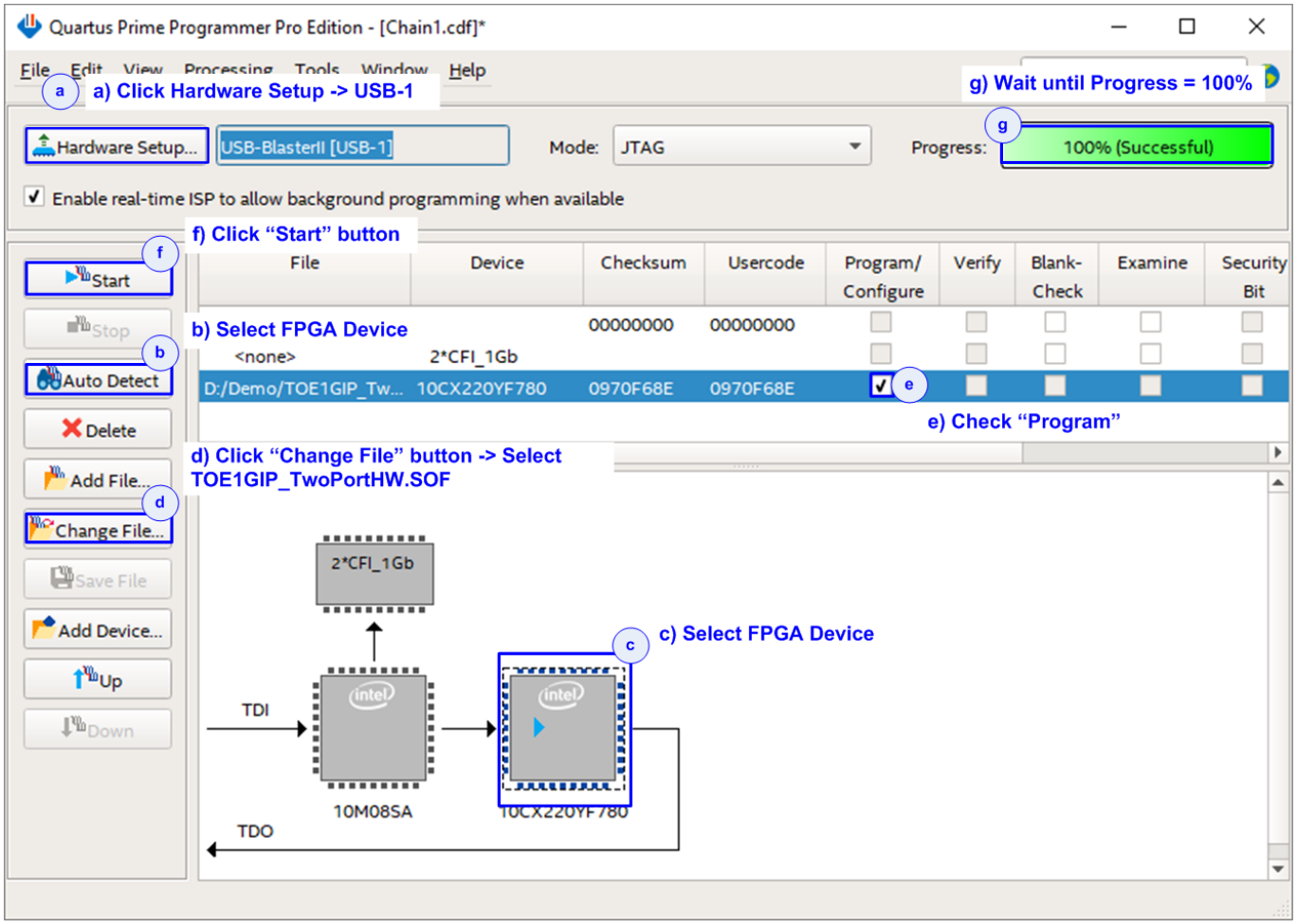



Figure 3-2 FPGA Programmer

6) Open NiosII command shell.
   a) Type “nios2-terminal”.
   b) Enter ‘0’ to initialize TOE1G-IP in client mode (ask PC MAC address by sending ARP request).
   c) Default parameter in client mode is displayed on NiosII command shell.

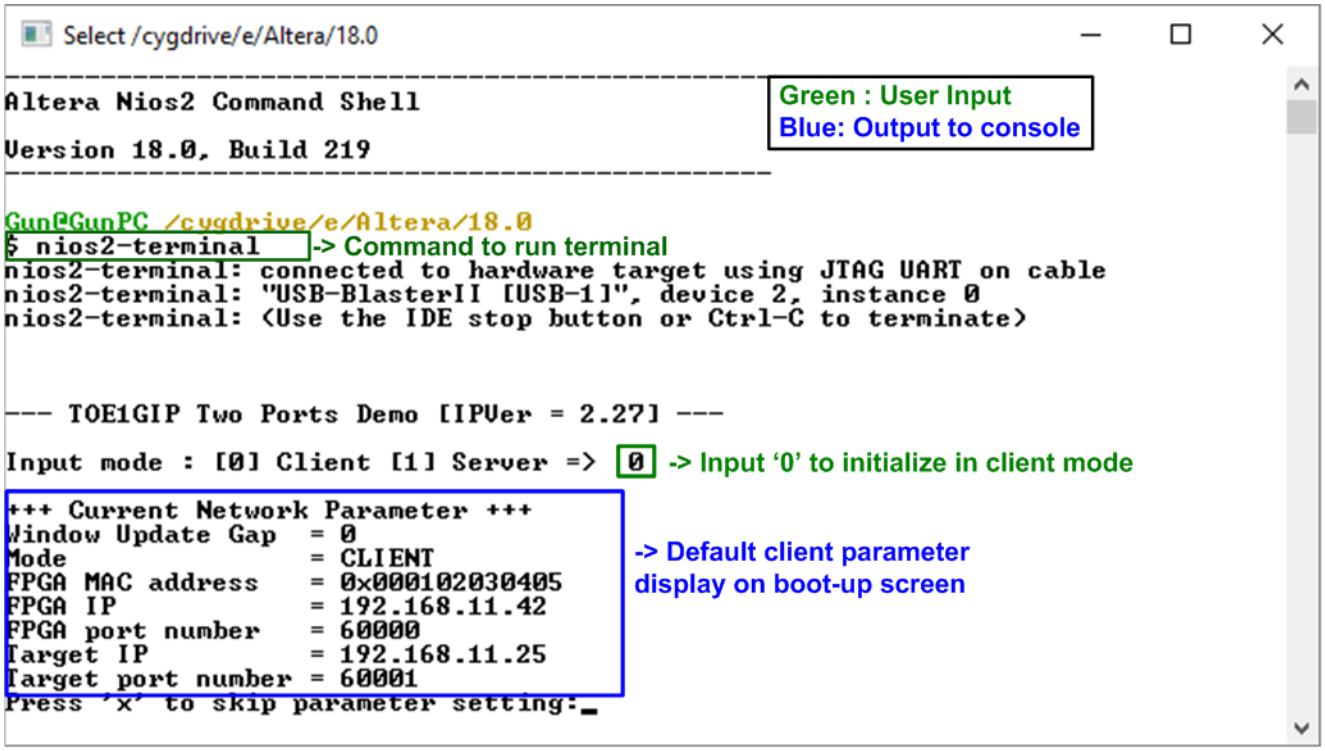



Figure 3-3 Message after system boot-up

7) User enters ‘x’ to skip parameter setting and use default parameters for system initialization, as shown in Figure 3-4. When user enters other keys, the menu to change parameter is displayed. The example to change parameter is shown in topic 4.2

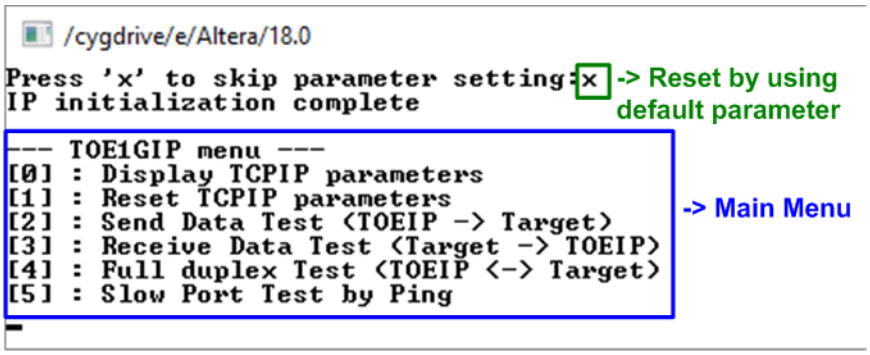



Figure 3-4 System initialization

*Note: Transfer performance depends on Test PC resource in Test platform*

# 4 Main Menu

## 4.1 Display current parameter

Select '0' to check current parameter in the demo. There are seven parameters displayed on NiosII command shell

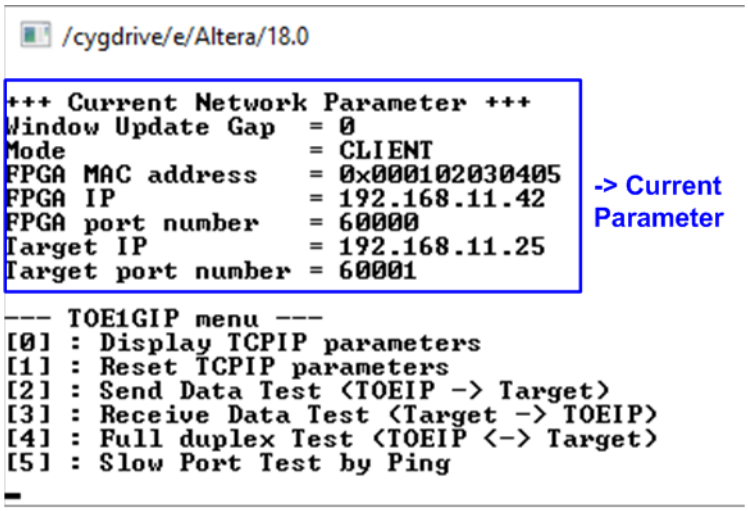



Figure 4-1 Display current parameter

1) Window Update Gap : Threshold value to transmit window update packet. Valid value is 0x00 – 0x3F (0-63). The unit size of threshold value is 1 Kbyte. Default value is 0 (disable window update feature).
2) Mode : Mode of TOE1G-IP to act as server or client. To run with PC, please input '0' to initialization the IP in client mode.
3) FPGA MAC address : 48-bit hex value to be MAC address of FPGA. Default value is 0x000102030405.
4) Target IP : IP address of destination device (1 Gb Ethernet on PC) to transfer 1 Gb Ethernet data. Default value is 192.168.11.25.
5) FPGA IP : IP address of FPGA. Default value is 192.168.11.42.
   *Note: This value is used to be server IP address parameter for test application on PC.*
6) Target port number : Port number of destination device to transfer 1 Gb Ethernet data. Default value is 60001.
7) FPGA port number : Port number of FPGA. Default value is 60000.
   *Note: This value is used to be server port for test application on PC.*

To change some parameters, user can set by using menu [1].

## 4.2 Reset TOE1G-IP

Select '1' to reset the IP and change IP parameters. This menu is used to change IP parameters. After user selects this menu, the current parameters are displayed. User enters 'x' to use same parameters or other keys to change some parameters. There are seven parameters which can be modified by user. When user enters invalid value such as 'n', the parameter does not change. After setting parameters completely, IP is reset. More details of each parameter are described as follows.

1) Window Update Gap : Threshold value to transmit window update packet. Valid value is 0x00 – 0x3F (0-63). The unit size of threshold value is 1 Kbyte. Default value is 0 (disable window update feature).
2) Mode : '0' to initialization the IP as client mode.
3) FPGA MAC address : 12-digit of hex value. Add "0x" as a prefix to input as hex value.
4) FPGA IP address : A set of four decimal digits is separated by ".". The valid range of each decimal digit is 0-255.
5) FPGA port number : Valid range is 0-65535.
6) Target IP address : A set of four decimals like FPGA IP address. This value is IP address of Test PC.
7) Target port number : Valid range is 0-65535.

After finishing all parameter assignment, new parameters are displayed on NiosII command shell. Next, reset signal is sent to the IP to load new parameters. Finally, "IP initialization complete" is shown after IP completes initialization process, as shown in Figure 4-2.

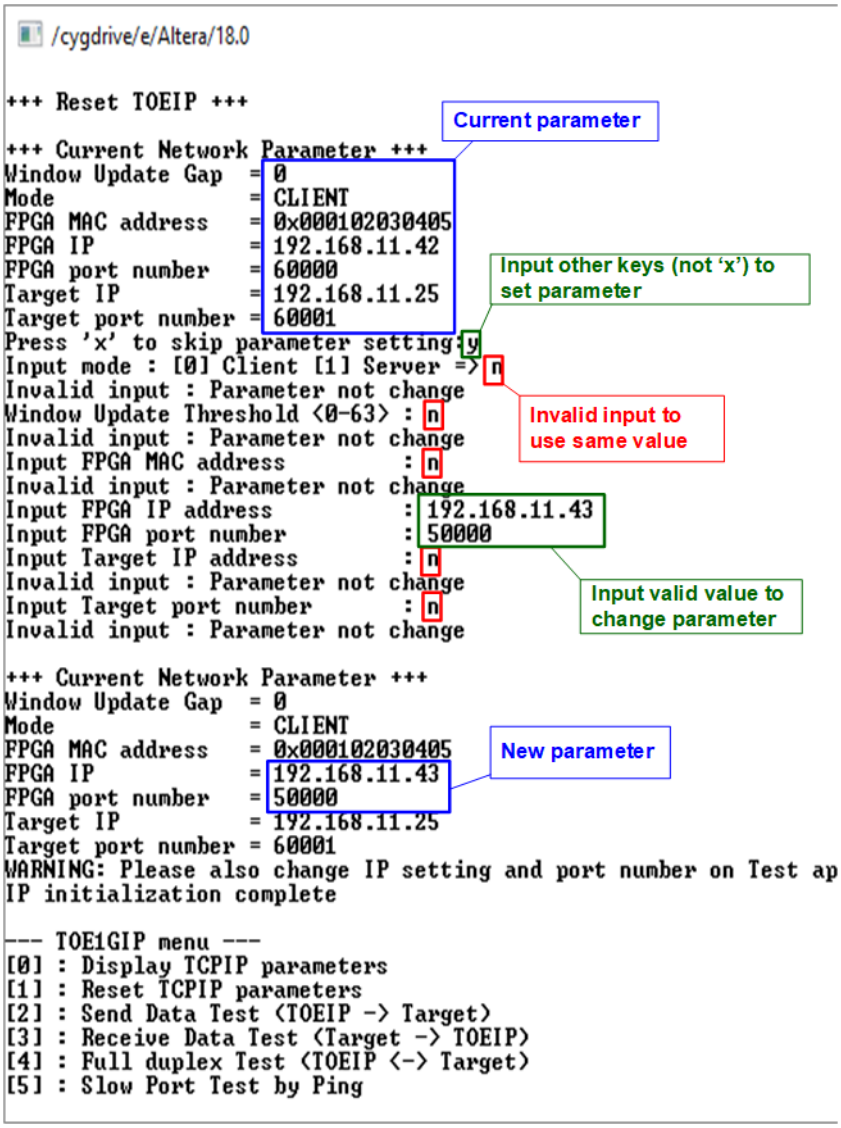



Figure 4-2 Change IP parameter result

### 4.3 Send Data Test

To transfer data from FPGA to PC, select '2' to run send data test on FPGA and prepare "tcpdatatest.exe" on PC to receive data. User sets test parameters on FPGA for sending data through NiosII command shell. On PC, user sets test parameters of "tcpdatatest" through command prompt. The step to run the test is described as follows.

1) On NiosII command shell, input three parameters in send data test.
   a) Input transfer size: Unit of transfer size is byte. Valid value is 1 - 0xFFFF_FFFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
   b) Input packet size: Unit of packet size is byte. Valid value is 1 – 8960. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
   c) Input Mode: Mode of FPGA to transfer data. Set '1' to run as server mode.
2) When all inputs are valid, the recommended parameters to run test application on PC and "Wait Open connection …" are displayed.
3) On Command prompt, user runs application by using the recommended parameters. There are six parameters for "tcpdatatest".
   >> tcpdatatest [Mode] [Dir] [ServerIP] [ServerPort] [Bytelen] [Pattern]
   a) Mode : Set 'c' to run Test PC as a client
   b) Dir : Set 'r' to receive test data from FPGA
   c) Server IP : Set the same value as IP address of FPGA
   d) Server por t: Set the same value as port number of FPGA
   e) Bytelen : Set the same value as "Input transfer size" of step 1a)
   f) Pattern : '1'-enable data verification, '0'-disable data verification
4) After running test application, the port is created. Current transfer size is displayed on NiosII command shell and Command prompt every second. "Send data complete" is displayed on NiosII command shell after all data are sent.
5) FPGA closes the connection. Finally, total transfer size and performance are displayed on NiosII command shell and Command prompt.

Figure 4-3 shows the example of send data test when using non-jumbo frame size. The left window is NiosII command shell on FPGA operating as server and the right window is Command prompt on PC operating as client.

Figure 4-4 shows the example of send data test when using jumbo frame size.

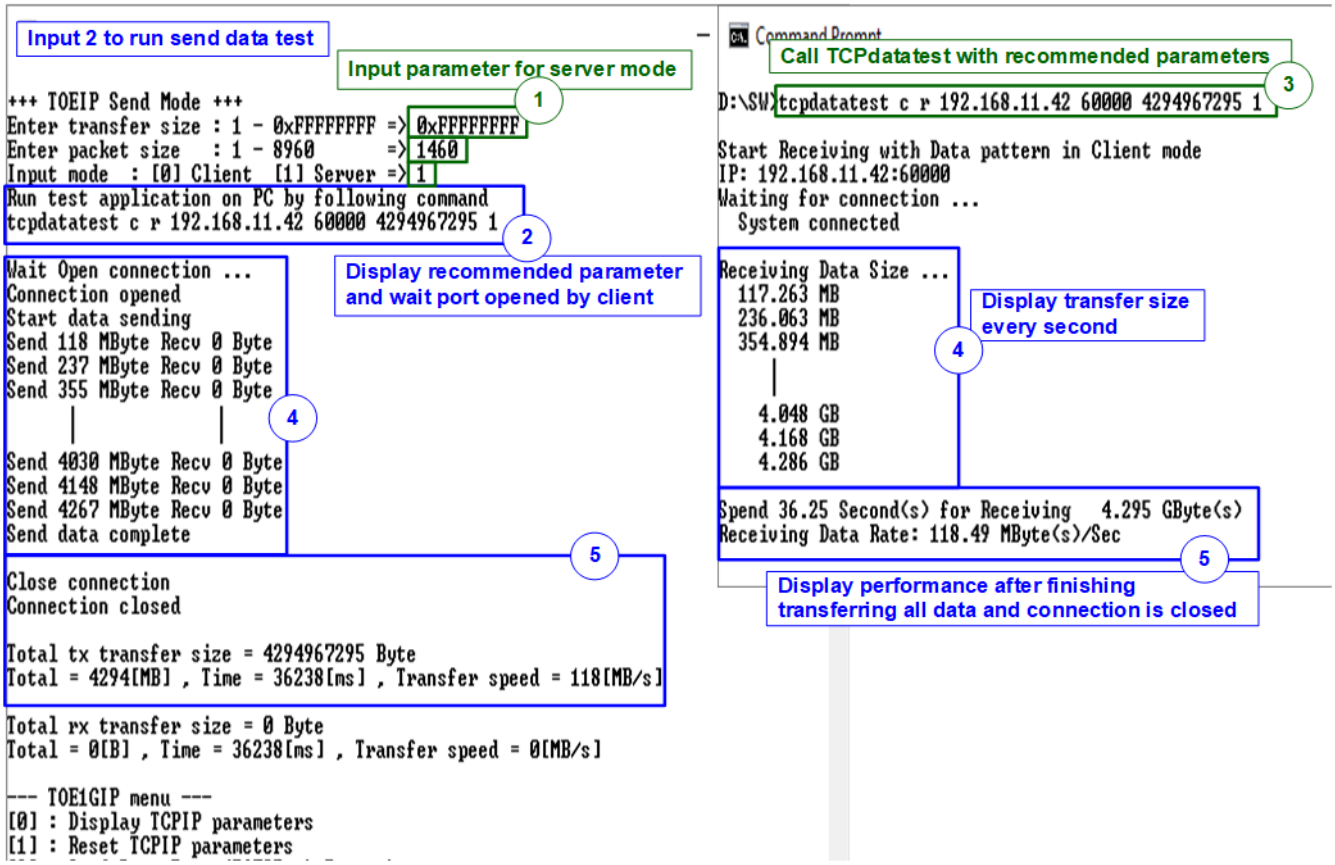



Figure 4-3 Send data test by using non-jumbo frame

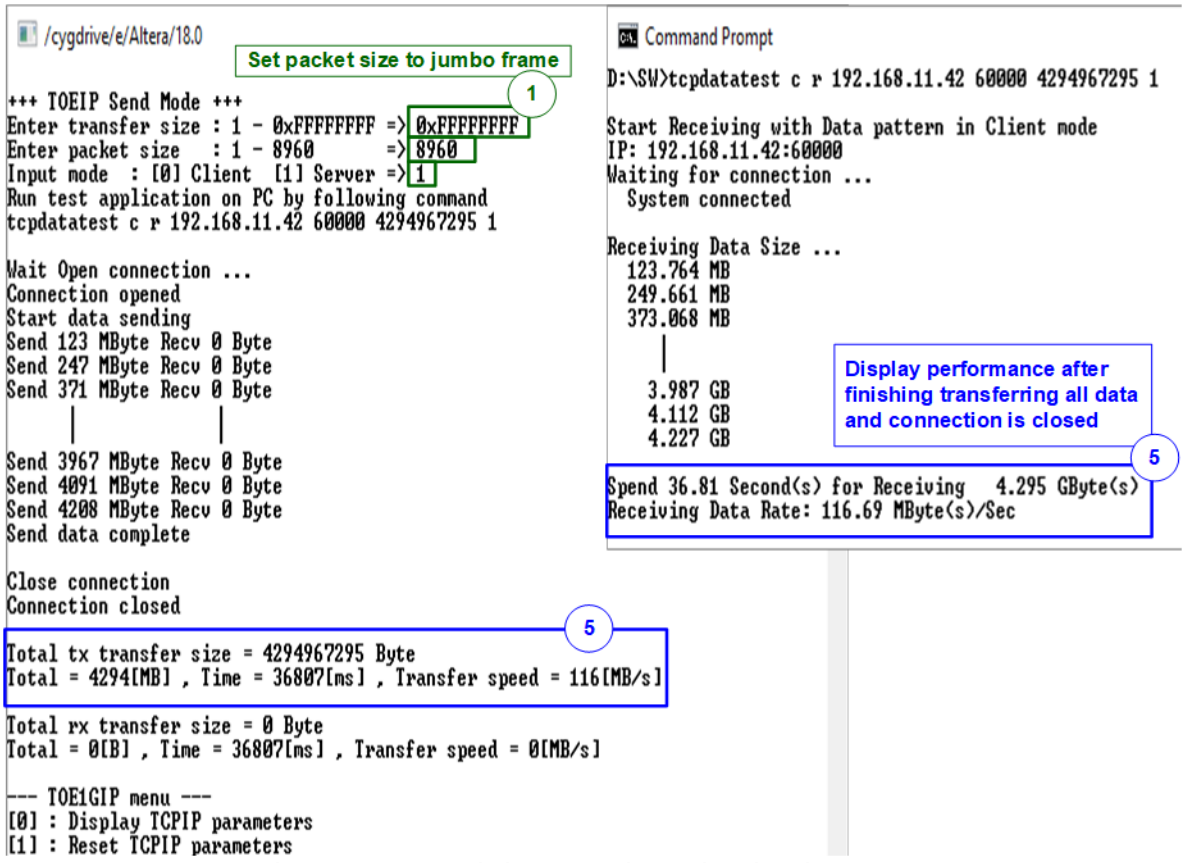



Figure 4-4 Send data test by using jumbo frame

When the input is invalid, “Out-of-range input”/”Invalid input” is displayed and the operation is cancelled, as shown in Figure 4-5 - Figure 4-7.

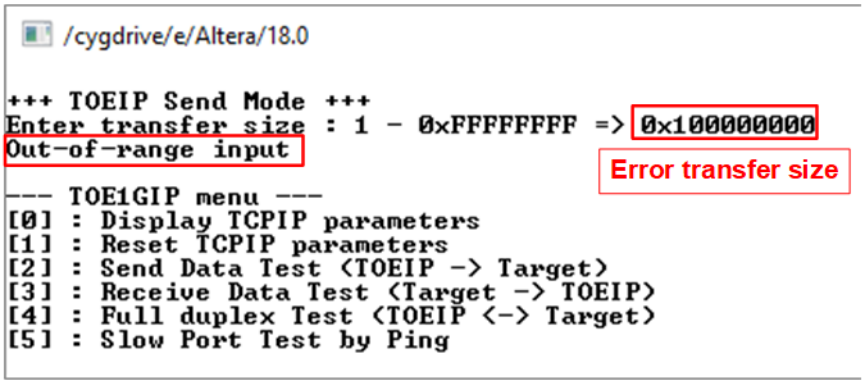



Figure 4-5 Error from invalid transfer size

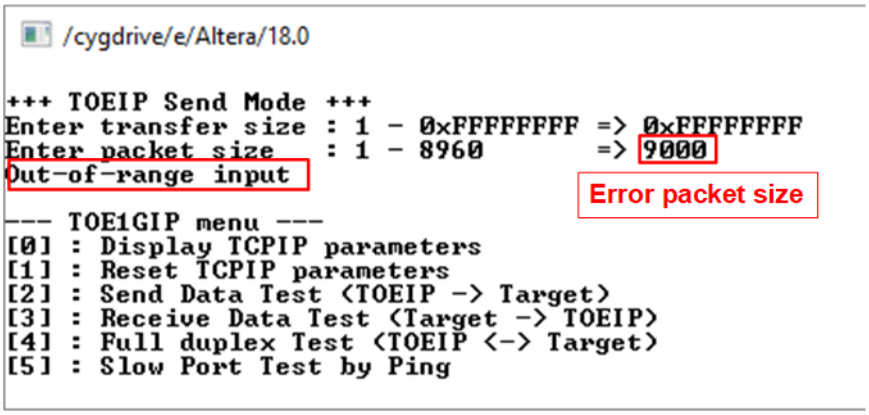



Figure 4-6 Error from invalid packet size

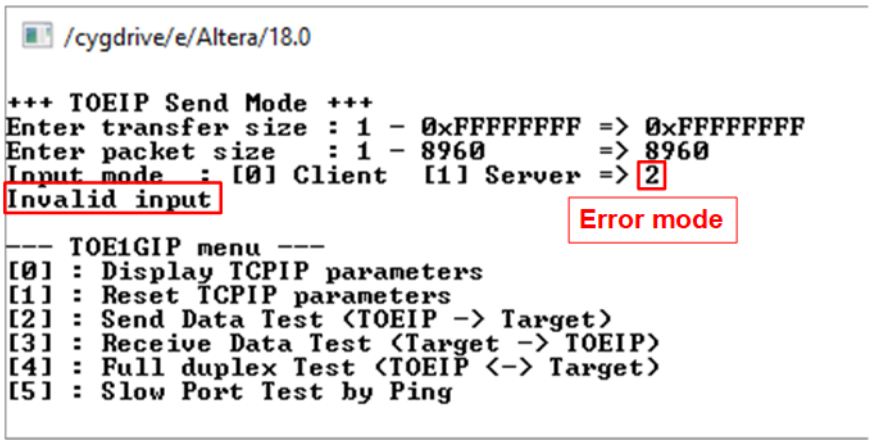



Figure 4-7 Error from invalid mode

### 4.4 Receive Data Test

To transfer data from PC to FPGA, select '3' to run receive data test on FPGA and prepare "tcpdatatest.exe" on PC to send data. User sets test parameters on FPGA for receiving data through NiosII command shell. On PC, user sets test parameters of "tcpdatatest" to send data through Command prompt. The step to run the test is described as follows.

1) On NiosII command shell, set three parameters under receive data test menu.
   a) Input transfer size: Unit of transfer size is byte. Valid value is 1 - 0xFFFF_FFFF. The input is decimal unit when the input is only digit number. User can add "0x" as a prefix for hexadecimal input.
   b) Input data verification mode: '0'-disable data verification, '1'-enable data verification sent from PC.
   c) Input Mode: Mode of FPGA to transfer data. Set '1' to run server mode.
2) When all inputs are valid, the recommended parameters to run test application on PC are displayed. After that, "Wait Open connection …" is displayed.
3) On Command prompt, user runs application by using the recommended parameters. There are six parameters for "tcpdatatest".
   >> tcpdatatest [Mode] [Dir] [ServerIP] [ServerPort] [Bytelen] [Pattern]
   a) Mode : Set 'c' to run Test PC as a client
   b) Dir : Set 't' to send test data to FPGA
   c) Server IP : Set the same value as IP address of FPGA
   d) Server port : Set the same value as port number of FPGA
   e) Bytelen : Set the same value as "Input transfer size" of step 1a)
   f) Pattern : Set the same value as "Input data verification mode" of step 1b). Select '0' to send dummy data or '1' to send incremental data.
4) After running test application, the port is created. Current transfer size is displayed on NiosII command shell and Command prompt every second.
5) "Connection closed" and "Receive data completed" are displayed on NiosII command shell after PC completes to send all data and closes the connection. Finally, total transfer size and performance are displayed on NiosII command shell and Command prompt.

Figure 4-8 shows the example of receive data test when disable data verification mode on FPGA and send dummy data by PC. The left window is test result on NiosII command shell while the right window is test result on Command prompt.
Figure 4-9 shows the example of receive data test when enable data verification mode on FPGA and send incremental data by PC.

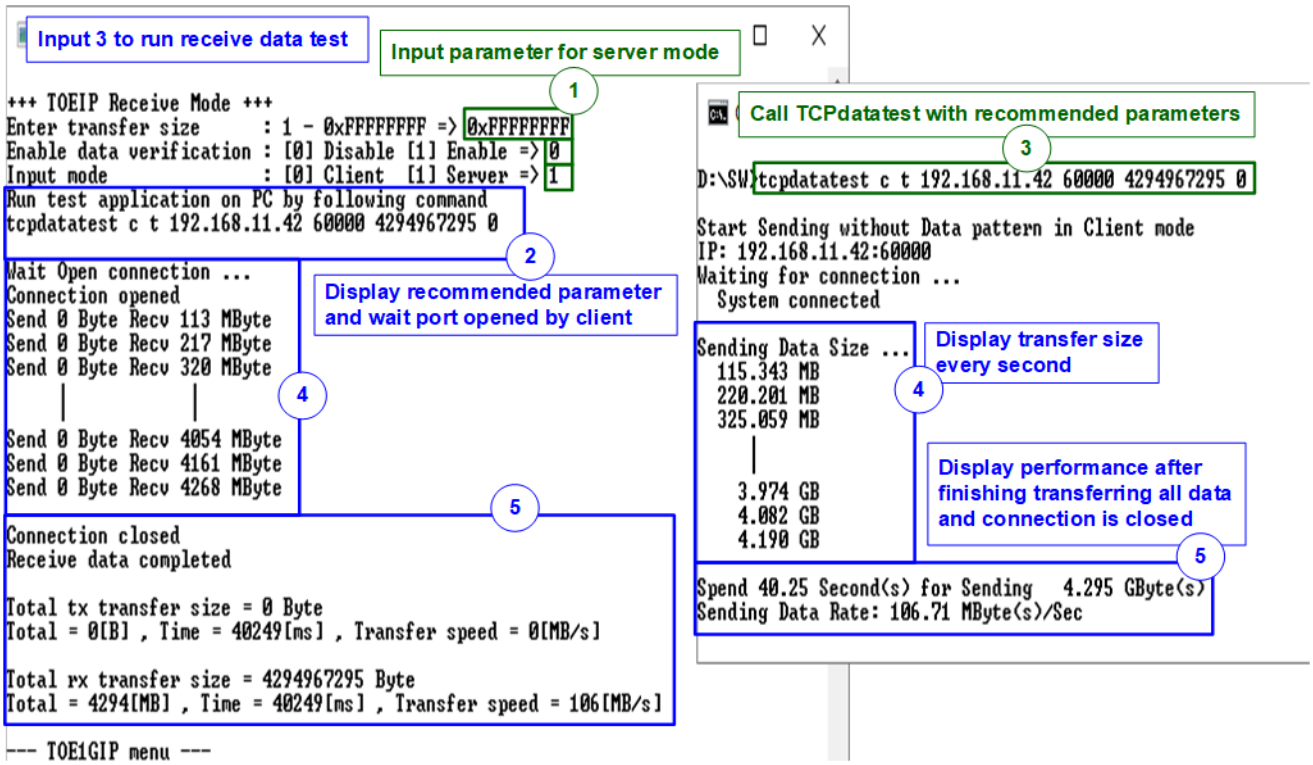



Figure 4-8 Receive data test without data verification

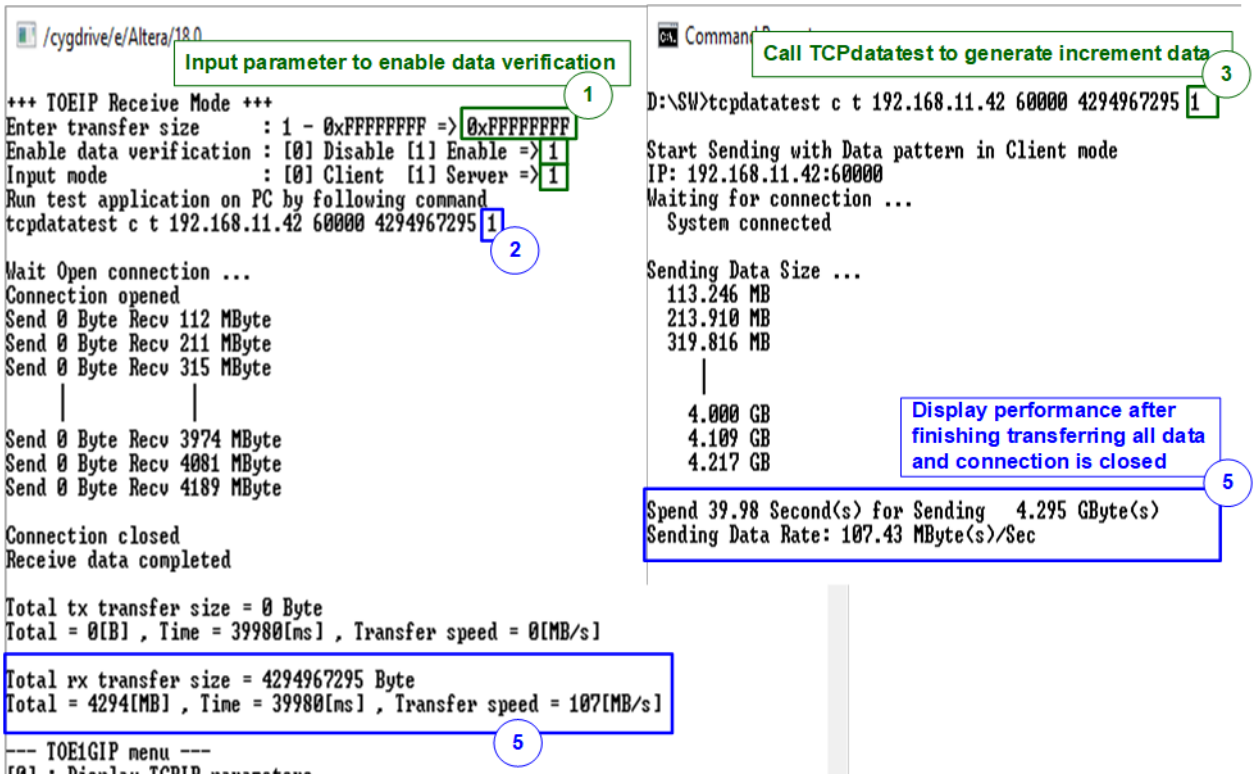



Figure 4-9 Receive data test when enable data verification

Figure 4-10 shows the example of error when data verification is failed. In the example, the error is caused from mismatch verification mode value. FPGA enables data verification while "tcpdatatest" sends dummy data. The error message is displayed on NiosII command shell.

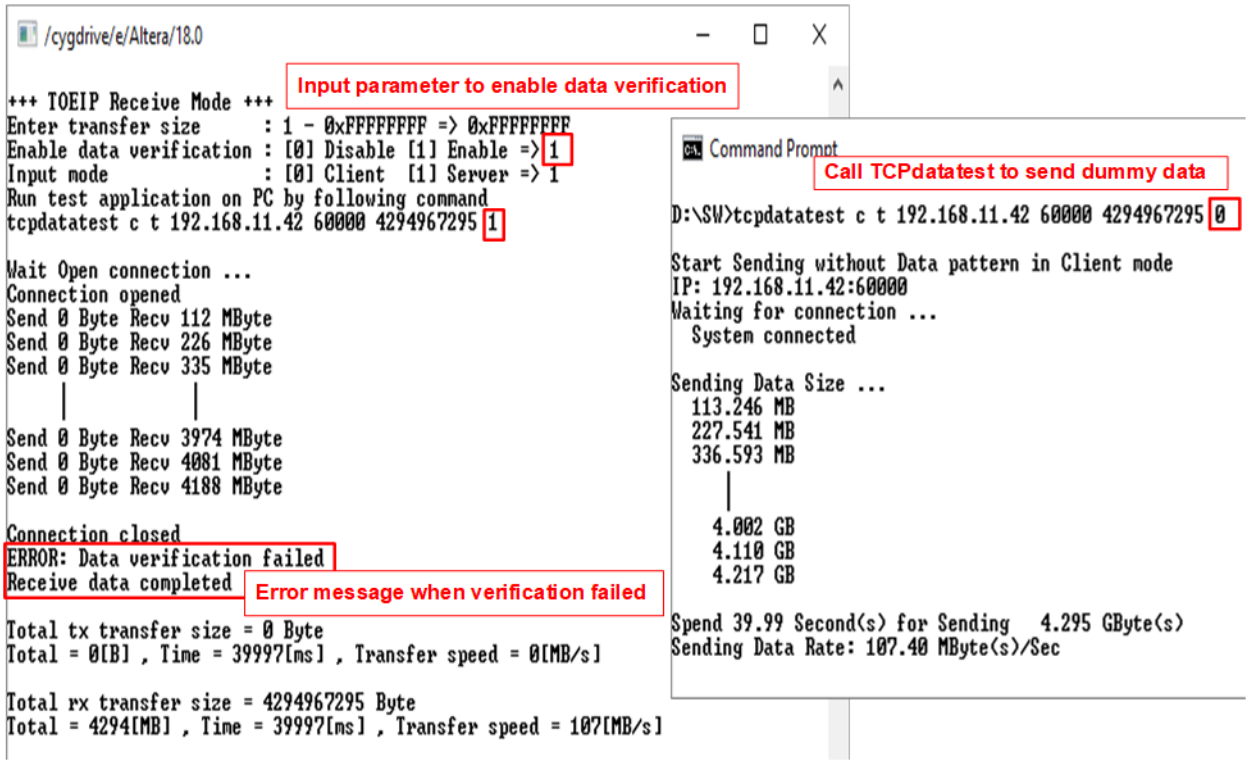



Figure 4-10 Receive data test when data verification is failed

## 4.5 Full duplex Test

Select ‘4’ to run full duplex test to transfer data between FPGA and PC in both directions at the same time. User sets test parameters on FPGA through NiosII command shell and test parameters on PC through Command prompt. The step to run the test is described as follows.

1) On NiosII command shell, set four parameters under full duplex test menu.
   a) Input transfer size: Unit of transfer size is byte. Valid value is 1-0xFFFF_FFFF. The input is decimal unit when the input is only digit number. User can add “0x” as a prefix for hexadecimal input. This value must be equal to total transfer size setting on test application.
   b) Input packet size: Unit of packet size is byte. Valid value is 1 – 8960. The input is decimal unit when the input is only digit number. User can add “0x” as a prefix for hexadecimal input.
   c) Input data verification mode: ‘0’-disable data verification, ‘1’-enable data verification.
   d) Input Mode: Mode of FPGA to transfer data. Sett ‘1’ to run as server mode.
2) When all inputs are valid, the recommended parameters to run test application on PC are displayed. After that, “Wait Open connection …” is displayed.
3) On Command prompt, user runs application by using the recommended parameters. There are four parameters for “tcp_client_txrx_40G”.
   >> tcp_client_txrx_40G [ServerIP] [ServerPort] [ByteLen] [Verification]
   a) Server IP : Set the same value as IP address of FPGA
   b) Server port : Set the same value as port number of FPGA
   c) ByteLen : Total transfer size in byte unit.
      Set the same value as “Input transfer size” of step 1a).
   d) Verification : Set the same value as “Input data verification mode” of step 1b).
      ‘0’-send dummy data and disable data verification,
      ‘1’-send incremental data and enable data verification.
4) After running test application, the port is created. During transferring data, current transfer size is displayed on NiosII command shell and Command prompt every second.
5) “Send data complete” is displayed on NiosII command shell after it finishes sending and receiving all data. After that, the connection is closed. Finally, total transfer size and performance are displayed on NiosII command shell and Command prompt.
   Step 4) – 5) is repeated as forever loop until user cancels the operation by pressing “Ctrl+C” on Command prompt and pressing any key(s) on NiosII command shell.

As shown in Figure 4-11 and Figure 4-12, transfer performance when running full duplex without data verification is better than running with data verification. The left window is the test result on NiosII command shell while the right window is the test result on Command prompt.

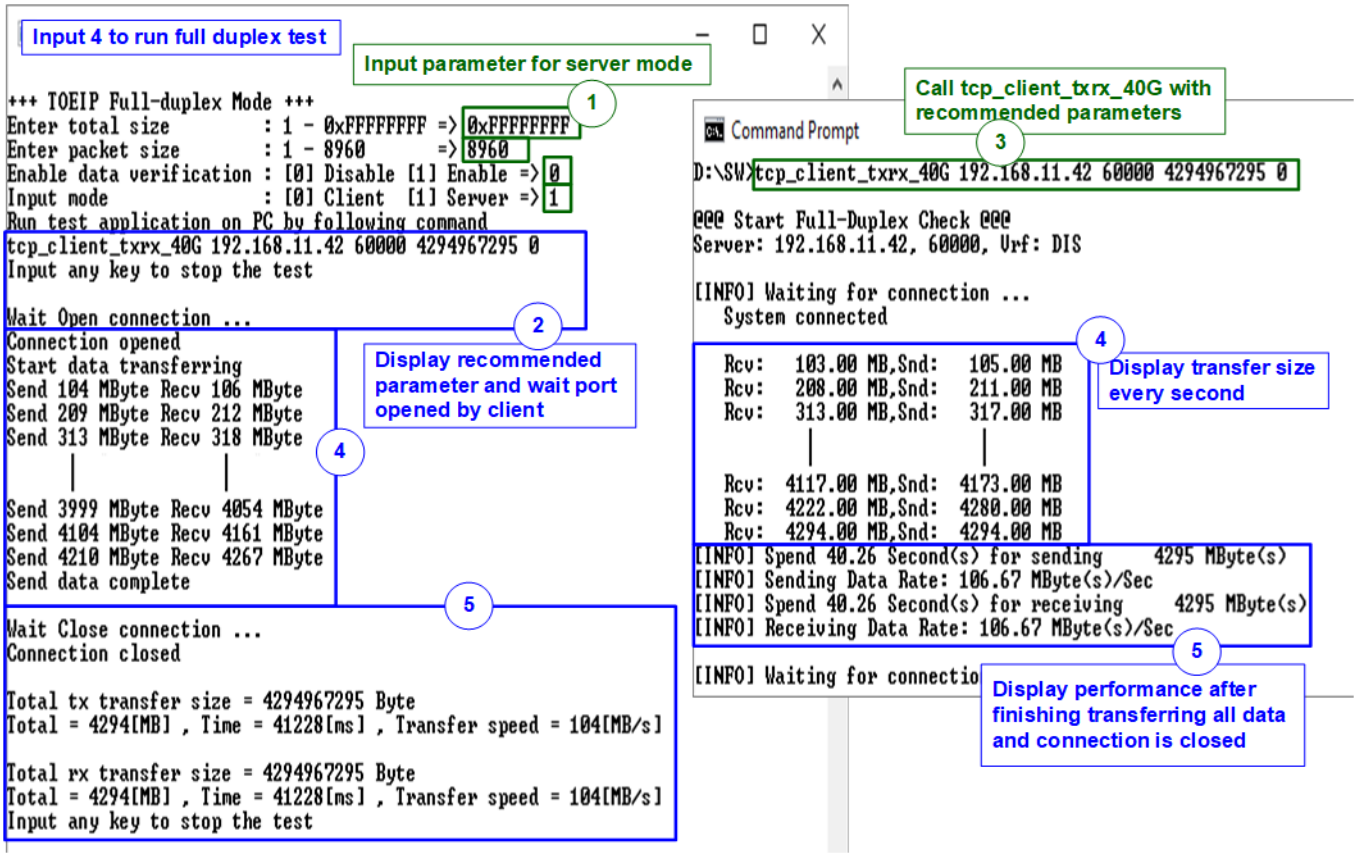
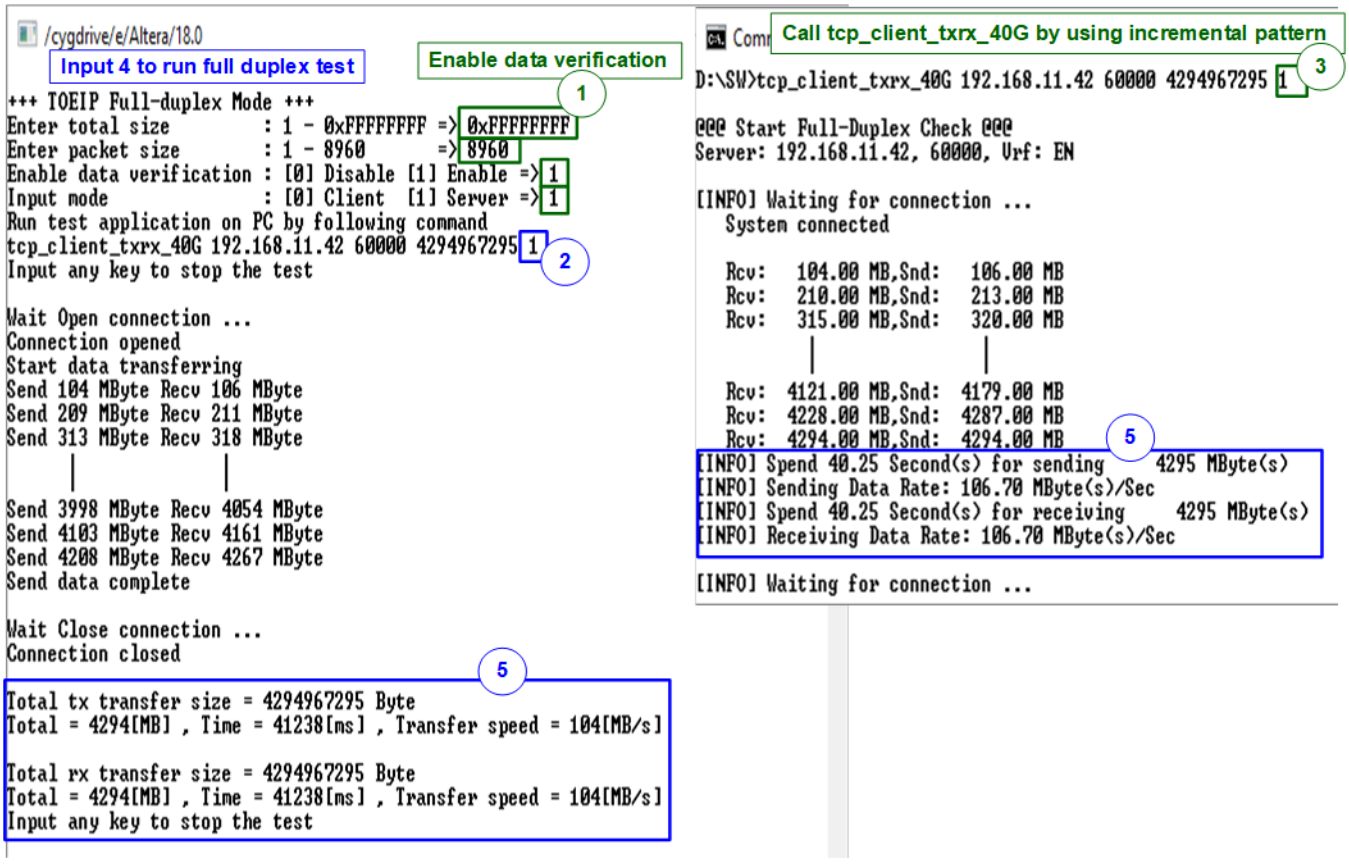



Figure 4-11 Full duplex test without data verification




c

Figure 4-12 Full duplex test with data verification

## 4.6 Slow Port Test by Ping

Select '5' to run Ping request command with PC. After selecting this menu, "Please start run Ping command on PC" message is displayed on the console. After that, user can type "ping <FPGA board IP address>" command on Command prompt to star "Ping" command test, as shown in Figure 4-14.

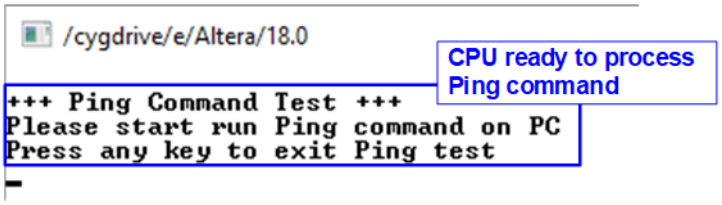



Figure 4-13 Result from Slow Port Test by Ping

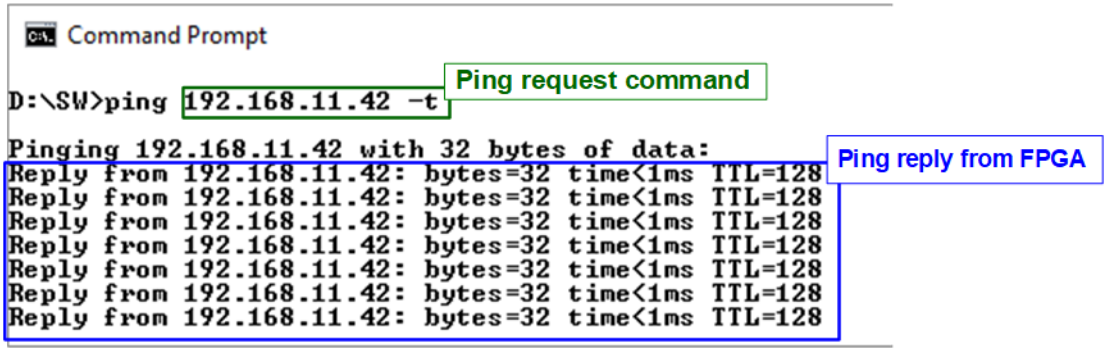



Figure 4-14 Ping command result on PC

User can exit this menu by pressing any key(s) to the console. After that, main menu is displayed as shown in Figure 4-15.

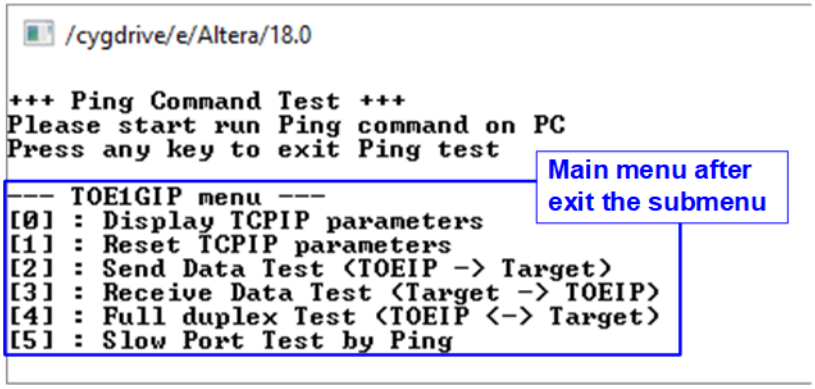



Figure 4-15 Main menu is displayed after exit the submenu

# 5 Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 3-Dec-19 | Initial version release |