TOE1G-IP Full Duplex Demo Instruction

Rev1.3 19-Oct-16

This document describes the instruction to run TOE1G-IP for transferring data between FPGA development board and PC in both directions at the same time through Gigabit Ethernet.

1 Environment Setup

As shown in Figure 1-1- Figure 1-4, to run TOE1G-IP full duplex demo, please prepare

1) FPGA Development board (StratixIV GX/CycloneV E/ArriaV GX Starter /Arria10 SoC board)
2) Quartus Programmer
3) PC with Gigabit Ethernet support
4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
5) USBA-B cable (StratixIV GX/CycloneV E/ArriaV GX Starter board) or micro USB cable (Arria10 SoC board) connecting between FPGA Development board and PC for FPGA programming
6) Test Application “tcp_client_txrx.exe” running on PC, provided by Design Gateway

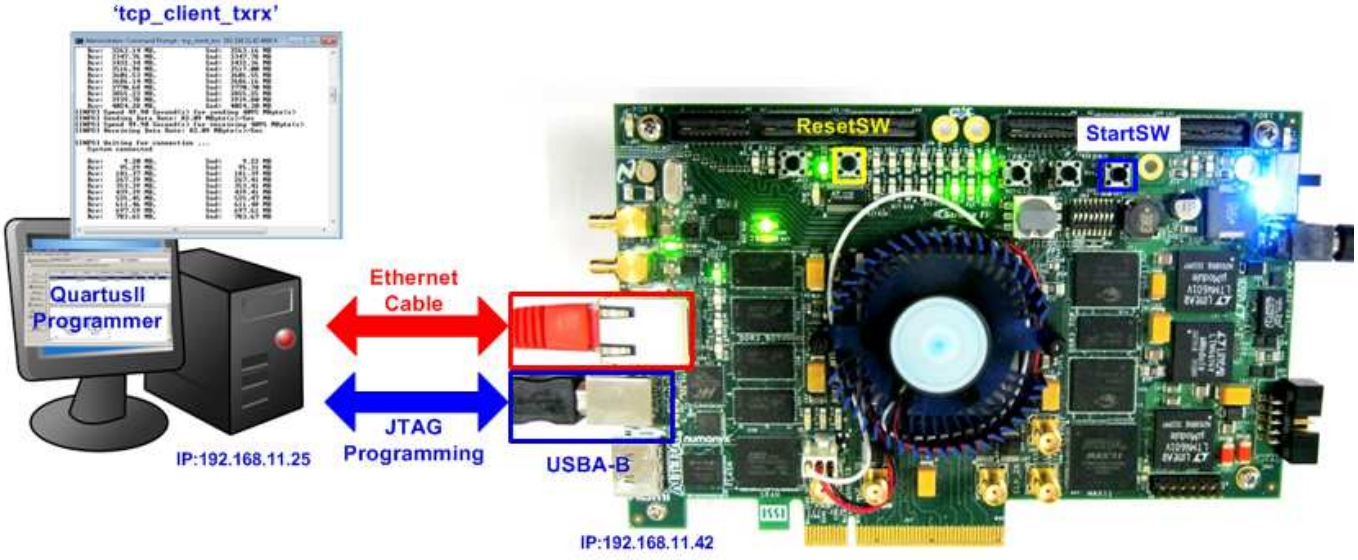

Figure 1-1 TOE1G-IP Full Duplex Demo Environment Setup on StratixIV GX board

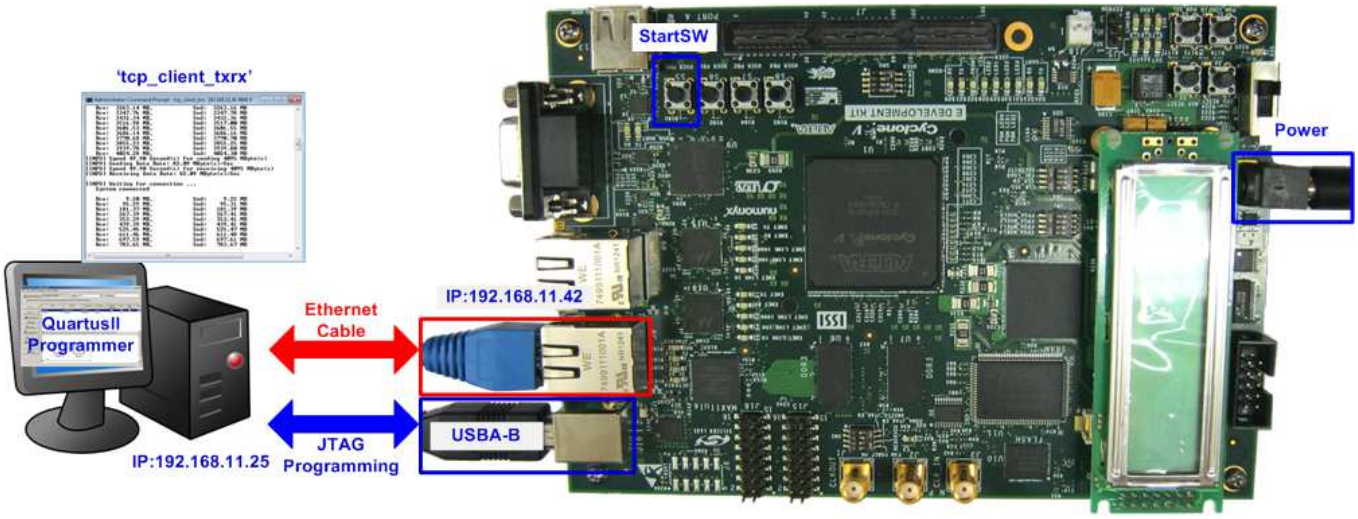

Figure 1-2 TOE1G-IP Full Duplex Demo Environment Setup on CycloneV E board

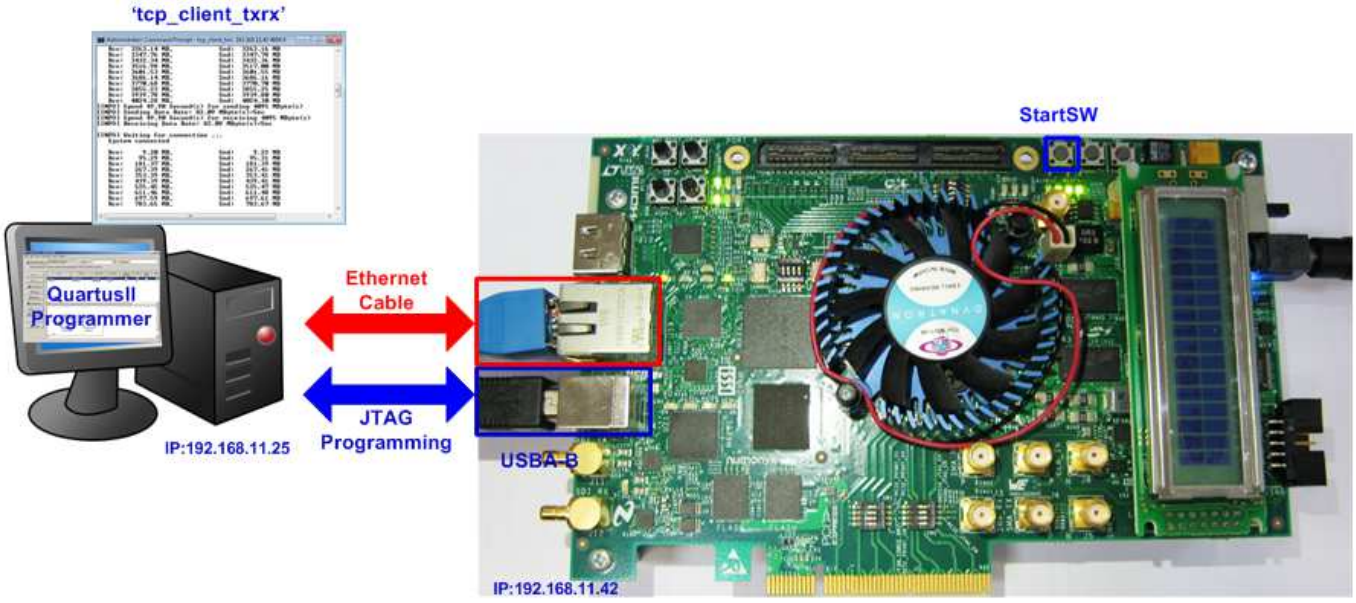

Figure 1-3 TOE1G-IP Full Duplex Demo Environment Setup on ArriaV GX Starter board

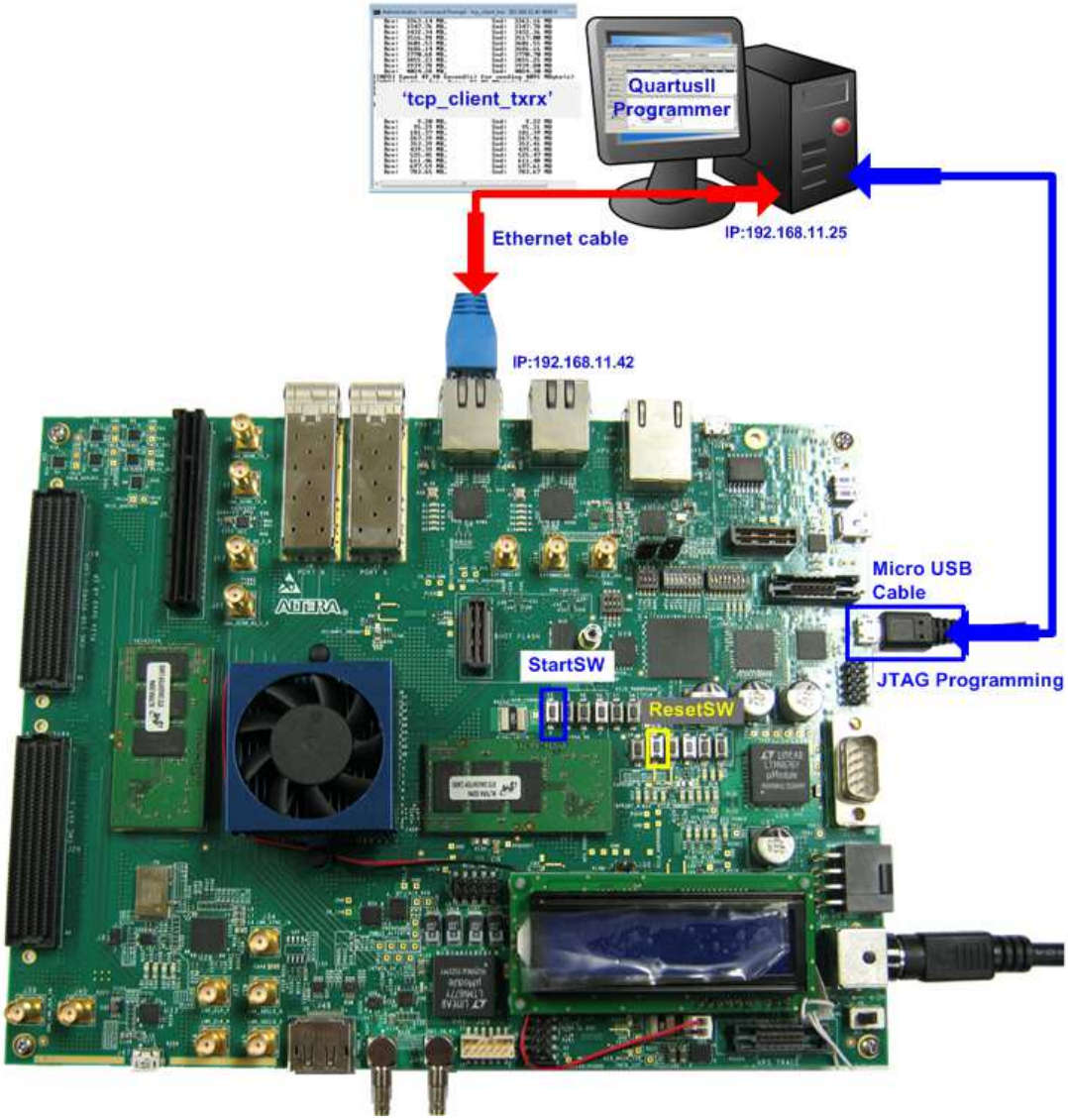

Figure 1-4 TOE1G-IP Full Duplex Demo Environment Setup on Arria10 SoC board

2 Demo description

The logic on FPGA is designed to connect data input and output of TOE1G-IP as loopback connection. So, total transmit data from test application on PC will be returned to PC for checking the data by test application. TCP connection is opened by PC, so PC runs on TCP Client mode while FPGA runs on TCP Server mode. The definition of LED on FPGA Development board is described in Table 2-1.

Table 2-1 LED Definition

LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (PB0-SW) has already been pressed and confirm IP address setting on PC that is correct.
1	BLINK: Operation timeout or cable lost	Normal operation
2	N/A	N/A
3	ON: Port is established	No operation

3 PC Setup

Please follow the same setting as described in “dg_toe1gip_instruction_altera” document (half duplex demo).

4 How to run demo

4.1 FPGA Programming

To run the demo, please follow these steps.

- Connect USB A-B cable/micro USB cable from FPGA Development board to PC and connect power supply to FPGA board.
- Connect Ethernet cable between FPGA Development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA Development board.
- Open Quartus Programmer and download SOF file to FPGA Development board, as shown in Figure 4-1.

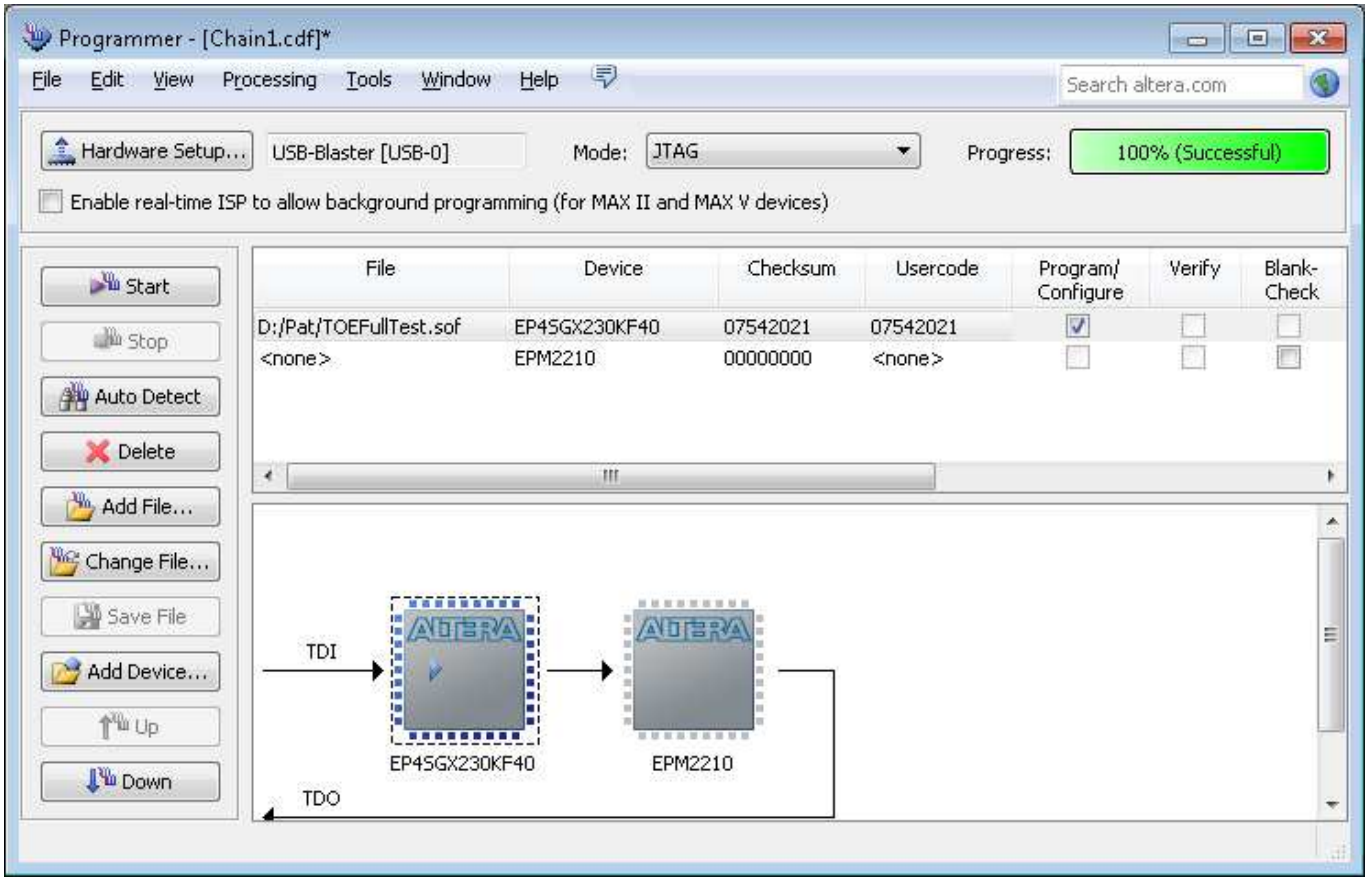

Figure 4-1 Programmer Environment

- Check LED status on FPGA Development board now and LED0/1/3 are all turn off.
- Check 1G link status LED of PHY chip must be ON, as shown in Figure 4-2.

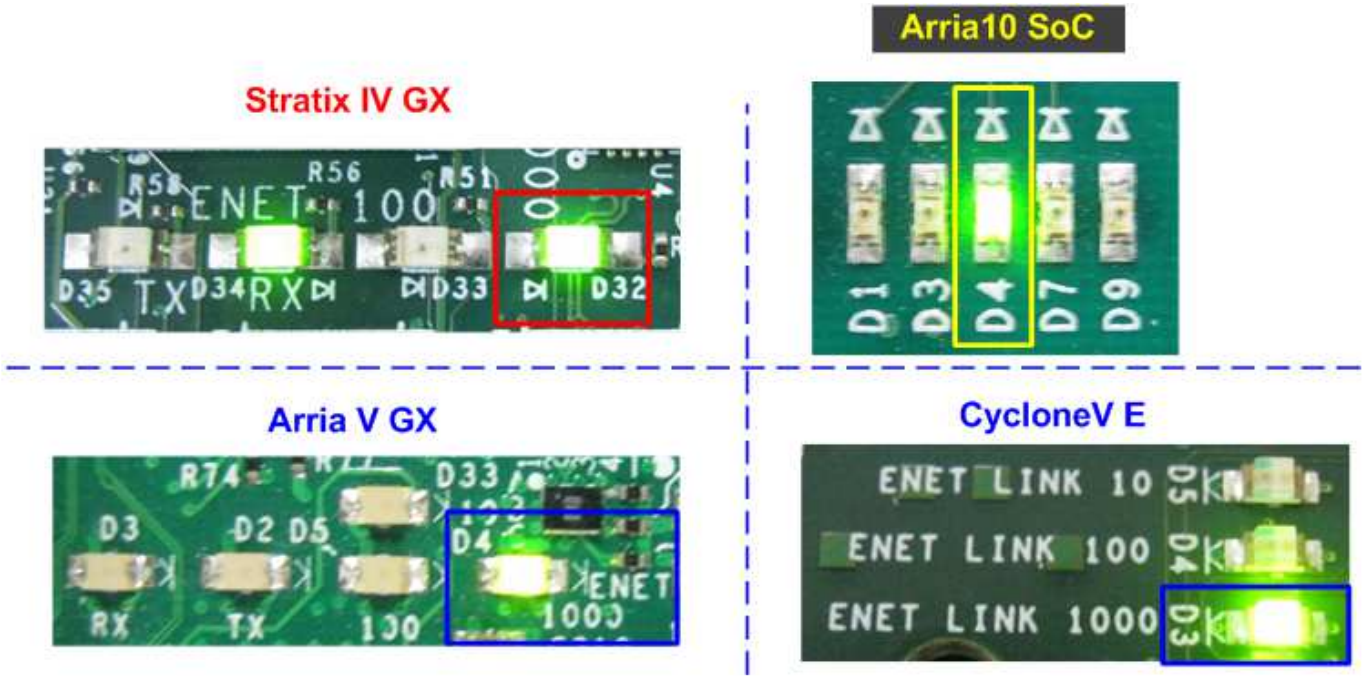

Figure 4-2 Ethernet1000 LED Status

- Press StartSW as shown in Figure 1-1 - Figure 1-4 to initialize system parameter, and then LED0 will turn on, as shown in Figure 4-3. Now system is ready to transfer data.

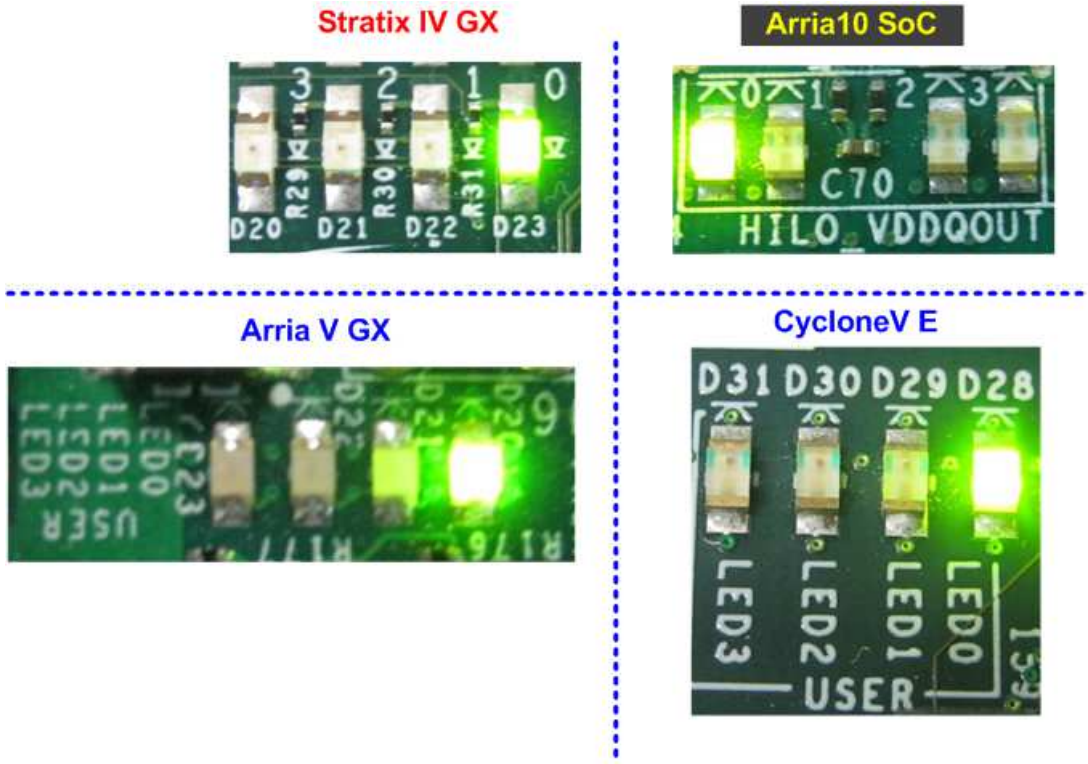

Figure 4-3 LED Status after press StartSW

Note:

- Transfer performance on the demo depends on the performance of Ethernet controller on Test PC.

4.2 Run Test Application

Test application will operate to send and receive 4 GB data at the same time. When all 4 GB are transferred for both directions, port connection will be closed by FPGA. Test application is designed to operate in loop, so new connection will be created by Test application to rerun the test. User needs to cancel the application to stop the test.

There are two operation modes for running the demo, i.e. Performance test mode, and Verification mode. The details of each mode are follows.

4.2.1 Performance Test mode

- Open “command prompt” on PC, and run “tcp_client_txrx” test application by following command
  >> tcp_client_txrx <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘0’-All ‘0’ pattern are sent out and no data verification

  For example,
  >> tcp_client_txrx 192.168.11.42 4000 0

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 4-4.
- User can cancel operation by pressing “Ctrl+C”.

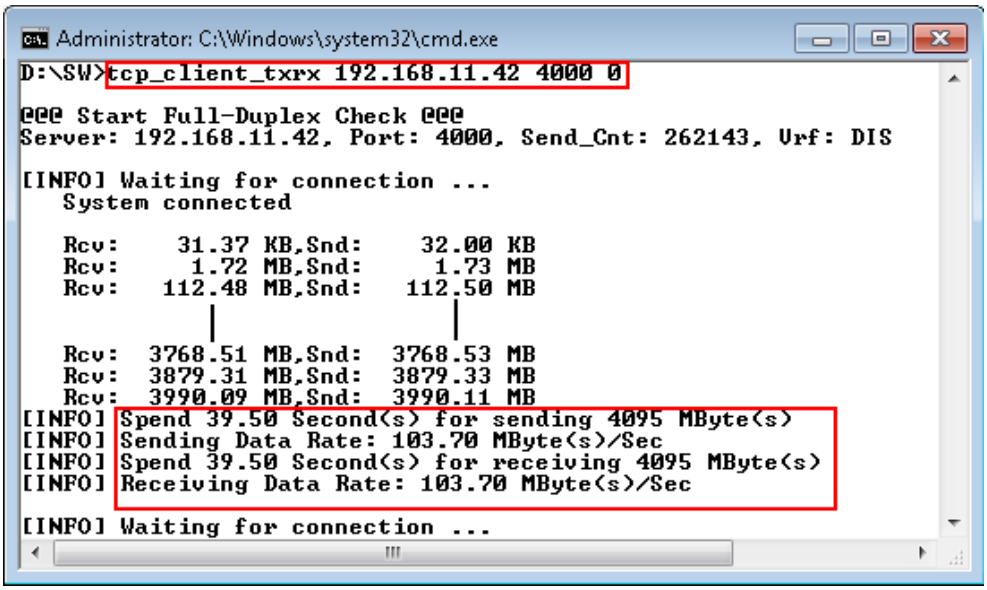

Figure 4-4 Test Result on Performance test mode

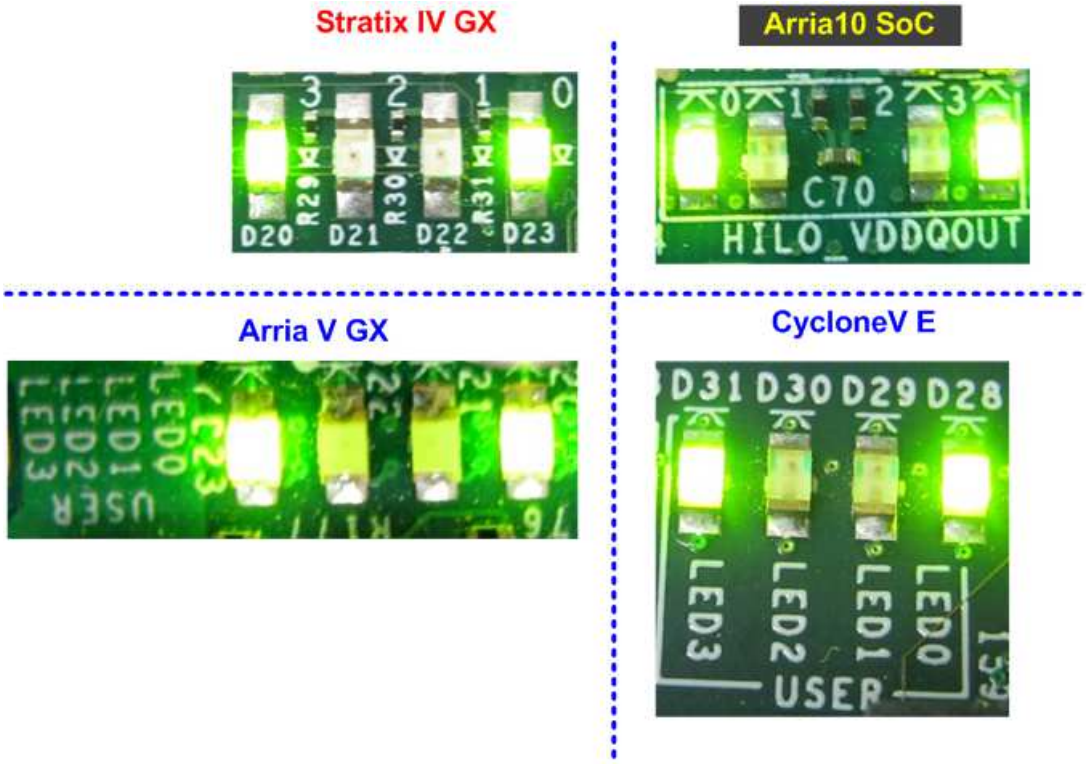

Figure 4-5 LED Status when running full duplex Demo for both modes

4.2.2 Verification mode

- Open “command prompt” on PC, and run “tcp_client_txrx” test application by following command
  >> tcp_client_txrx <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘1’-32-bit increment data are sent out and data verification is enabled.

  For example,
  >> tcp_client_txrx 192.168.11.42 4000 1

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 4-6.
- User can cancel operation by pressing “Ctrl+C”.

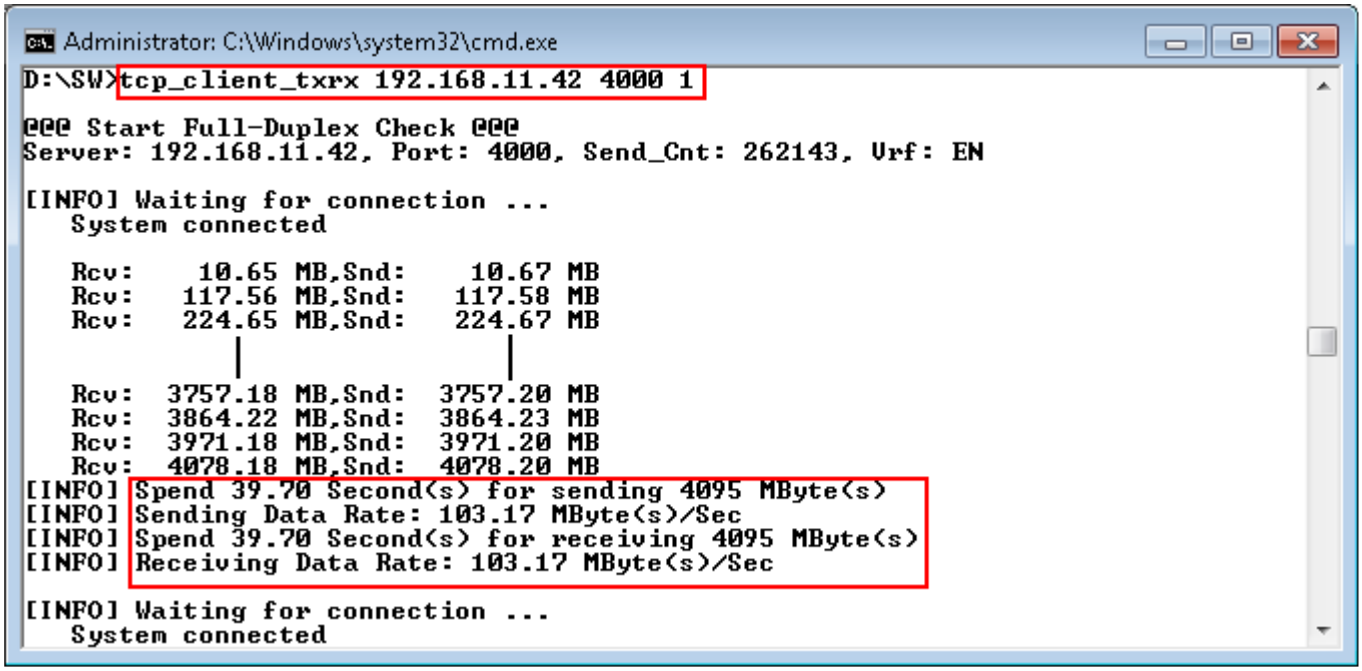

Figure 4-6 Test Result on Verification mode

5 Revision History

Revision	Date	Description
1.0	22-Aug-14	Initial version release
1.1	3-Dec-14	Add performance options
1.2	19-Aug-16	Change IP name and support Arria10
1.3	19-Oct-16	Support CycloneV E board