# TOE1G-IP Demo Instruction

Rev1.3 19-Oct-16

This document describes the instruction to run TOE1G-IP for transferring data between FPGA development board and PC through Gigabit Ethernet. This demo can select to run with supported and not supported Jumbo frame PC.

## 1 Environment Setup

As shown in Figure 1-1 - Figure 1-4, to run TOE1G-IP standard demo, please prepare

1) FPGA Development board (StratixIV GX/CycloneV E/ArriaV GX Starter/Arria10 SoC board)
2) QuartusII Programmer
3) PC with Gigabit Ethernet support
4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
5) USB-AB cable (StratixIV GX/CycloneV E/ArriaV GX Starter board) or micro USB cable (Arria10 SoC board) connecting between FPGA development board and PC for FPGA programming
6) “send_tcp_client.exe” and “recv_tcp_client.exe”, provided by Design Gateway, which are test application available on PC

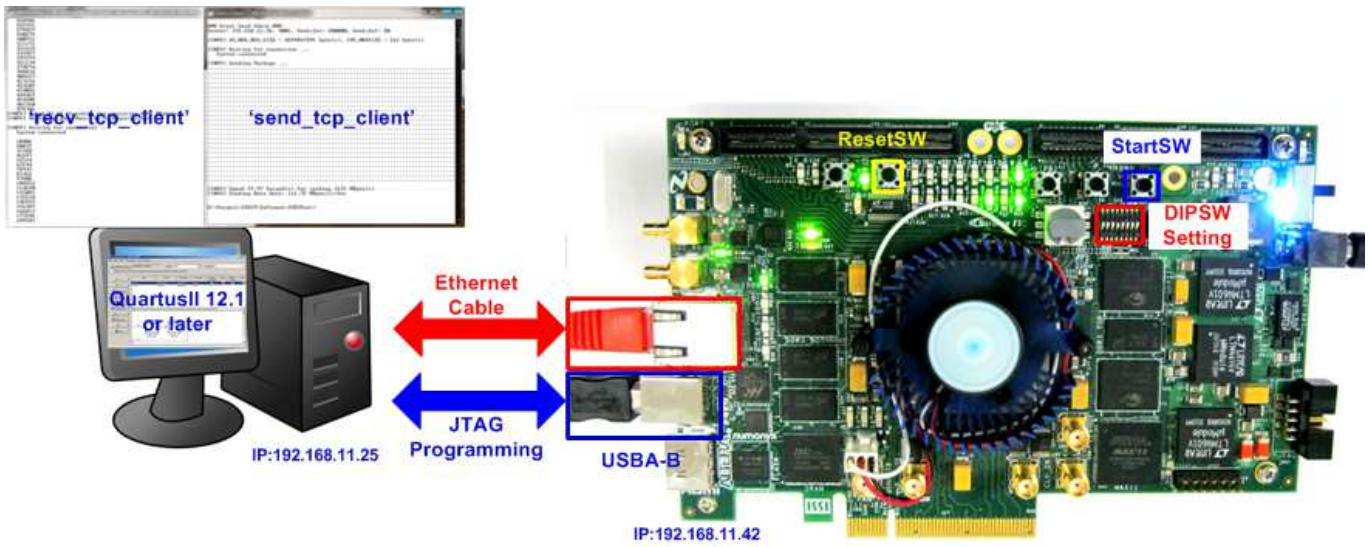


Figure 1-1 TOE1G-IP Demo Environment Setup on StratixIV GX board

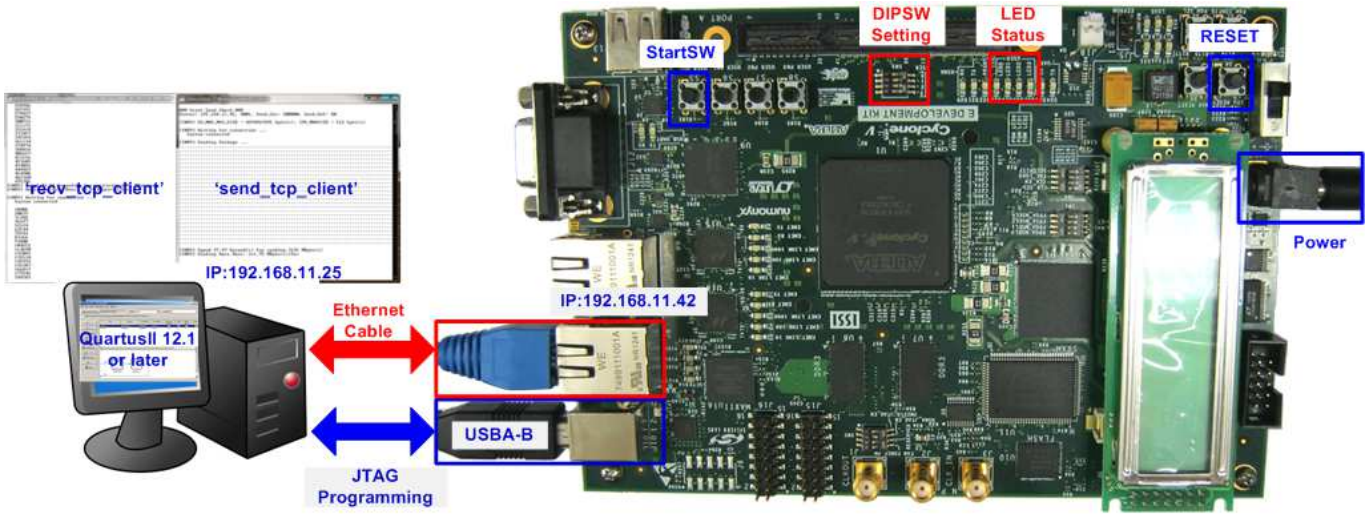


Figure 1-2 TOE1G-IP Demo Environment Setup on CycloneV E board

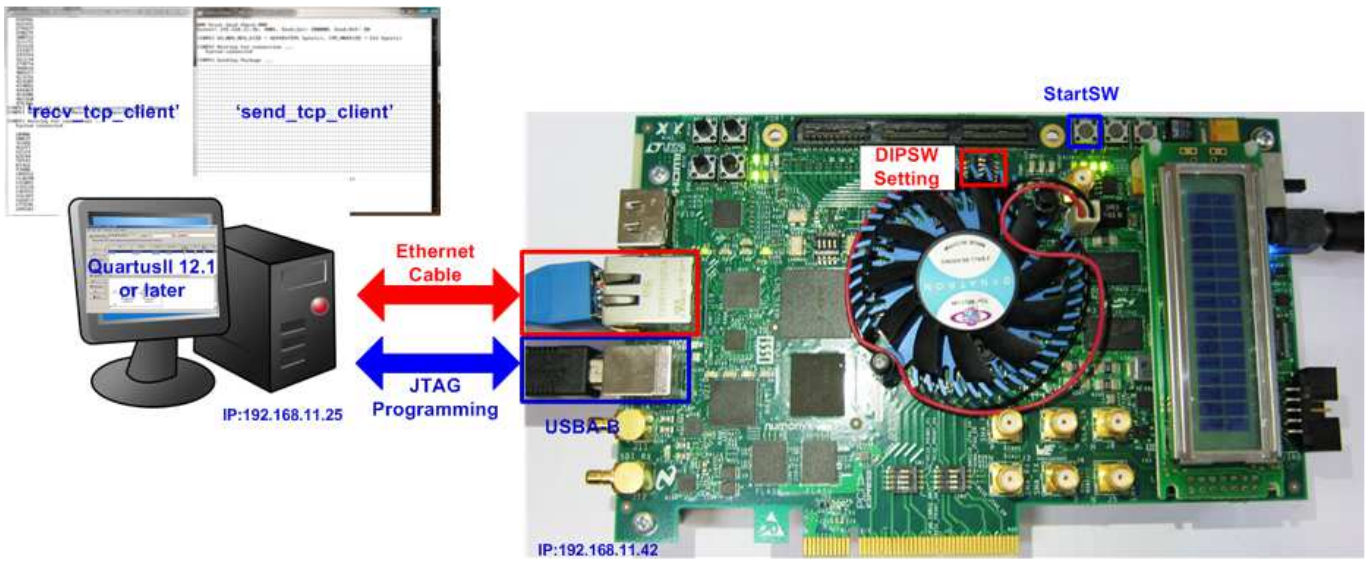


Figure 1-3 TOE1G-IP Demo Environment Setup on ArriaV GX Starter board

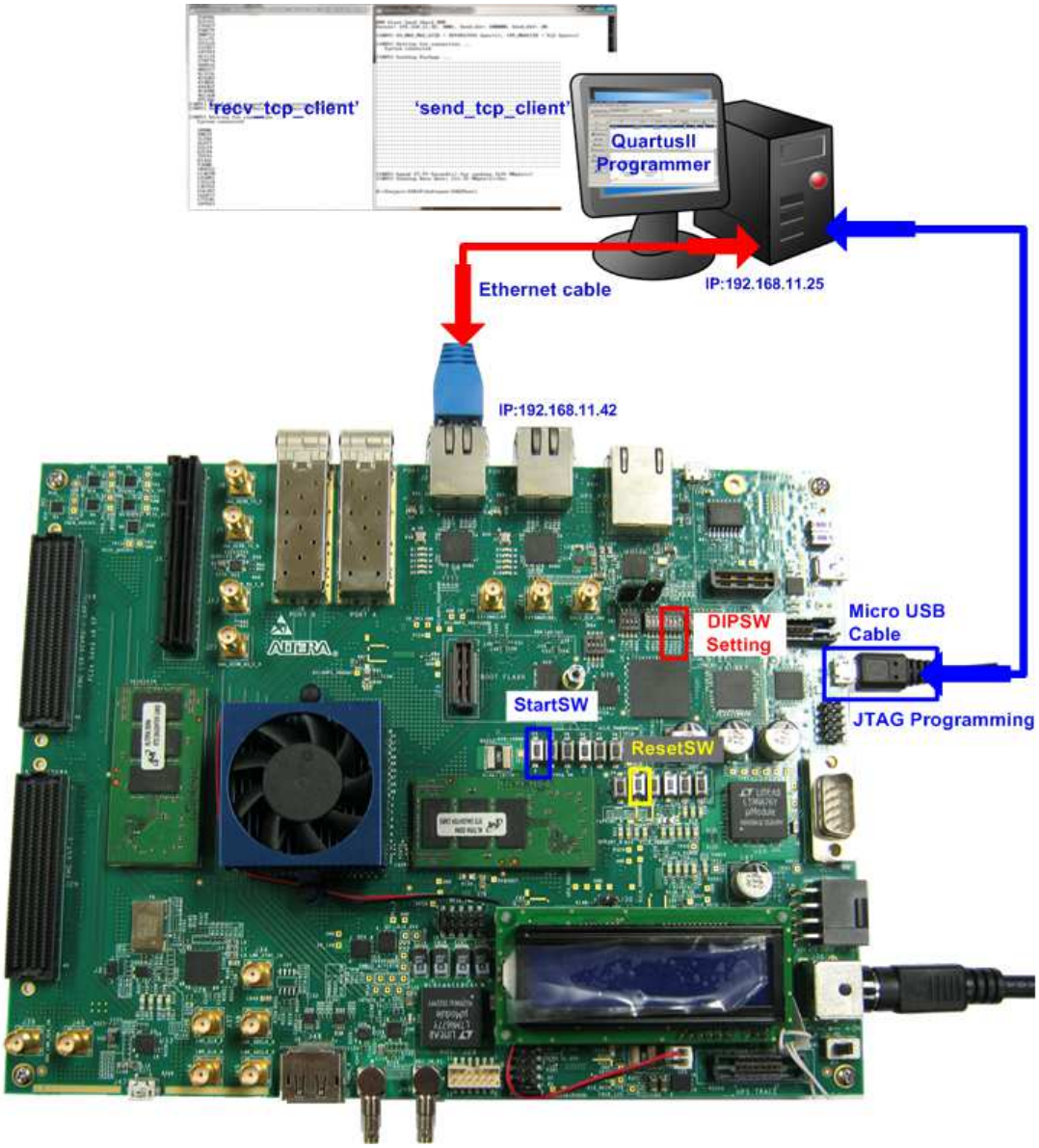


Figure 1-4 TOE1G-IP Demo Environment Setup on Arria10 SoC board

# 2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC and different DIPSW setting on FPGA development board. The definition of DIPSW and LED on FPGA development board are described in Table 2-1 and Table 2-2.

Table 2-1 DIPSW Setting Definition

| DIPSW | ON | OFF |
|---|---|---|
| Bit 1 | Sending mode by using non-Jumbo frame (1460 bytes) | Sending mode by using Jumbo frame (8960 bytes) |
| Bit 2 | Sending mode | Receiving mode |
| Bit 3 | Receiving mode without data verification | Receiving mode with data verification |

Table 2-2 LED Definition

| LED | ON/BLINK | OFF |
|---|---|---|
| 0 | ON: IP initialize complete | Not complete.<br>Please check that StartSW (PB0 SW) has already been pressed and confirm IP address setting on PC that is correct. |
| 1 | BLINK: Operation timeout or cable lost | Normal operation |
| 2 | Sending mode in Jumbo frame. | Sending mode in non-jumbo frame |
| 3 | BLINK: data verification is fail in receiving mode<br>ON: Port is established. | No operation |

Note:
- Cable lost detection is not available on ArriaV GX and CycloneV E board.
- DIPSW setting must not be changed during operation.

More details about each test mode are follows.

## 2.1 Sending mode

In this mode, 4 GB data will be transferred from FPGA development board to PC, and "recv_tcp_client.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select two transfer packet sizes by DIPSW[1] setting, i.e. 1460 data byte for running with not supported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting from LED2 status.

The operation sequence for sending mode is follows.

1) TOE1G-IP within FPGA development board initializes system parameters such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
2) Test application on PC opens connection to connect with FPGA development board, and waits data sending from FPGA.
3) TOE1G-IP starts to send 4 GB data to PC while PC verifies receiving data that is correct.
4) After all data are transferred, TOE1G-IP sends packet to close connection.
5) PC sends acknowledge to close connection. Then, operation will run as loop from Step2) to Step5) until operation cancelled.

## 2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By using "send_tcp_client.exe" operating on PC, data will be sent out until total number of transferred data equal to setting value. This test can run as two modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC and verification module within FPGA development board will be OFF for achieving best performance transfer. In data verification mode, 32-bit increment data will be generated from PC and verification module will be ON for data verification. LED3 will blink if error data is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can be set as option value in command line.

The operation sequence for receiving mode is follows.

1) Similar to Step 1) in Sending mode.
2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
3) TOE1G-IP receives data and verifies data if enable.
4) After all data are transferred, Test application sends packet to close connection.
5) TOE1G-IP sends acknowledgment to close connection. This mode will run only one time, not in repeat loop like Sending mode.

# 3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

## 3.1 IP Setting

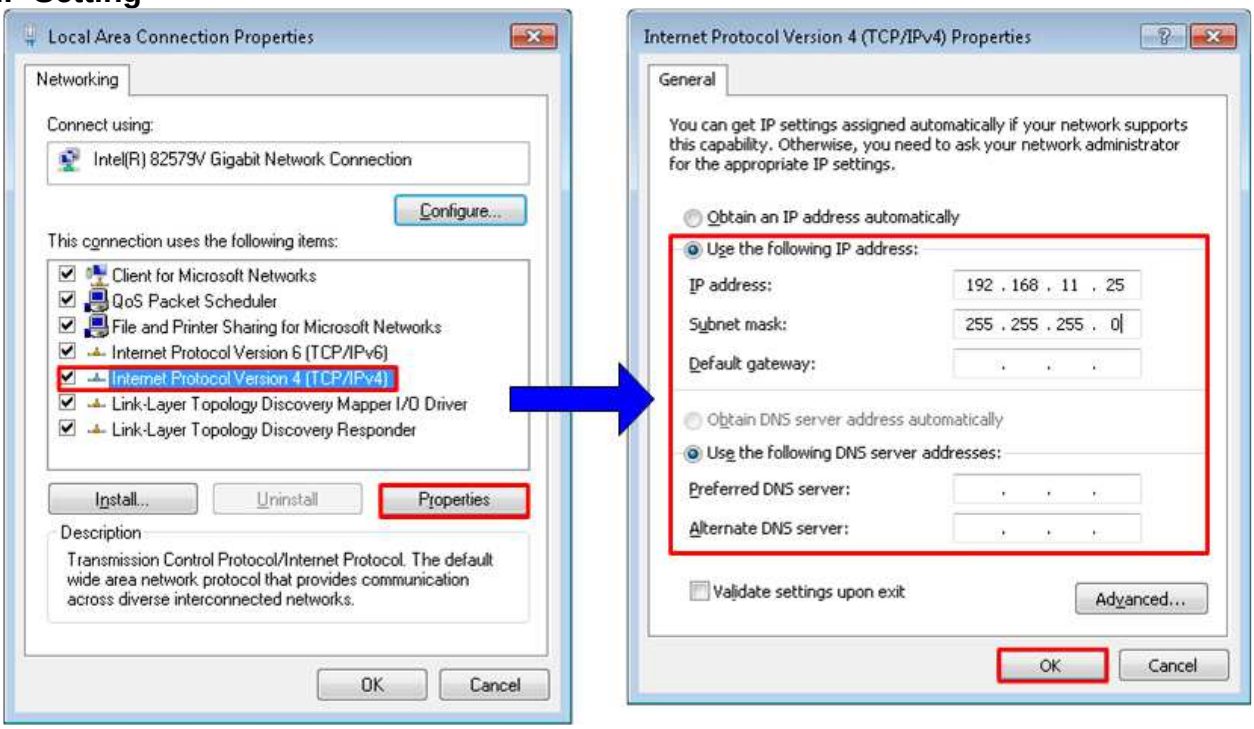


Figure 3-1 IPv4 Setting

- Open Local Area Connection Properties of test connection, as shown in left window of Figure 3-1.
- Select “TCP/IPv4” and then click Properties.
- Set IP address = 192.168.11.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 3-1.

## 3.2 Speed and Frame Setting

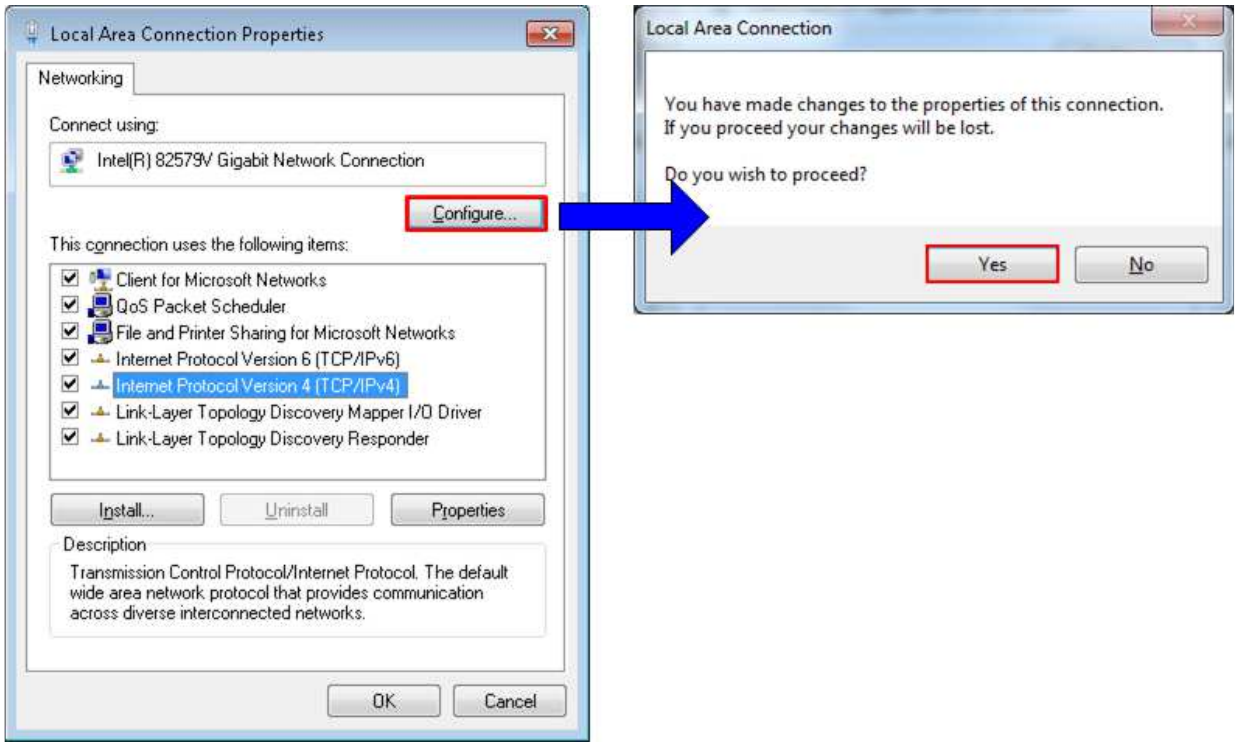


Figure 3-2 Network Configure

- On Local Area Connection Properties window, click “Configure”, as shown in Figure 3-2.
- On Advance tab, Jumbo Packet = 9014 Bytes to enable jumbo frame, as shown in Figure 3-3.

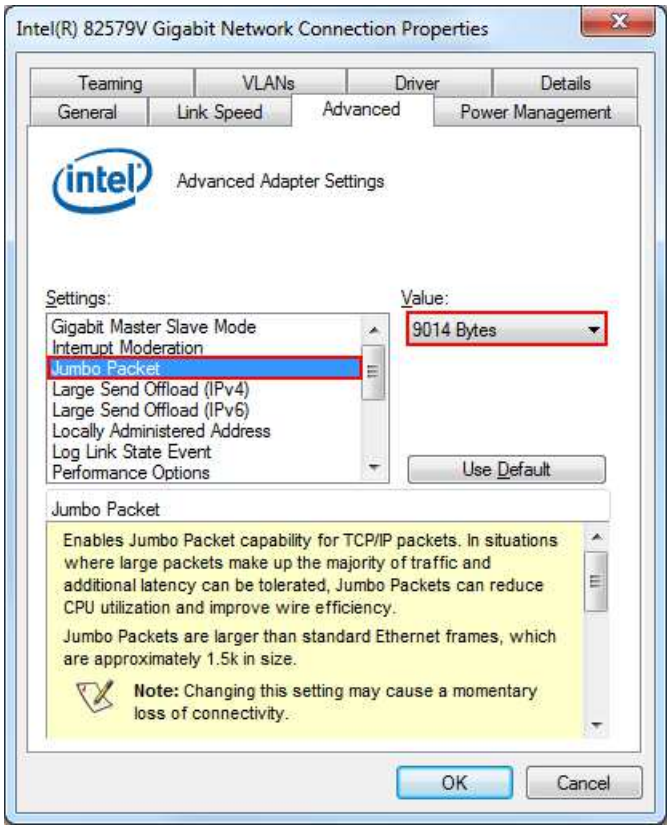


Figure 3-3 Jumbo Frame Setting

- On Link Speed tab, select “1.0 Gbps Full Duplex” for running Gigabit transfer test, as shown in left window of Figure 3-4.
- On Advance tab, Settings=Interrupt Moderation and Value= “Enabled”, as shown in right window of Figure 3-4.

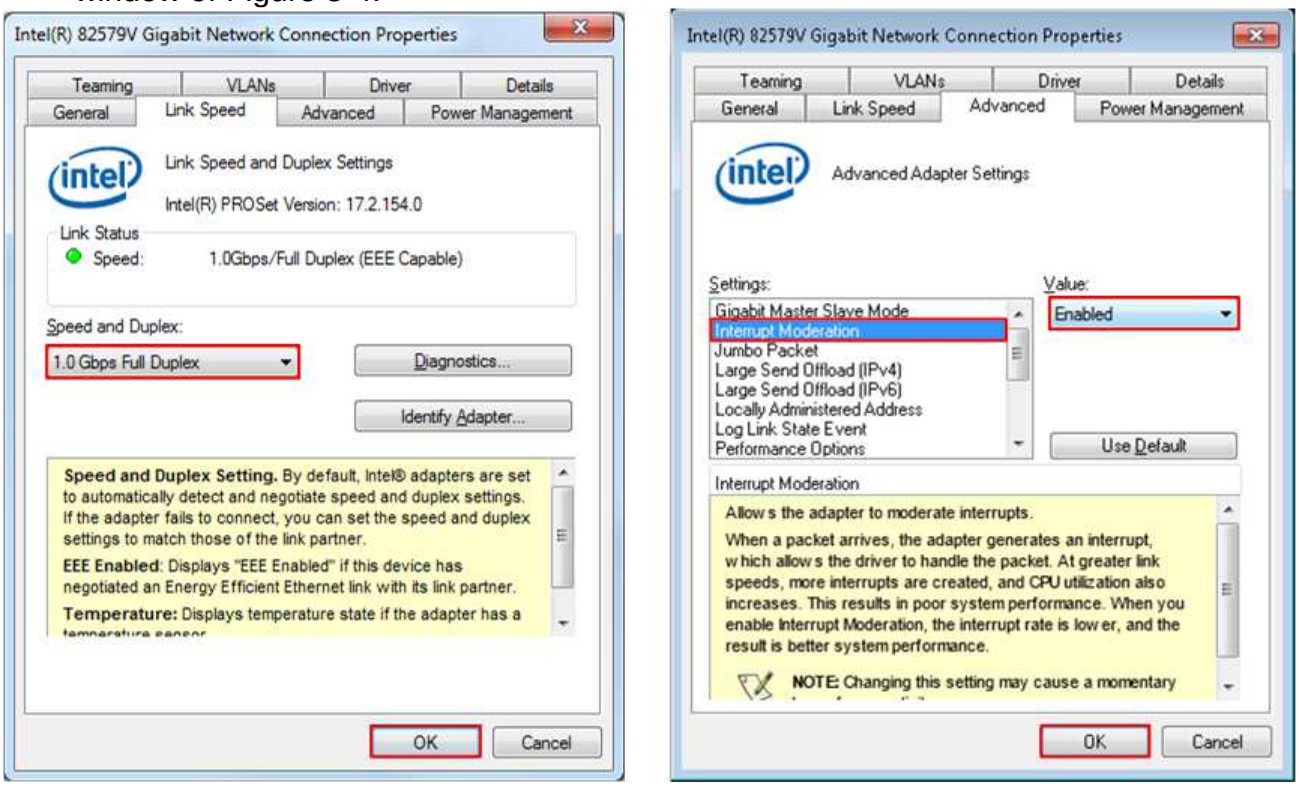


Figure 3-4 Link speed and Jumbo frame setup

- For Intel LAN controller, Performance Options in “Advanced” tab should be set for better performance as shown in Figure 3-5. “Interrupt Moderation Rate” in “Performance Options” windows must be set to “Off”.

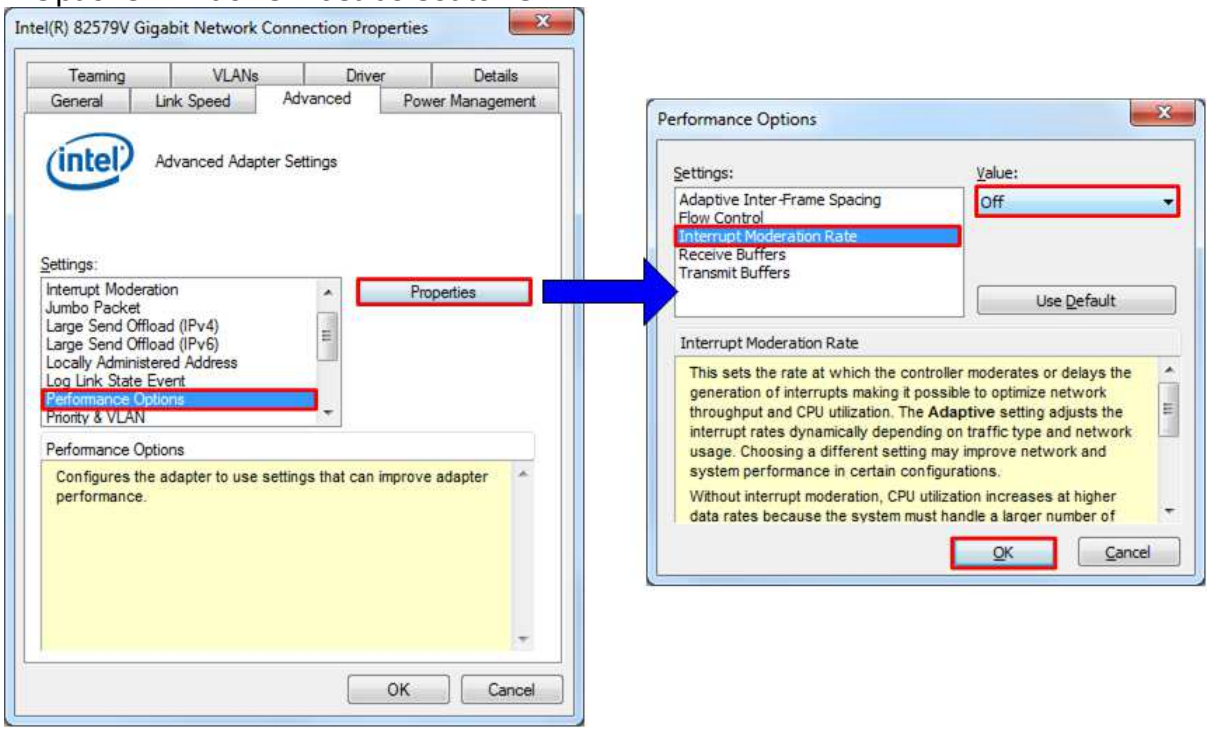


Figure 3-5 Enable Interrupt Moderation

# 4 How to run demo

Both Sending and Receiving demo requires same initial steps to set up hardware as follows.

- Connect USB-AB cable/micro USB cable from FPGA development board to PC and connect power supply to FPGA board.
- Connect Ethernet cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- Open QuartusII Programmer and download SOF to FPGA development board, as shown in Figure 4-1.

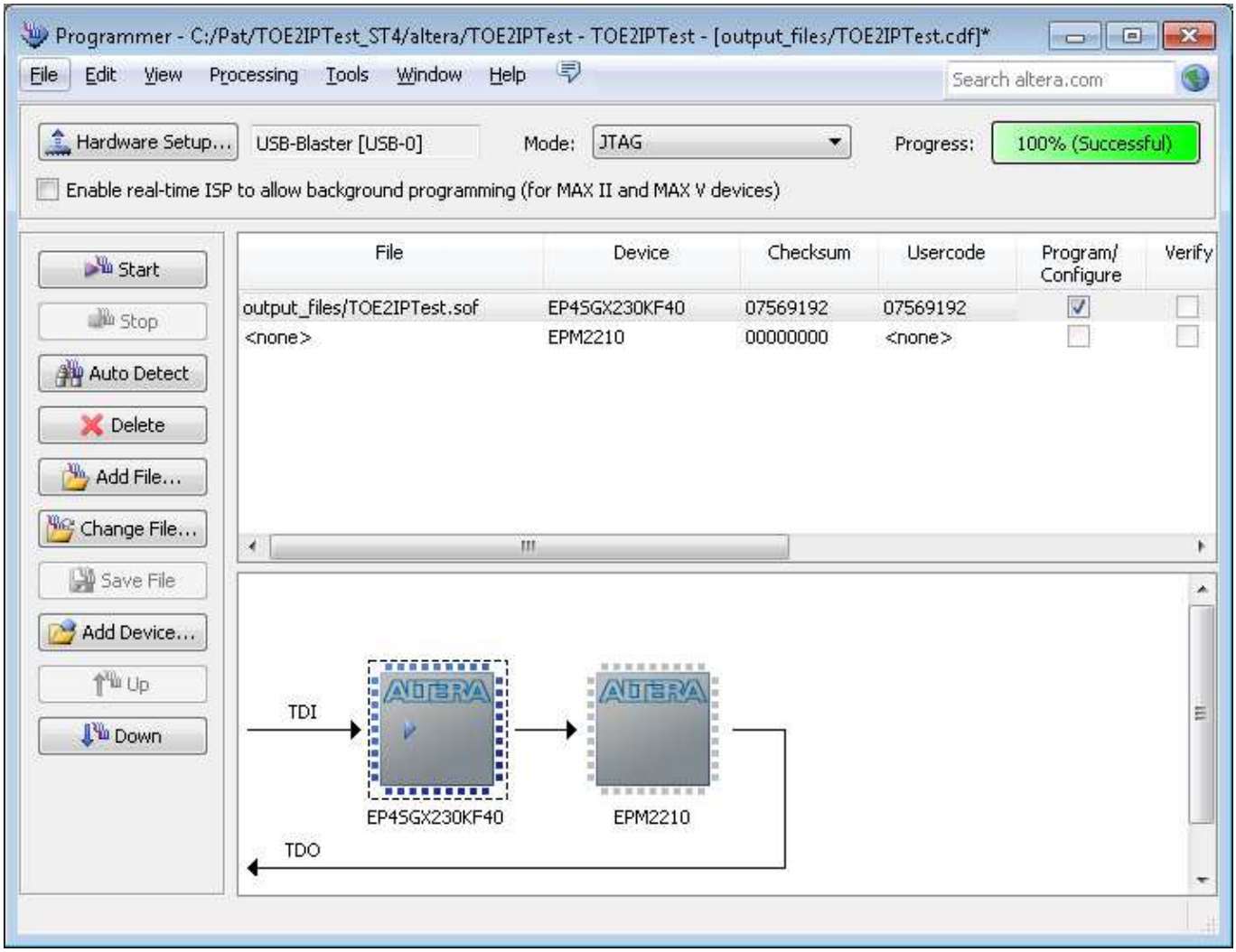


Figure 4-1 Programmer Environment

- Check LED status on FPGA development board now and LED0/1/3 are all turn off.
- Check 1G link status LED of PHY chip must be ON, as shown in Figure 4-2.

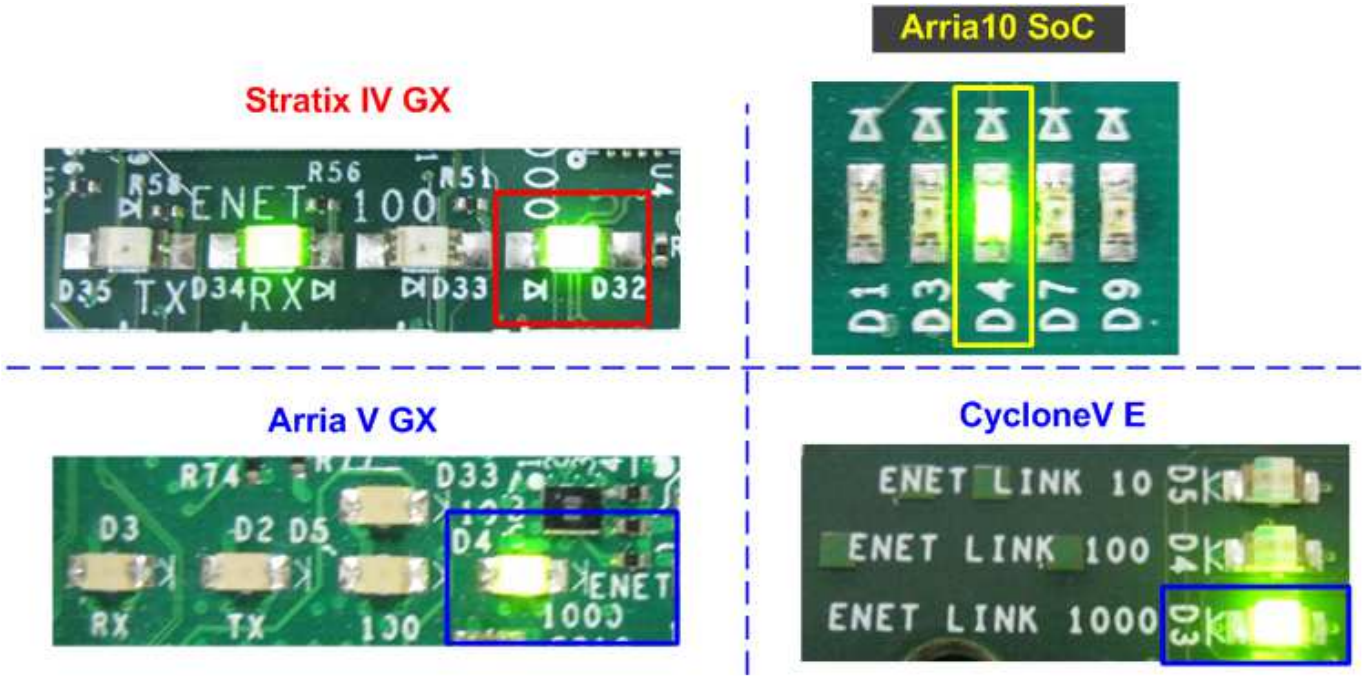


Figure 4-2 Ethernet1000 LED Status

- Press StartSW at PB0-SW as shown in Figure 1-1 - Figure 1-4 to initialize system parameter, and then LED0 will turn on, as shown Figure 4-3 - Figure 4-4 following DIPSW[1] setting.

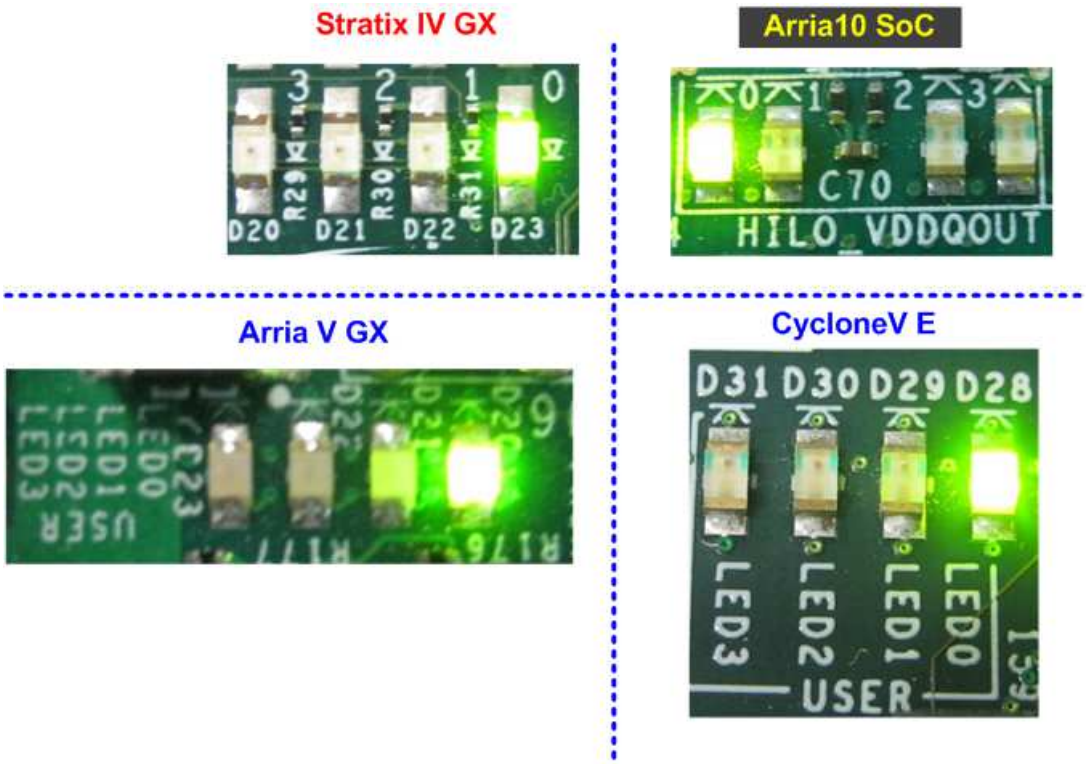


Figure 4-3 LED Status after press StartSW when DIPSW[1]=ON for non-Jumbo frame

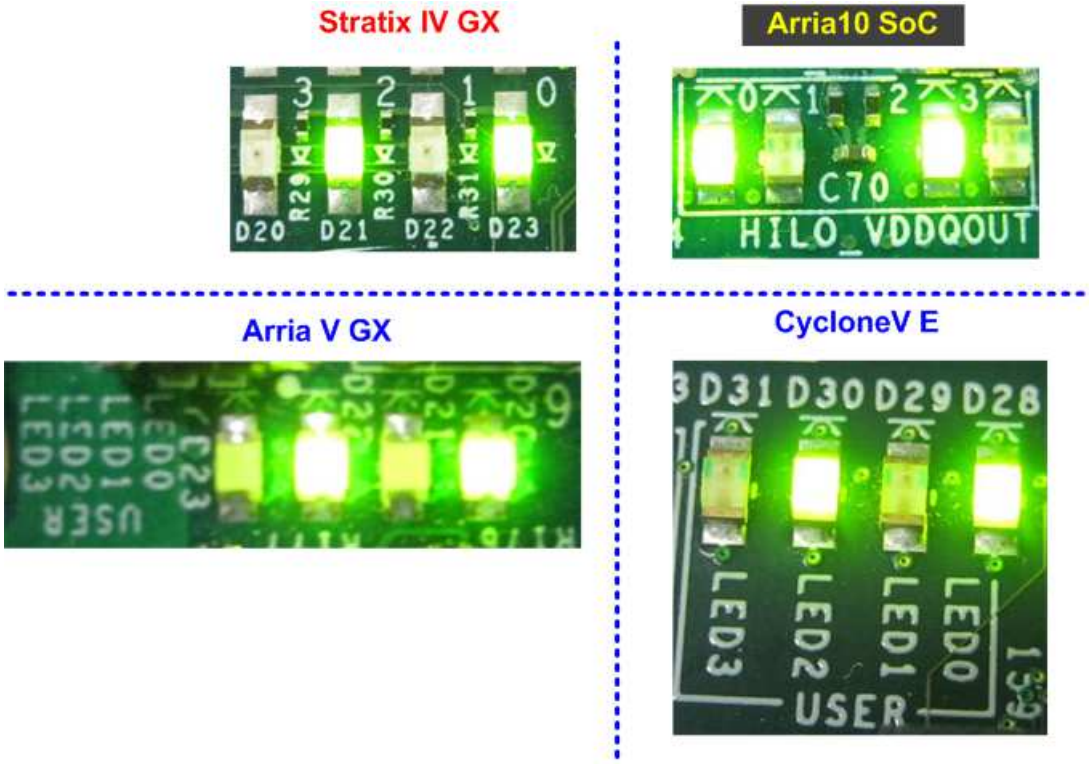


Figure 4-4 LED Status after press StartSW when DIPSW[1]=OFF for Jumbo frame

Now system is ready to transfer data. The step to test Sending and Receiving data is described in next topic.

Note:

- Transfer performance on the demo depends on Test PC performance to send and receive data through Gigabit Ethernet

## 4.1 Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test.

4.1.1 Non-Jumbo frame mode

- Set DIPSW[2] = ON to run Sending demo.
- Set DIPSW[1] = ON and confirm that LED2 status is OFF.
- Open “command prompt” on PC, and run “recv_tcp_client” test application by following command
  >> recv_tcp_client <FPGA IP address> <FPGA port number> <number of data in packet>
  For example,
  >> recv_tcp_client 192.168.11.42 4000 1460
  Note: This demo fixes IP address, port number, and the number of data. So, please do not change any value without vhdl code modification.
- Test application displays current number of packet, and time usage with performance will be displayed when complete each loop transfer, as shown in Figure 4-5.
- User can cancel operation by pressing “Ctrl+C”.

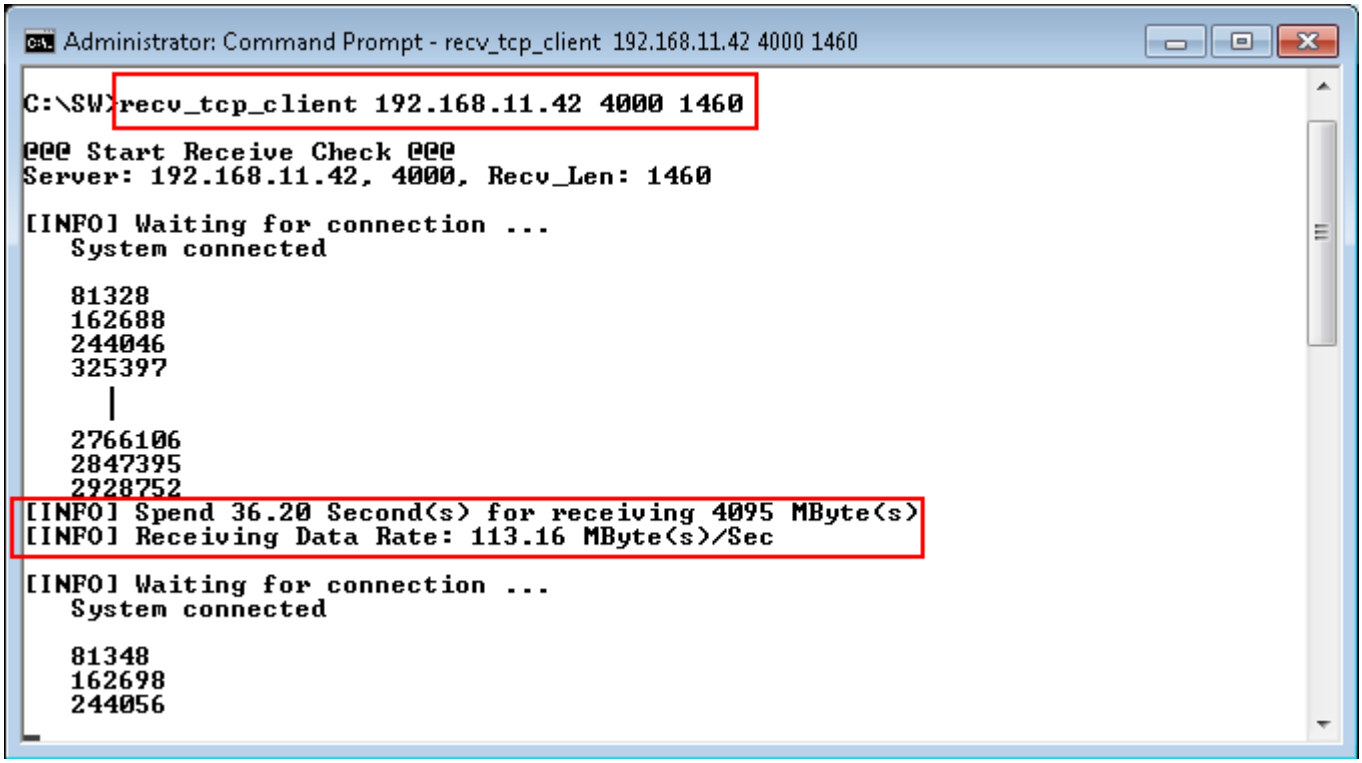


Figure 4-5 Non-Jumbo frame Sending Demo

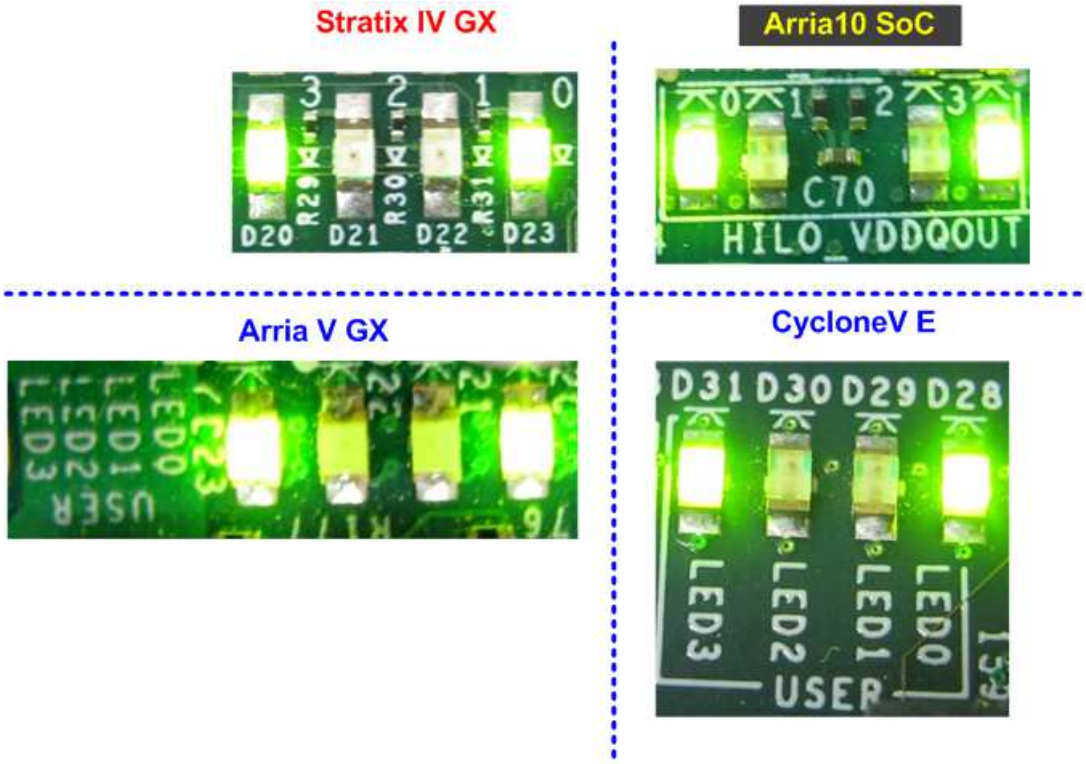


Figure 4-6 LED Status when running Sending Demo with Non-Jumbo frame

### 4.1.2 Jumbo frame mode

- Set DIPSW[2] = ON to run Sending demo.
- Set DIPSW[1] = OFF and confirm that LED2 status is ON.
- Open “command prompt” on PC, and run “recv_tcp_client” test application by following command
  >> recv_tcp_client 192.168.11.42 4000 8960
  Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without vhdl code modification.
- Message during test operation and how to cancel operation are similar to Non-Jumbo frame mode.

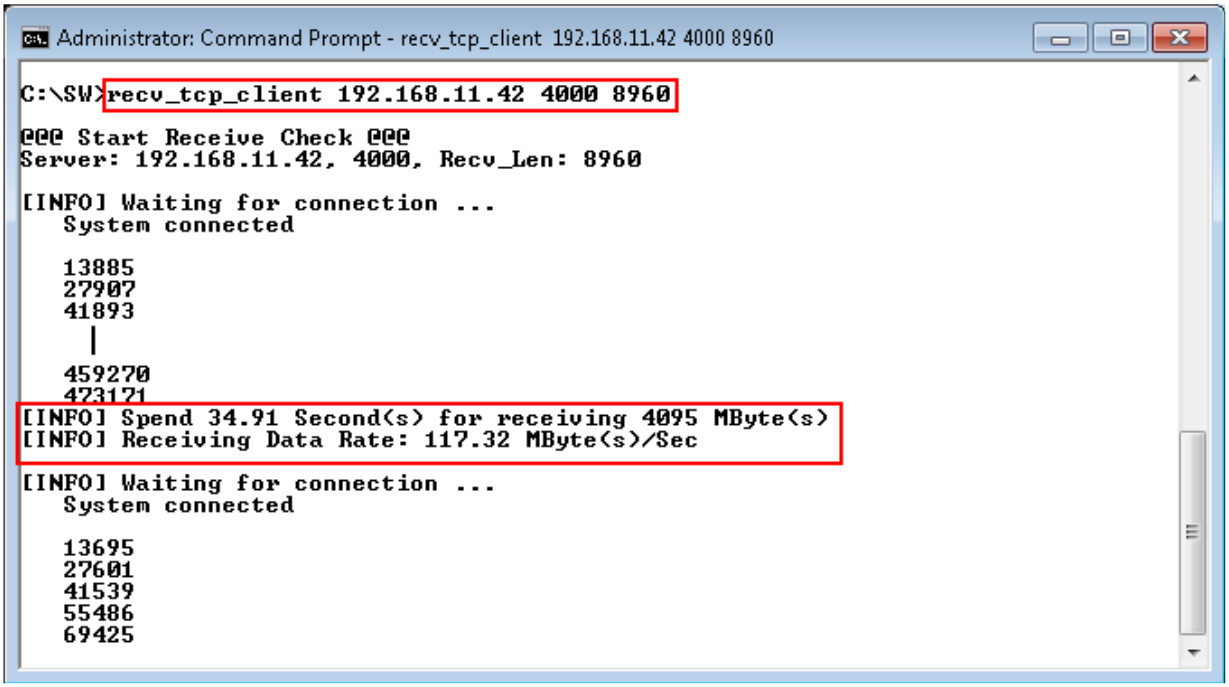


Figure 4-7 Jumbo frame Sending Demo

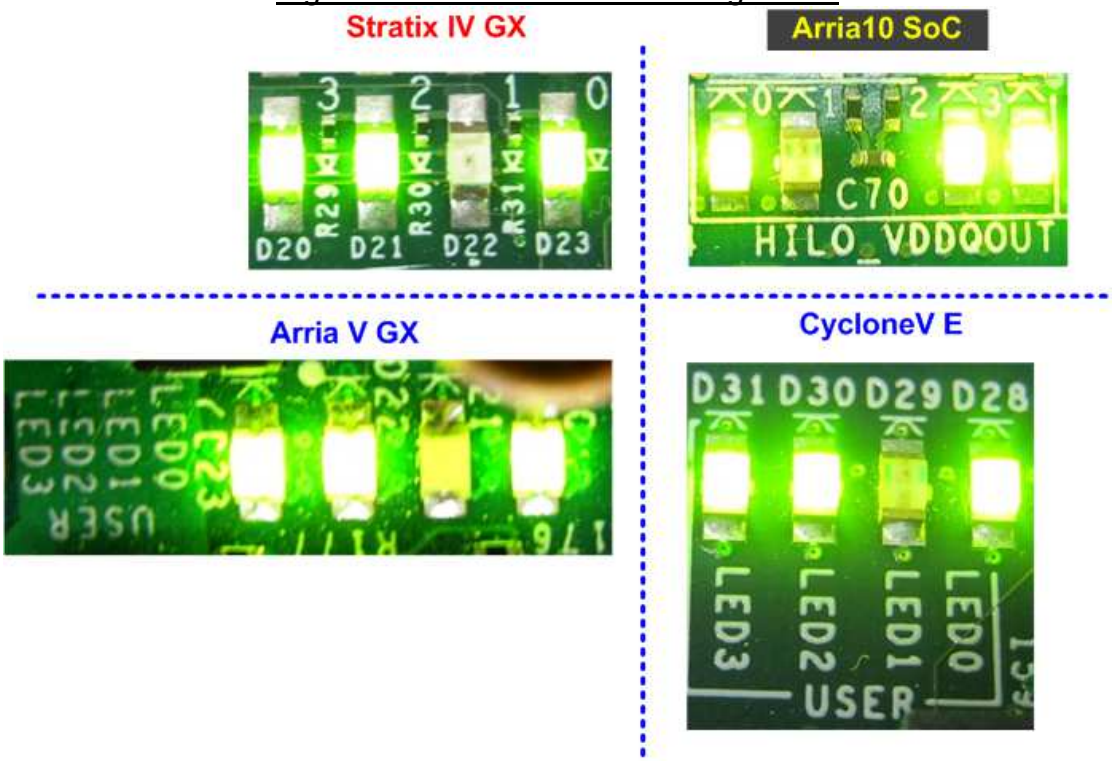


Figure 4-8 LED Status when running Sending Demo with Jumbo frame

## 4.2 Run Receiving Demo

### 4.2.1 Performance test mode

- Set DIPSW[2] = OFF to run Receiving demo.
- Set DIPSW[3] = ON to disable verification module.
- Open “command prompt” on PC, and run “send_tcp_client” test application by following command
  >> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
  - User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 MByte data is transferred. Valid range of transfer size is 1 – 262143.
  - Mode: ‘0’- All ‘0’ pattern are sent for performance test.

  For example,
  >> send_tcp_client 192.168.11.42 4000 100000 0

- Test application displays “…” during transferring packet. Time usage with performance will be displayed when complete data transfer, as shown in Figure 4-10.

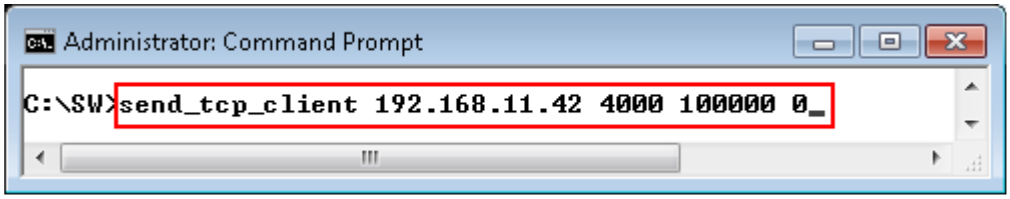


Figure 4-9 Command line for receiving demo on Performance test mode

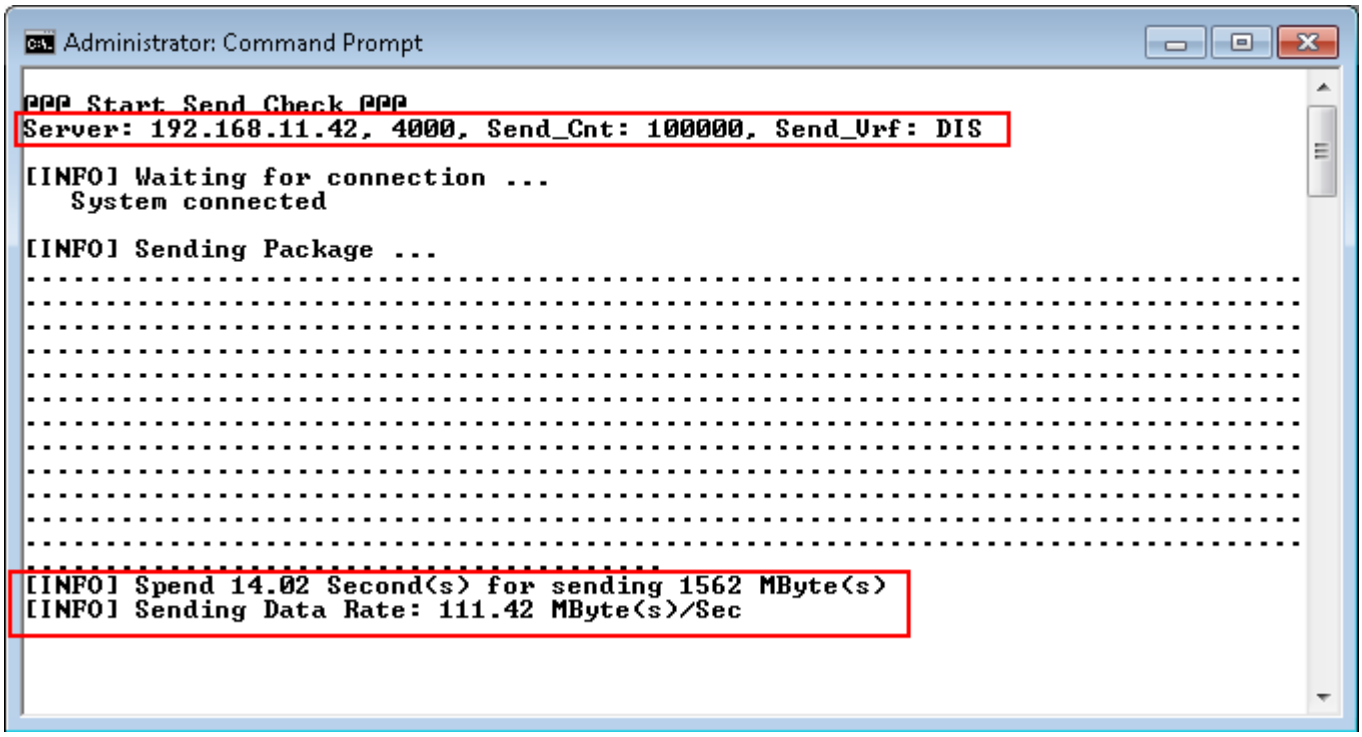


Figure 4-10 Receiving Demo on Performance test mode

### 4.2.2 Verification mode

- Set DIPSW[2] = OFF to run Receiving demo.
- Set DIPSW[3] = OFF to enable verification module.
- Open “command prompt” on PC, and run “send_tcp_client” test application by following command
  >> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
  - Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
  - User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 Mbyte data is transferred. Valid range of transfer size is 1 – 262143.
  - Mode: ‘1’- 32-bit increment data are sent for data verification.

  For example,
  >> send_tcp_client 192.168.11.42 4000 100000 1
- Test application displays “…” during transferring packet and time usage with performance will be displayed when complete data transfer, as shown in Figure 4-12.

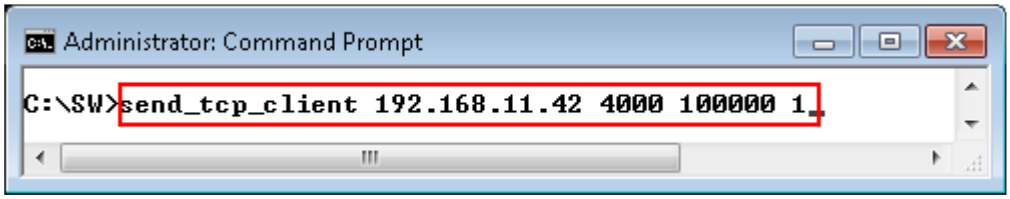


Figure 4-11 Command line for receiving demo on Performance test mode

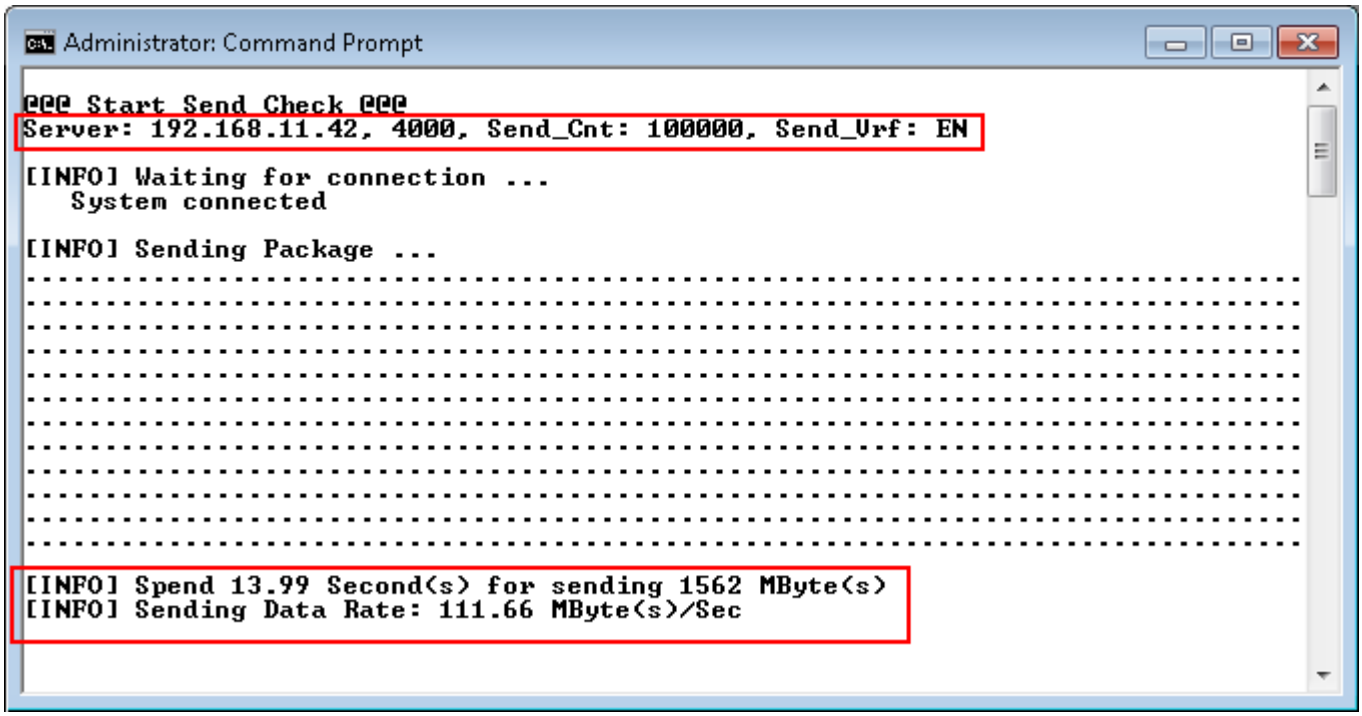


Figure 4-12 Receiving Demo on Verification mode

- LED3 will blink if any error data detects from Verification module.

# 5 Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 28-Aug-14 | Initial version release |
| 1.1 | 3-Dec-14 | Change Internet controller model |
| 1.2 | 18-Aug-16 | Change IP name and support Arria10 |
| 1.3 | 19-Oct-16 | Support CycloneV E board |