

TOE1G-IP Demo Instruction

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This document describes the instruction to run TOE1G-IP for transferring data between FPGA development board and PC through Gigabit Ethernet. This demo can select to run with supported and not supported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1-1 - Figure 1-4, to run TOE1G-IP standard demo, please prepare

- 1) FPGA Development board (StratixIV GX/CycloneV E/ArriaV GX Starter/Arria10 SoC board)
- 2) QuartusII Programmer
- 3) PC with Gigabit Ethernet support
- 4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
- USB-AB cable (StratixIV GX/CycloneV E/ArriaV GX Starter board) or micro USB cable (Arria10 SoC board) connecting between FPGA development board and PC for FPGA programming
- 6) "send_tcp_client.exe" and "recv_tcp_client.exe", provided by Design Gateway, which are test application available on PC



Figure 1-1 TOE1G-IP Demo Environment Setup on StratixIV GX board





Figure 1-2 TOE1G-IP Demo Environment Setup on CycloneV E board



Figure 1-3 TOE1G-IP Demo Environment Setup on ArriaV GX Starter board





Figure 1-4 TOE1G-IP Demo Environment Setup on Arria10 SoC board



2 Demo description

There are two test modes, i.e. sending mode and receiving mode between FPGA development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC and different DIPSW setting on FPGA development board. The definition of DIPSW and LED on FPGA development board are described in Table 2-1 and Table 2-2.

Table 2-1 DIPSW Setting Definition

DIPSW	ON	OFF
Bit 1	Sending mode by using non-Jumbo frame	Sending mode by using Jumbo frame
	(1460 bytes)	(8960 bytes)
Bit 2	Sending mode	Receiving mode
Bit 3	Receiving mode without data verification	Receiving mode with data verification

Table 2-2 LED Definition

LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete.
		Please check that StartSW (PB0 SW) has already been pressed and confirm IP address setting on PC that is
		correct.
1	BLINK: Operation timeout or	Normal operation
	cable lost	
2	Sending mode in Jumbo frame.	Sending mode in non-jumbo frame
3	BLINK: data verification is fail in	No operation
	receiving mode	
	ON: Port is established.	

Note:

- Cable lost detection is not available on ArriaV GX and CycloneV E board.
- DIPSW setting must not be changed during operation.

More details about each test mode are follows.



2.1 Sending mode

In this mode, 4 GB data will be transferred from FPGA development board to PC, and "recv_tcp_client.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select two transfer packet sizes by DIPSW[1] setting, i.e. 1460 data byte for running with not supported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting from LED2 status.

The operation sequence for sending mode is follows.

- 1) TOE1G-IP within FPGA development board initializes system parameters such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
- 2) Test application on PC opens connection to connect with FPGA development board, and waits data sending from FPGA.
- 3) TOE1G-IP starts to send 4 GB data to PC while PC verifies receiving data that is correct.
- 4) After all data are transferred, TOE1G-IP sends packet to close connection.
- 5) PC sends acknowledge to close connection. Then, operation will run as loop from Step2) to Step5) until operation cancelled.

2.2 Receiving mode

In this demo, data will be transferred from PC to FPGA development board. By using "send_tcp_client.exe" operating on PC, data will be sent out until total number of transferred data equal to setting value. This test can run as two modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC and verification module within FPGA development board will be OFF for achieving best performance transfer. In data verification mode, 32-bit increment data will be generated from PC and verification module will be ON for data verification. LED3 will blink if error data is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can be set as option value in command line.

The operation sequence for receiving mode is follows.

- 1) Similar to Step 1) in Sending mode.
- 2) Test application on PC opens connection to connect with FPGA development board, and then start transferring all '0' or increment data out until complete.
- 3) TOE1G-IP receives data and verifies data if enable.
- 4) After all data are transferred, Test application sends packet to close connection.
- 5) TOE1G-IP sends acknowledgment to close connection. This mode will run only one time, not in repeat loop like Sending mode.



3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.

3.1 IP Setting

Connect using.	You can get IP settings assigned this canability. Otherwise, you	d automatically if your network supports
Intel(R) 82579V Gigabit Network Connection	for the appropriate IP settings.	·
Configure	🕐 Obtain an IP address auto	omatically
This connection uses the following items:	Use the following IP addre	955:
Client for Microsoft Networks	IP address:	192.168.11.25
File and Printer Sharing for Microsoft Networks	Sybnet mask:	255 . 255 . 255 . 0
Internet Protocol Version 6 (TCP/IPv6)	Default gateway:	
Internet Protocol Version 4 (TCP/IPv4)		
THE LUK LOVEL LUDUIDUV DISCUVER MIDDLEI I/O DIVEL	Obtain DNS server addres	is automatically
Link-Layer Topology Discovery Responder		
Link-Layer Topology Discovery Responder	Use the following DNS ser	ver addresses:
Link-Layer Topology Discovery Responder Install Properties	Use the following DN5 ser Preferred DN5 server:	ver addresses:
Link-Layer Topology Discovery Responder Install Uninstall Properties Description	Use the following DNS ser Preferred DNS server: <u>A</u> lternate DNS server:	ver addresses:
Link-Layer Topology Discovery Responder Install Properties Description Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks.	Use the following DNS ser Preferred DNS server: Alternate DNS server: Valjdate settings upon ex	ver addresses:

- Open Local Area Connection Properties of test connection, as shown in left window of Figure 3-1.
- Select "TCP/IPv4" and then click Properties.
- Set IP address = 192.168.11.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 3-1.



3.2 Speed and Frame Setting

Tenne et indiani			You have made changes to the properties of this connection.
Intel(R) 82579V Gigabit Network Connection			If you proceed your changes will be lost. Do you wish to proceed?
This connection uses Client for Mi Client for Mi Client for Mi Client for Mi Client for Mi Client for Client for Client for Client for Client for Client for Client for Client for Client for Mi Client f	s the following items: crosoft Networks t Scheduler ter Sharing for Microsof tocol Version 6 (TCP/IP tocol Version 4 (TCP/IP Fopology Discovery Map Fopology Discovery Res	Loningure tt Networks \v6] \v4] pper I/D Driver sponder	Ves No
	Uninstall	Properties	
l <u>n</u> stall			

Figure 3-2 Network Configure

- On Local Area Connection Properties window, click "Configure", as shown in Figure 3-2.
- On Advance tab, Jumbo Packet = 9014 Bytes to enable jumbo frame, as shown in Figure 3-3.

Teaming	VLAN	s Drive	er	Details
General	Link Speed	Advanced	Power Mar	nagement
ettings: Gigabit Master Interrupt Mode Large Send Of Locally Admini on Link State	Advanced Ada Slave Mode ration fload (IPv4) fload (IPv6) stered Address Event	Value	ue: 114 Bytes	×
Performance (Options	•	Use <u>D</u> efau	lt j
Enables Jum where large additional lat CPU utilizatio Jumbo Packa are approxim	bo Packet capab packets make up ency can be toler in and improve w ets are larger tha nately 1.5k in size te: Changing this	lity for TCP/IP pact the majority of tra- rated, Jumbo Pack ire efficiency. In standard Ethernes. setting may cause	kets. In situation offic and ets can reduce et frames, which a momentary	ns È
los	s of connectivity.			

Figure 3-3 Jumbo Frame Setting



- On Link Speed tab, select "1.0 Gbps Full Duplex" for running Gigabit transfer test, as shown in left window of Figure 3-4.
- On Advance tab, Settings=Interrupt Moderation and Value= "Enabled", as shown in right window of Figure 3-4.

reaming	VLANs	Driver	Details	Teaming	VLANs	Driver	Details
ieneral	Link Speed	Advanced Po	ower Management	General	Link Speed	Advanced	Power Manageme
Link Status	Link Speed and Du Intel(R) PROSet Ve	plex Settings rsion: 17.2.154.0		(intel)	Advanced Adap	ter Settings	
Speed:	1.0Gbps/Full	Duplex (EEE Capab	le)	Settings:		⊻alue	B.
need and Dur	lev.			Gigabit Master	Slave Mode	Ena	woled 🗸
Speed and	Duplex Setting. By	Identif default, Intel® adap	y <u>A</u> dapter	Large Send Of Large Send Of Locally Admini Log Link State Performance O	fload (IPv6) stered Address Event ptions	-	Use <u>D</u> efault
to automatica f the adapted settings to m EEE Enabled negotiated an Temperatu	ally detect and negot r fails to connect, yo atch those of the lini f: Displays "EEE Ena h Energy Efficient Eth re: Displays temperation secon	iate speed and dupi u can set the speed partner. bled" if this device h hernet link with its lin ature state if the ada	ex settings. and duplex as ik partner. upter has a	Allow s the a When a pack which allows speeds, mor- increases. The enable interru-	dapter to moderate et arrives, the ada the driver to hand interrupts are created in results in poor upt Moderation, the	e interrupts. upter generates and die the packet. At eated, and CPU util system performan- e interrupt rate is le	n interrupt, greater link lization also ice. When you ow er, and the

Figure 3-4 Link speed and Jumbo frame setup

- For Intel LAN controller, Performance Options in "Advanced" tab should be set for better performance as shown in Figure 3-5. "Interrupt Moderation Rate" in "Performance Options" windows must be set to "Off".

Teaming	VLANs	Driver	Details			
ieneral	Link Speed Adv	anced Po	wer Management	Performance	e Options	
intel)	Advanced Adapter Sett	lings		<u>S</u> ettings:		<u>V</u> alue:
				Adaptive I Flow Cont	Inter-Frame Spacing rol	Off
attings:				Receive Bu Transmit B	Moderation Rate uffers Juffers	
iterrupt Modera umbo Packet arge Send Offly	ation pad (IPv4)	A F	roperties		2015 C	Use <u>D</u> efau
arge Send Offic	pad (IPv6)			Interrupt	Moderation Rate	
og Link State E enformance Op nority & VLAN	Event	3.		This sets generation throughp	s the rate at which the co on of interrupts making it out and CPU utilization. Th	ntroller moderates or delays possible to optimize network e Adaptive setting adjusts th
erformance Op	tions			usage. C	rates dynamically depen Choosing a different settir	ding on traffic type and netwing may improve network and
Configures the performance.	e adapter to use setting	s that can impro	ve adapter 🔶	Without i data rate	performance in certain co interrupt moderation, CPU as because the system m	nfigurations. utilization increases at highe ust handle a larger number o
						<u>o</u> k
				<u>e</u>		
			-			
			1940			
			4.97.07			

Figure 3-5 Enable Interrupt Moderation



4 How to run demo

Both Sending and Receiving demo requires same initial steps to set up hardware as follows.

- Connect USB-AB cable/micro USB cable from FPGA development board to PC and connect power supply to FPGA board.
- Connect Ethernet cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- Open QuartusII Programmer and download SOF to FPGA development board, as shown in Figure 4-1.



Figure 4-1 Programmer Environment

- Check LED status on FPGA development board now and LED0/1/3 are all turn off.
- Check 1G link status LED of PHY chip must be ON, as shown in Figure 4-2.





- Press StartSW at PB0-SW as shown in Figure 1-1 - Figure 1-4 to initialize system parameter, and then LED0 will turn on, as shown Figure 4-3 - Figure 4-4 following DIPSW[1] setting.



Figure 4-3 LED Status after press StartSW when DIPSW[1]=ON for non-Jumbo frame





Figure 4-4 LED Status after press StartSW when DIPSW[1]=OFF for Jumbo frame

Now system is ready to transfer data. The step to test Sending and Receiving data is described in next topic.

Note:

- Transfer performance on the demo depends on Test PC performance to send and receive data through Gigabit Ethernet

4.1 Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test.

- 4.1.1 Non-Jumbo frame mode
 - Set DIPSW[2] = ON to run Sending demo.
 - Set DIPSW[1] = ON and confirm that LED2 status is OFF.
 - Open "command prompt" on PC, and run "recv_tcp_client" test application by following command

>> recv_tcp_client <FPGA IP address> <FPGA port number> <number of data in packet> For example,

>> recv_tcp_client 192.168.11.42 4000 1460

Note: This demo fixes IP address, port number, and the number of data. So, please do not change any value without vhdl code modification.

- Test application displays current number of packet, and time usage with performance will be displayed when complete each loop transfer, as shown in Figure 4-5.
- User can cancel operation by pressing "Ctrl+C".

🔤 Administrator: Command Prompt - recv_tcp_client 192.168.11.42 4000 1460	- • •
C:\SW <mark>}recv_tcp_client 192.168.11.42 4000 1460</mark>	*
000 Start Receive Check 000 Server: 192.168.11.42, 4000, Recv_Len: 1460	
[INFO] Waiting for connection System connected	=
81328 162688 244046 325397	
2766106 2847395	
2928752 [INFO] Spend 36.20 Second(s) for receiving 4095 MByte(s) [INFO] Receiving Data Rate: 113.16 MByte(s)/Sec	
[INFO] Waiting for connection System connected	
81348 162698 244056	
	Ŧ

Figure 4-5 Non-Jumbo frame Sending Demo

Figure 4-6 LED Status when running Sending Demo with Non-Jumbo frame

4.1.2 Jumbo frame mode

- Set DIPSW[2] = ON to run Sending demo.
- Set DIPSW[1] = OFF and confirm that LED2 status is ON.
- Open "command prompt" on PC, and run "recv_tcp_client" test application by following command

>> recv_tcp_client 192.168.11.42 4000 8960

Note: This demo fixes IP address, port number, and number of data. So, please do not change any value without vhdl code modification.

 Message during test operation and how to cancel operation are similar to Non-Jumbo frame mode.

Figure 4-8 LED Status when running Sending Demo with Jumbo frame

4.2 Run Receiving Demo

- 4.2.1 Performance test mode
 - Set DIPSW[2] = OFF to run Receiving demo.
 - Set DIPSW[3] = ON to disable verification module.
 - Open "command prompt" on PC, and run "send_tcp_client" test application by following command

>> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>

- Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
- User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 MByte data is transferred. Valid range of transfer size is 1 – 262143.
- Mode: '0'- All '0' pattern are sent for performance test.

For example,

>> send_tcp_client 192.168.11.42 4000 100000 0

- Test application displays "..." during transferring packet. Time usage with performance will be displayed when complete data transfer, as shown in Figure 4-10.

Figure 4-9 Command line for receiving demo on Performance test mode

Administrator: Command Prompt	
PPP Start Send Check PPP Server: 192.168.11.42, 4000, Send_Cnt: 100000, Send_Vrf: DIS	
[INFO] Waiting for connection System connected	
[INFO] Sending Package	
[INFO] Spend 14.02 Second(s) for sending 1562 MByte(s)	
[INFO] Sending Data Rate: 111.42 MByte(s)/Sec	
	-
Figure 4-10 Receiving Demo on Performance test mode	

4.2.2 Verification mode

- Set DIPSW[2] = OFF to run Receiving demo.
- Set DIPSW[3] = OFF to enable verification module.
- Open "command prompt" on PC, and run "send_tcp_client" test application by following command

>> send_tcp_client <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>

- Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
- User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 1600 Mbyte data is transferred. Valid range of transfer size is 1 – 262143.
- o Mode: '1'- 32-bit increment data are sent for data verification.

For example,

>> send_tcp_client 192.168.11.42 4000 100000 1

- Test application displays "..." during transferring packet and time usage with performance will be displayed when complete data transfer, as shown in Figure 4-12.

🛋 Administrator: Command Prompt 📃 🗖		3
C:\SW> <mark>send_tcp_client 192.168.11.42 4000 100000 1</mark>		* *
<	Þ	

Figure 4-11 Command line for receiving demo on Performance test mode

🔤 Administrator: Command Prompt	×
PCC Start Send Check PCC Server: 192.168.11.42, 4000, Send_Cnt: 100000, Send_Vrf: EN	Î
[INFO] Waiting for connection System connected	
[INFO] Sending Package	
	:
[INFO] Spend 13.99 Second(s) for sending 1562 MByte(s) [INFO] Sending Data Rate: 111.66 MByte(s)/Sec	
	-

Figure 4-12 Receiving Demo on Verification mode

- LED3 will blink if any error data detects from Verification module.

5 Revision History

Revision	Date	Description
1.0	28-Aug-14	Initial version release
1.1	3-Dec-14	Change Internet controller model
1.2	18-Aug-16	Change IP name and support Arria10
1.3	19-Oct-16	Support CycloneV E board