

FPGA Setup for TOE/UDP1G IP with CPU Demo

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## FPGA Setup for TOE/UDP1G IP with CPU Demo

This document describes how to setup FPGA board and prepare the test environment for running TOE1G-IP or UDP1G-IP demo. The user can setup two test environments for transferring TCP data or UDP data via 1Gb Ethernet connection by using TOE1G-IP or UDP1G-IP, as shown in Figure 1-1.



First uses one FPGA board and Test PC with 1Gb Ethernet card for transferring the data. Test PC runs test application, i.e., tcpdatatest (half-duplex test for TOE1G-IP), tcp\_client\_txrx\_40G for (full-duplex test for TOE1G-IP) or udp1gdatatest (test application for UDP1G-IP). Also, Serial console is run on Test PC to be user interface console.

Second uses two FPGA boards which may be different board or the same board. Both boards run TOE1G-IP or UDP1G-IP demo with assigning the different initialization mode (Client for Server) for transferring data.



## 1 Test environment setup when using FPGA and PC

Before running the test, please prepare following test environment.

- FPGA development boards: ZC706/KC705/AC701 board
- PC with 1 Gigabit Ethernet or connecting with 1 Gigabit Ethernet card
- 1Gb Ethernet connection: Cat5e or Cat6 cable for between FPGA and PC/FPGA <u>Note</u>: When using ZC706, SFP+ to RJ45 adapter for connecting to SFP+ connector on ZC706 board must be used.
- micro USB cable for programming FPGA, connecting between FPGA board and PC
- mini USB cable for Serial console, connecting between FPGA board and PC
- Test application provided by Design Gateway for running on Test PC: TOE1G-IP: "tcpdatatest.exe" and "tcp\_client\_txrx\_40G.exe" UDP1G-IP: "udp1gdatatest.exe"
- Serial console software such as TeraTerm installed on PC. The setting on the console is Baud rate=115,200, Data=8-bit, Non-parity and Stop=1.
- Vivado tool for programming FPGA, installed on PC





Figure 1-1 TOE1G-IP/UDP1G-IP with CPU demo (FPGA <-> PC) on ZC706



dg\_toeudp1gip\_fpgasetup\_xilinx.doc 😸 COMG - Tera Term VT Ele £dit Setup Control Window Help Serial Console 'tcpdatatest.exe'/ 'tcp\_client\_txrx\_40G.exe'
 or 'udp1gdatatest.exe' EXILINX. Total and mini USB cable 🧕 🖩 FMC KINTEX (UART) C E 00.0A 35 02 78 44 micro USB cable (JTAG) KC705 0 CAT5e/CAT6 cable for 1Gb Ethernet 11 S/N 1230-2352 Figure 1-2 TOE1G-IP/ UDP1G-IP with CPU demo (FPGA <-> PC) on KC705







The step to setup test environment by using FPGA and PC is described in more details as follows.

- 1) Power off system.
- 2) Connect micro USB cable and mini USB cable from FPGA board to PC for JTAG programming and USB UART (Serial Console).
- 3) Connect power supply to FPGA development board.
- 4) For ZC706, connect SFP to RJ45 adapter into SFP+ connector on ZC706 board.



Figure 1-4 Connect SFP to RJ45 adapter to ZC706

5) Connect CAT5e or CAT6 cable between RJ45 on FPGA board to PC



- 6) Power on FPGA board.
- 7) Open Serial console to connect to FPGA board. Serial setting is Baud rate = 115,200, Data=8-bit, Non-parity, and Stop = 1.



- 8) Download and program configuration file and firmware to FPGA board.
  - a) For ZC706 board, open Vivado TCL shell and change current directory to download folder which includes demo configuration file. Type "xxx1gcputest\_zc706.bat", as shown in Figure 1-6.

Vivado 2017.4 Tcl Shell - E:\Program\Xilinx\Vivado\2017.4\bin\vivado.bat -mode tcl —	$\times$	
		^
Vivado%_cd_D:/Temp/download		
Vivado% udp1gcputest_zc706.bat_		
		۷
Figure 1-6 Example command script for download to ZC706 by Vivado to	bl	

b) For AC701/KC705 board, configure FPGA by using Vivado, as shown in Figure 1-7.

Vivado 2017.4	HARDWARE MANAGER - unconnected
<u>File Flow Iools Window Help</u>	Open target is open. Open target
HLx Editions	Hardware  Auto Connect  b. Open target -> Auto Connect  Available Targets on Server
Quick Start Create Project > Open Project >	Open New Target HARDWARE M AGER - localhost/xilinx_tct/Digile d. Click Program device There are no debug cores. Program device Refresh device
Open Example Project >	Hardware ? _ D C ×
Tasks Manage IP > a. Click Open Hardware Manager Open Hardware Manager > Xillinx Tcl Store > Program Device	Q       Image: Constraint of the second
Select a bitstream programming fil can optionally select a debug probe contained in the bitstream program	e and download it to your hardware device. You es file that corresponds to the debug cores imming file. e. Click "" to select Programming file (TOE1GCPUTest.bit/UDP1GCPUTest.bit)
Bitstre <u>a</u> m file: D:/Temp/Temp/Temp/Temp/Temp/Temp/Temp/Temp	OE1GCPUTest.bit
□ <u>E</u> nable end of startup check	د ــــــــــــــــــــــــــــــــــــ
3	Program Cancel f. Click Program button to
Figure 1-7 Program	start FPGA programming           FPGA by Vivado for AC701/KC705



- 9) On serial console, welcome message is displayed.
  - a. Input '0' to initialize TOE1G-IP/UDP1G-IP in client mode (ask PC MAC address by sending ARP request).
  - b. Default parameter in client mode is displayed on the console.

UDP1G-IP	TOE1G-IP <ul> <li>◆ : User Input</li> <li>◆ : User Output</li> </ul>					
UDP1GIP with CPU Demo [Ver = 1.6] Input mode : [0] Client [1] Server => 0	Input 'O'to initialize TOE1GIP with CPU Demo [IPVer = 2.25] in client mode Input mode : [O] Client [1] Server => D					
Default UDP1GIP Parameter Mode = CLIENT FPGA MAC address = 0x000102030405 FPGA IP = 192.168.11.42 Target IP = 192.168.11.25	Default TOE1GIP Parameter         Hindow Update Gap       0         Mode       = CLIENT         FPGA HAC address       = 0x000102030405         Target IP       = 192.168.11.25					
FPGA port number = 4000 Target port number (Target->FPGA) = 61000 Target port number (FPGA->Target) = 60000 Press 'x' to skip parameter setting:	FPGÅ IP = 192.168.11.42 Target port number = 60001 FPGÅ port number = 60000 Press 'x' to skip parameter setting:					
Figure 1-8 Message after system boot-up						

- c. User enters 'x' to skip parameter setting for using default parameters to begin system initialization, as shown in Figure 1-9. If user enters other keys, the menu for changing
- initialization, as shown in Figure 1-9. If user enters other keys, the menu for changing parameter is displayed, similar to "Reset TCPIP/UDPIP parameters" menu. The example when running the main menu is described in "dg\_toe1gip\_cpu\_instruction" or "dg\_udp1gip\_cpu\_instruction document.



<u>Note</u>: Transfer performance in the demo depends on Test PC resource in Test platform.



## 2 Test environment setup when using two FPGAs

Before running the test, please prepare following test environment.

- Two FPGA development boards which are the same board or the different board, ZC706/KC705/AC701
- Cat5e or Cat6 cable for 1 Gb Ethernet connection between two FPGA boards (Ethernet connection between two FPGA boards could be connected directly or connected through other network devices such as Ethernet switch) *Note: When using ZC706, insert SFP to RJ45 adapter to SFP+ connector on FPGA board.*
- Connect micro USB cable and mini USB cable for programming FPGA and Serial console between each FPGA board and PC (two sets are used for two FPGA boards)
- Serial console software such as TeraTerm, installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming FPGA, installed on PC





The step to setup test environment by using two FPGAs is described in more details as follows.

Follow step 1) - 8) of topic 1 (Test environment setup when using FPGA and PC) to prepare FPGA board for running the demo. After two FPGA boards have been configured completely, Serial console displays the menu to select client mode or server mode. The step after FPGA configuration is described as follows.

- 1) Open Serial console for board#1 and board#2 which are initialized as Server and Client respectively.
  - a. Set '1' on Serial console of FPGA board#1 for running server mode.
  - b. Set '0' on Serial console of FPGA board#2 for running client mode.
  - c. Default parameters for server or client are displayed on the console, as shown in Figure 2-2.

COM10 - Tera Tern	Server	_	UDP1G	-IP	COM26 - T	era Term V	Client	-	-	
e <u>E</u> dit <u>S</u> etup C <u>o</u>	ntrol Set '1' t mode fe	o select serv or FPGA boa	rd#1	<u>F</u> ile	<u>E</u> dit <u>S</u> et	up C <u>o</u> ntro	Set '0' to mode for	select clie FPGA boa	nt ard#2	
- UDP1GIP with put mode : [0]	CPU Demo   Client [1]	[Ver = 1.6]   Server =>		 Iոթւ	UDP1GIP it mode	with CP : [0] Cl	U Demo [V ient [1]	er = 1.6 Server =	, ¢	$\mathbf{D}$
Stault UDP1GIP Parameter odeDefault UDP1GIP Parameter ModePGA MAC address = 0x001122334455 PGA IP= 192.168.11.25 FPGA IA PPGA IP= 192.168.11.42 PGA port number = 60000 arget port number (Target->FPGA) = 4000 Target port number (FPGA->Target) = 4000 cPGS Yx' to skip parameter setting:Default UDP1GIP Parameter ModeDefault UDP1GIP Parameter SetureDefault UDP1GIP Parameter CLIENT FPGA Address = 0x000102030405 FPGA IPPGA port number = 192.168.11.42 Target port number (Target->FPGA) = 61000 Target port number (FPGA->Target) = 60000 c										
b. Default parameters for server mode is displayed client mode is disp							ers for layed			
💆 COM10 - Tera	Server	_	TOE1	G-IP	)M22 - Te	ra Term VT	Client	_		-
<u>F</u> ile <u>E</u> dit <u>S</u> etup	C <u>o</u> ntrol a. Se mod	et '1' to select s e for FPGA bo	server ard#1	<u>F</u> ile	<u>E</u> dit <u>S</u> etu	p C <u>o</u> ntrol	b. Set '0' to mode for F	select clier PGA board	nt #2	-
TOE1GIP w Input mode :	ith CPU Dema [0] Client	o [IPVer = 2 [1] Server =	2.25 a - => <u>1</u>	 Inpu	TOE1GIP t mode :	with CPU [0] Clie	Demo [IPV ent [1] Se	er = 2.25 rver => (	j b-	
Default TOE1G Window Update Mode FPGA MAC addr Target IP FPGA IP Target port n FPGA port num Press 'x' to	IP Parameter Gap = 0 = SER ess = 0x00 = 192 umber = 600 ber = 600 skip paramet	r JER 31122334455 .168.11.42 .168.11.25 30 31 ter setting:	C	Defa Wind FPGA Targ FPGA FPGA Pres	ult TOE1 ow Updat MAC add et IP IP et port port nu s 'x' to	GIP Paran e Gap = ress = = number = mber = skip pan	neter Ø CLIENT Ø×0001020 192.168.1 192.168.1 60001 60000 vameter se	30405 1.25 1.42 c tting:	)	
	c. Default p server mod	arameters for e is displayed				c. Default p client mod	oarameters f e is displaye	or d		-
		Fi	gure 2-2	Inp	ut mode					



2) Input 'x' to use default parameters or other keys to change parameters. The parameters of server mode must be set before client mode.

When running TOE1G-IP,

- a. Set parameters on server Serial console.
- b. Set parameters on client Serial console to start IP initialization by transferring ARP packet.
- c. After finishing initialization process. "IP initialization complete" and main menu are displayed on server console and client console.



Figure 2-3 Main menu of TOE1G-IP



When running UDP1G-IP,

- a. For server mode, if user does not change default parameters, input 'x' to skip parameter setting.
- b. For client mode, user must change target port number (Target->FPGA) to use same value as target port number (FPGA->Target).
- c. After finishing initialization process. "IP initialization complete" and main menu are displayed on server console and client console.

💆 COM10 - Tera Term VT Server		P1G-IP	6 - Tera Term VT	Client	<ul> <li>♦ : User Input</li> <li>♦ : User Output</li> </ul>
COM10 - Tera Term VT <u>File Edit Setup Control Window H</u> <u>File Edit Setup Control Window H</u> <u>Input mode : [0] Client [1] So</u> Default UDP1GIP Parameter Mode = SERUER FPGA MAC address = 0x00112233 FPGA IP = 192.168.11 Target IP = 192.168.11 FPGA port number = 60000 Target port number (Target->FP <u>Iarget port number (FPGA-&gt;Target</u> )	- UDF Default parameters for server mode $r = 1.61$ erver => 1 4455 .25 .42 PGA) = 4000 get = 4000	Eile Edit Eile Edit Default Mode FPGA MAU FPGA IP Target I FPGA por Target I Target I Press '2	Control Window Setup Control Window LGIP with CPU Demo [1] Dde : [0] Client [1] UDP1GIP Parameter = CLIENT C address = 0x000102 = 192.168. C = 192.1	Leip         Uer = 1.6] -         Server => 0         030405         11.42         11.25         >FPGA> = 610         setting y	<ul> <li>User Input</li> <li>User Output</li> </ul> Default parameters for client mode           1000           1000
Press 'x' to skip parameter so Use de	etting:k efault parameter	Input ma Invalid Input P Invalid Input F Invalid Input T Invalid Input T Invalid Input T Input T	ode : [0] Client [1] input : Parameter n PGA MAC address : n input : Parameter n GGA IP address : n input : Parameter n input : Parameter n PGA port number : n input : Parameter n arget port number (T arget port number (T input : Parameter n input : Parameter n	Server =) [ ot change ot change ot change ot change ot change arget->FPGA) PGA->Target)	hange Target port to use the same alue for both Tx and Rx directions
	Figure 2-4	UDP1GIP Mode FPGA MAC FPGA IP Target FPGA pop Target Target MARNING	Parameter = CLIENT C address = 0x000102 = 192.168. IP = 192.168. rt number = 4000 port number (Target- port number (FPGA->I. : Please also change menu of UDP1	030405 11.42 11.25 >FPGA) = 600 <u>arget) = 600</u> IP setting G-IP	New parameters for client mode and port number on Test app



## 3 Revision History

Revision	Date	Description		
1.0	2-Nov-18	Initial version release		
2.0	31-Jul-20	Remove test result on the console		
3.0	10-Nov-20	TOE1G-IP and UDP1G-IP		