FPGA setup for TOE/UDP25G-IP with CPU Demo

Rev2.1 15-Aug-22

1 Overview

This document describes how to setup FPGA board and prepare the test environment for running TOE25G-IP/UDP25G-IP demo. The user can setup two test environments for transferring TCP/UDP payload data via 25Gb Ethernet connection by using TOE25G-IP/UDP25G-IP, as shown in Figure 1-1.

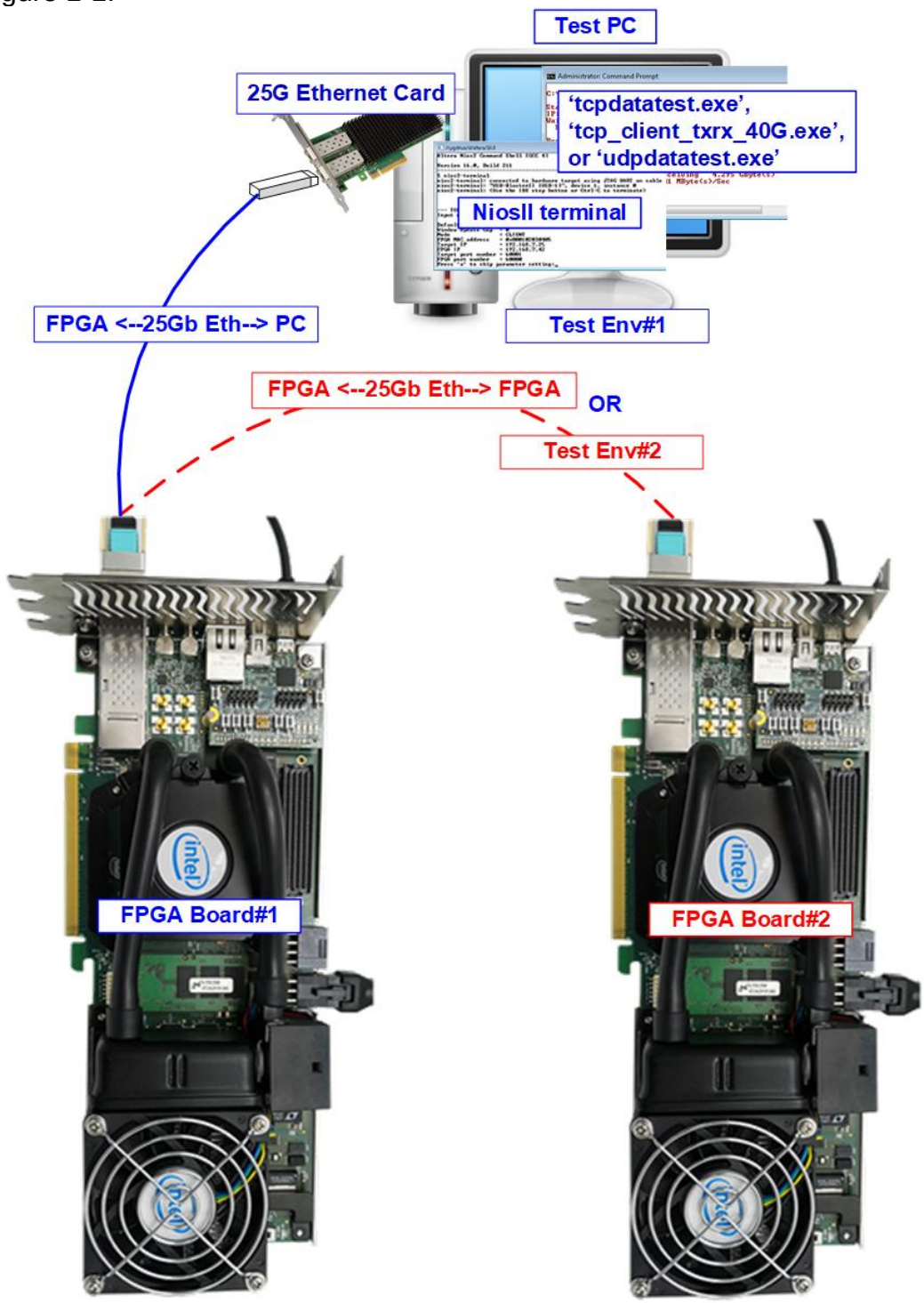

Figure 1-1 Two test environments for running the demo

First uses one FPGA board and Test PC with 25Gb Ethernet card for transferring the data. TestPC runs test application to transfer data with TOE25G-IP/UDP25G-IP on FPGA. “tcpdatatest” and “tcp_client_txrx_40G” are the application for half-duplex test and full-duplex test with TOE25G-IP while “udpdatatest” is the application for UDP25G-IP test. NiosII terminal is run on Test PC to be user interface console.

Second uses two FPGA boards which may be different board. Both boards run TOE25G-IP/UDP25G-IP demo with assigning the different initialization mode (Client, Server, or Fixed-MAC) for transferring data.

2 Test environment setup when using FPGA and PC

Before running the test, please prepare following test environment.

- FPGA development board: Stratix10 GX (H-Tile) development board, Stratix10 MX development board, and Agilex F-series development board
- PC with 25 Gigabit Ethernet card
- 25Gb Ethernet cable: QSFP28 transceiver + SFP28 transceiver + MTP-to-LC cable
- micro USB cable for JTAG connection
- Test application provided by Design Gateway for running on Test PC
  a) TOE25G-IP: “tcpdatatest.exe” and “tcp_client_txrx_40G.exe”
  b) UDP25G-IP: “udpdatatest.exe”
- QuartusII Programmer and NiosII command shell, installed on PC

Note: Example hardware for running the demo is listed as follows.
[1] 25G Network Adapter: Nvidia MCX631102AC-ADAT
https://store.nvidia.com/en-us/networking/store/product/MCX631102AC-ADAT/NVIDIAMCX631102ACADATConnectX6LxENAdapterCard25GbECryptoEnabled/
[2] 25G Ethernet cable
i) QSFP28 Transceiver: AMQ28-SR4-M1
https://www.sfpcables.com/100gbase-sr4-qsfp28-transceiver-for-mmf-70-100-meters-mpo-mtp-4813
ii) SFP28 Transceiver: AZS85-S28-M1
https://www.sfpcables.com/25gb-s-sfp28-sr-transceiver-850nm-up-to-100m-2866
iii) MTP to 4 LC breakout cable: OM4-MTP-8LC-1M
https://www.fs.com/sg/products/74297.html
[3] Test PC:

Motherboard:	*Gigabyte Z590 AORUS MASTER (rev. 1.0)*
CPU:	*Intel i7-11700K CPU 3.6 GHz*
RAM:	*32 GB DDR4*
OS:	*64-bit Windows10 OS*

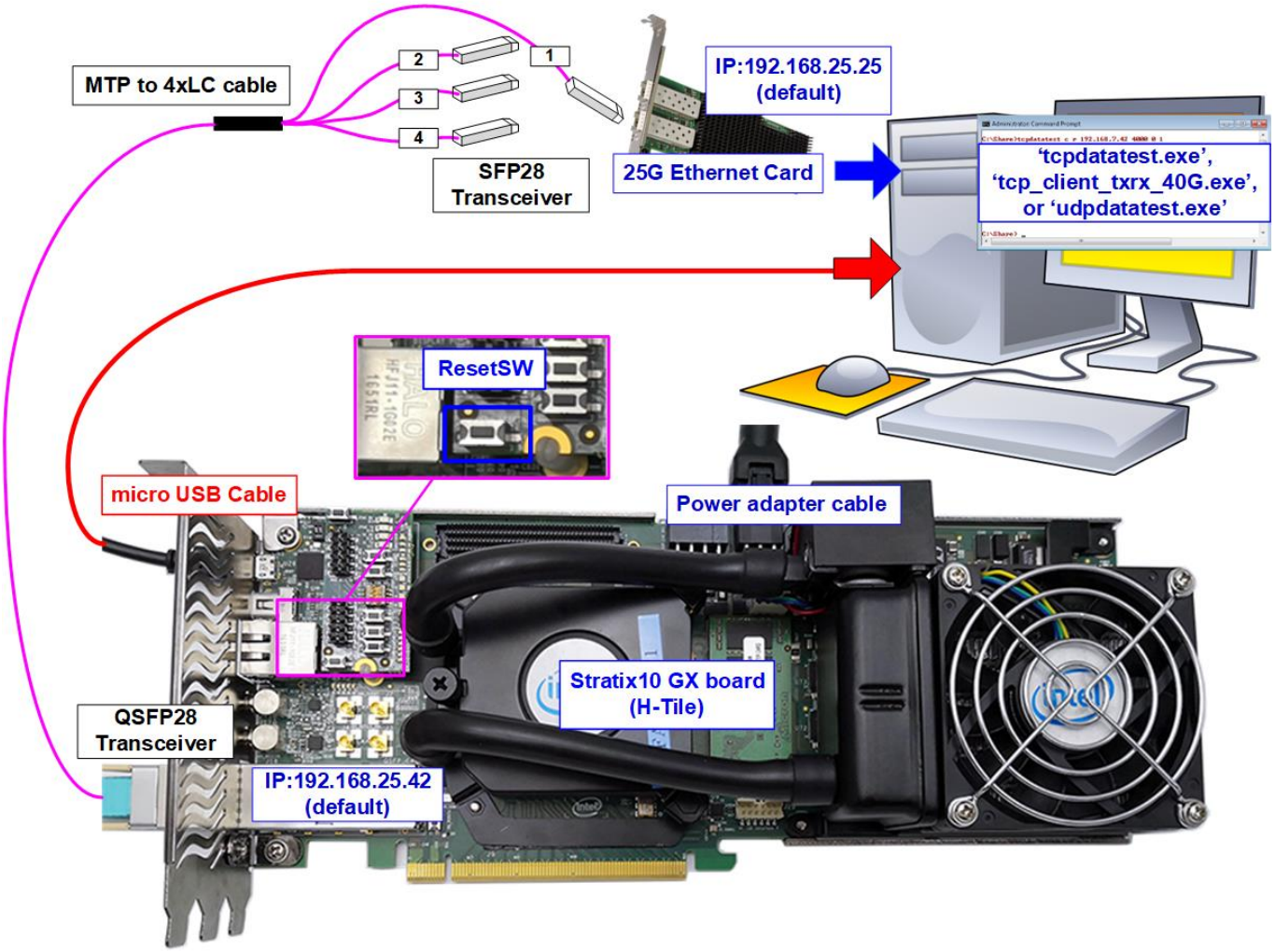

Figure 2-1 TOE25G-IP/UDP25G-IP with CPU demo (FPGA<->PC) on Stratix10 GX

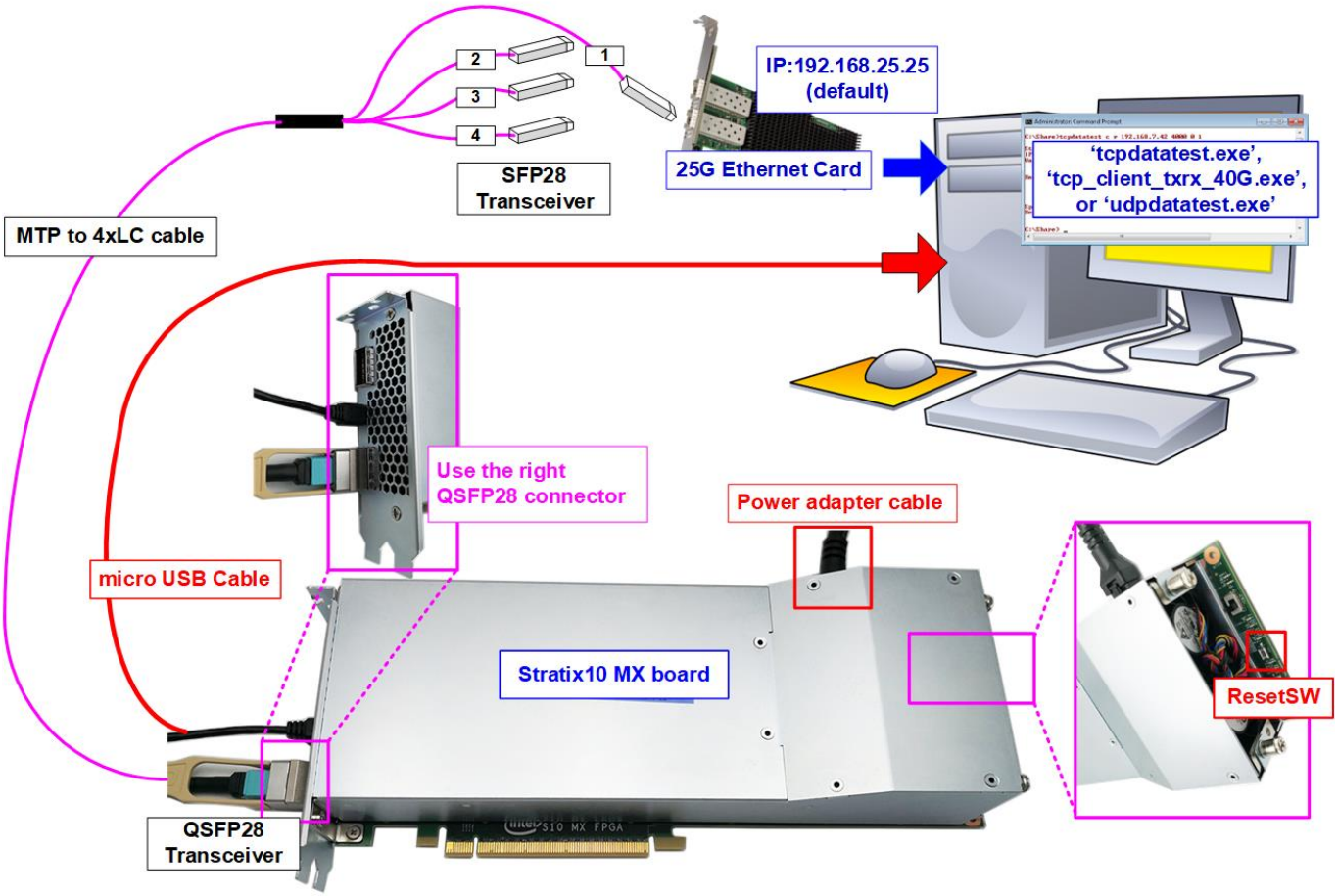

Figure 2-2 TOE25G-IP/UDP25G-IP with CPU demo (FPGA<->PC) on Stratix10 MX

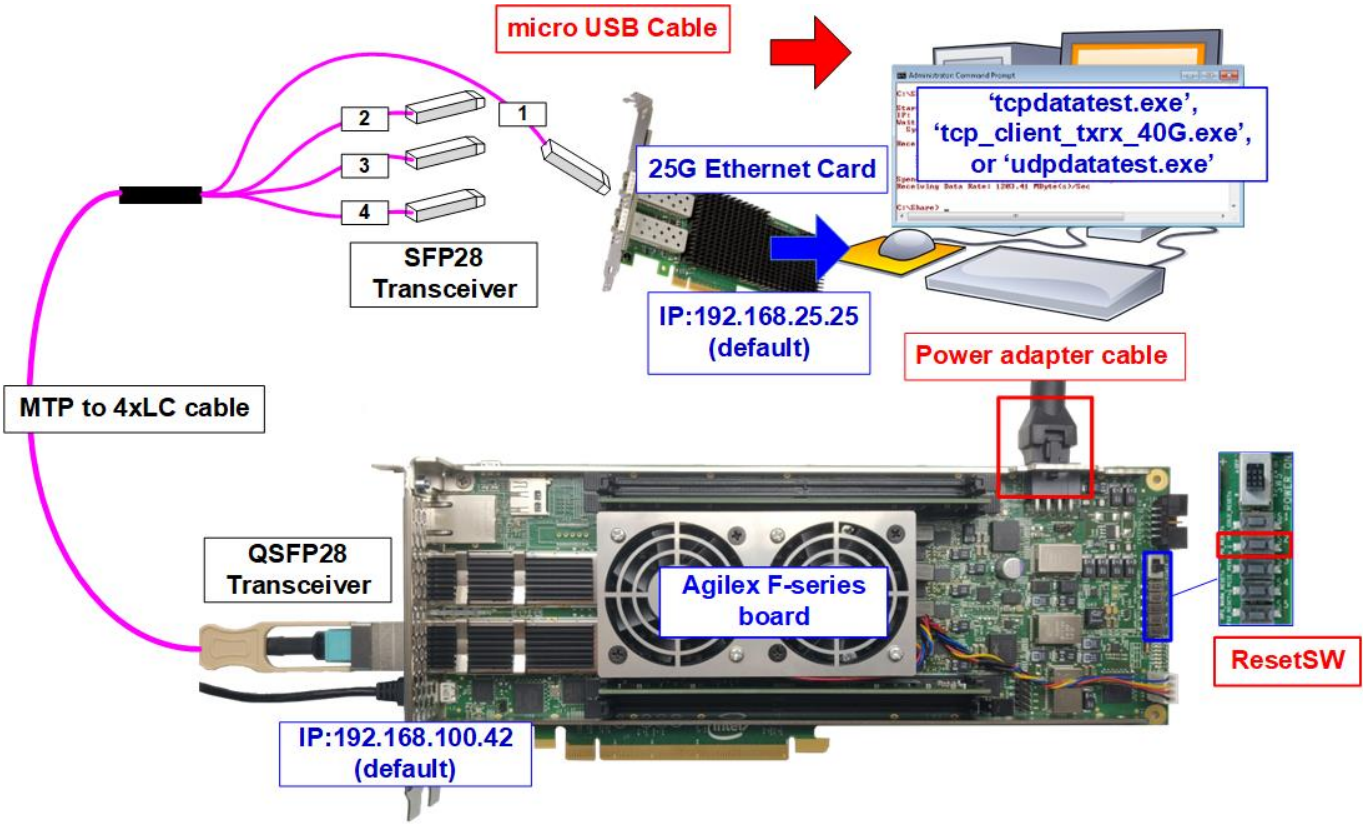

Figure 2-3 TOE25G-IP/UDP25G-IP with CPU demo (FPGA<->PC) on Agliex F-Series board

The step to setup test environment by using FPGA and PC is described in more details as follows.

1) Turn off power switch and connect power supply to FPGA board.
2) Connect micro USB cable from FPGA board to PC for JTAG programming and JTAG UART.

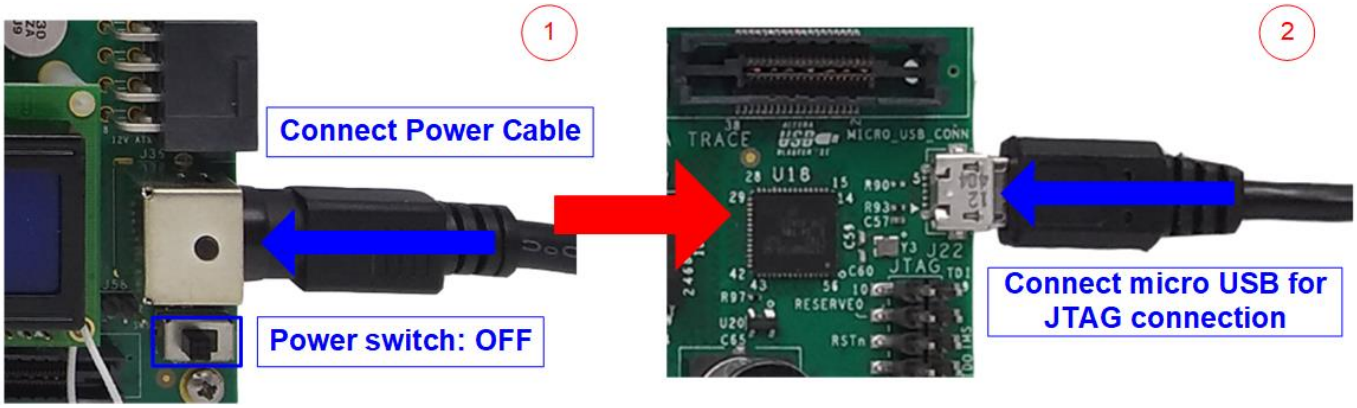

Figure 2-4 Power connection and microUSB connection

3) Connect 25Gb Ethernet cable between FPGA board and PC. Insert QSFP28 to 4xSFP28 cable between FPGA board and PC. Use SFP28 no.1 to connect to QSFP28, as shown in Figure 2-5.
   Note: On Stratix10 MX and Agilex F-series board which have two QSFP28 connectors, use the right connector.

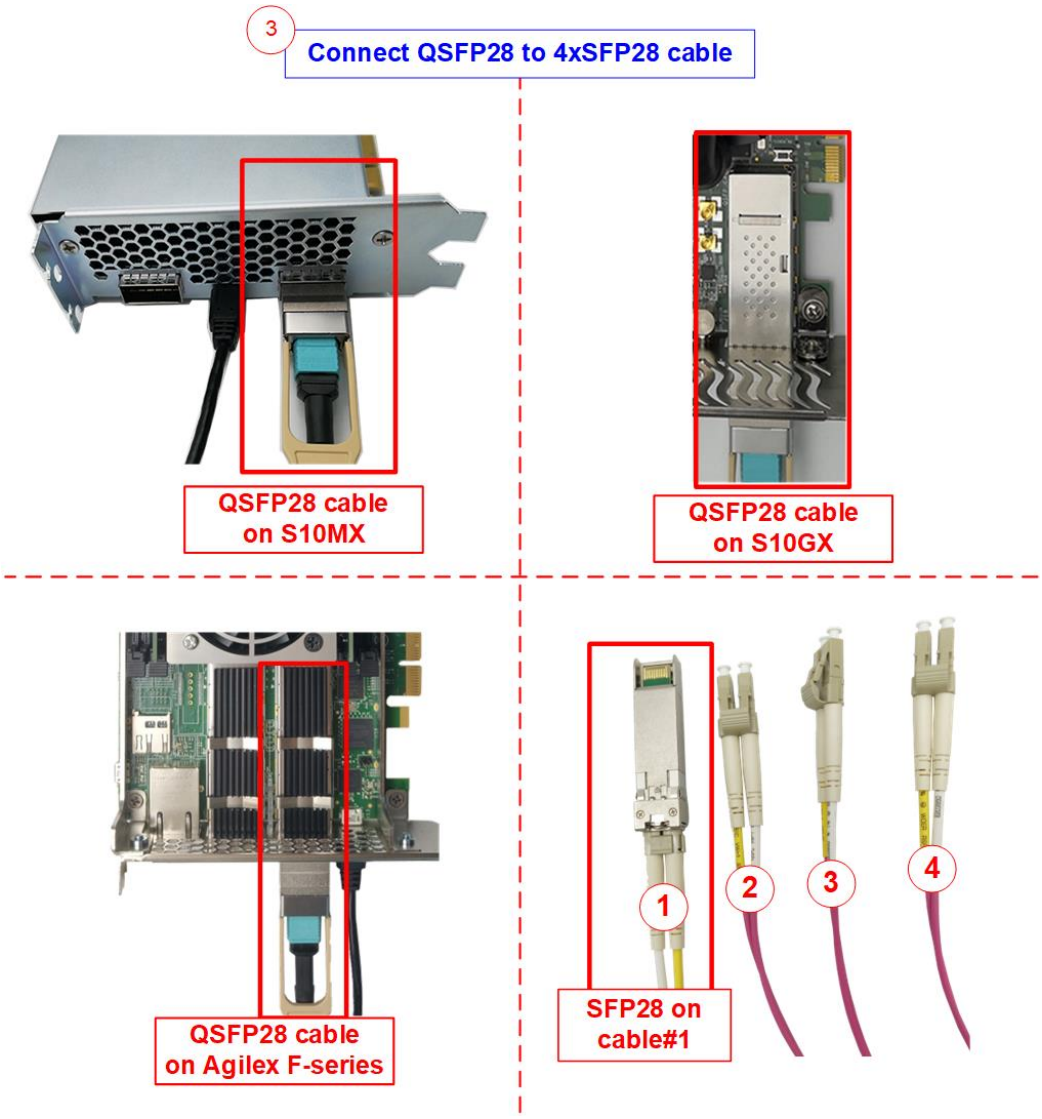

Figure 2-5 25Gb Ethernet connection

4) For Agilex F-series board, please check SW1 which is placed at the bottom side of the board. The setting of bit[1]-[3] must be OFF OFF OFF to configure FPGA by using JTAG only.

Figure 2-6 SW1 setting on Agilex F-series board

5) Turn on power switch on FPGA board.
6) Open QuartusII Programmer to program FPGA through USB-1 by following step.
   i) Click “Hardware Setup…” to select USB-BlasterII[USB-1].
   ii) Click “Auto Detect” and select FPGA number.
   iii) Select FPGA device icon.
   iv) Click “Change File” button, select SOF file in pop-up window and click “open” button.
   v) Check “program”.
   vi) Click “Start” button to program FPGA.
   vii) Wait until Progress status is equal to 100%.

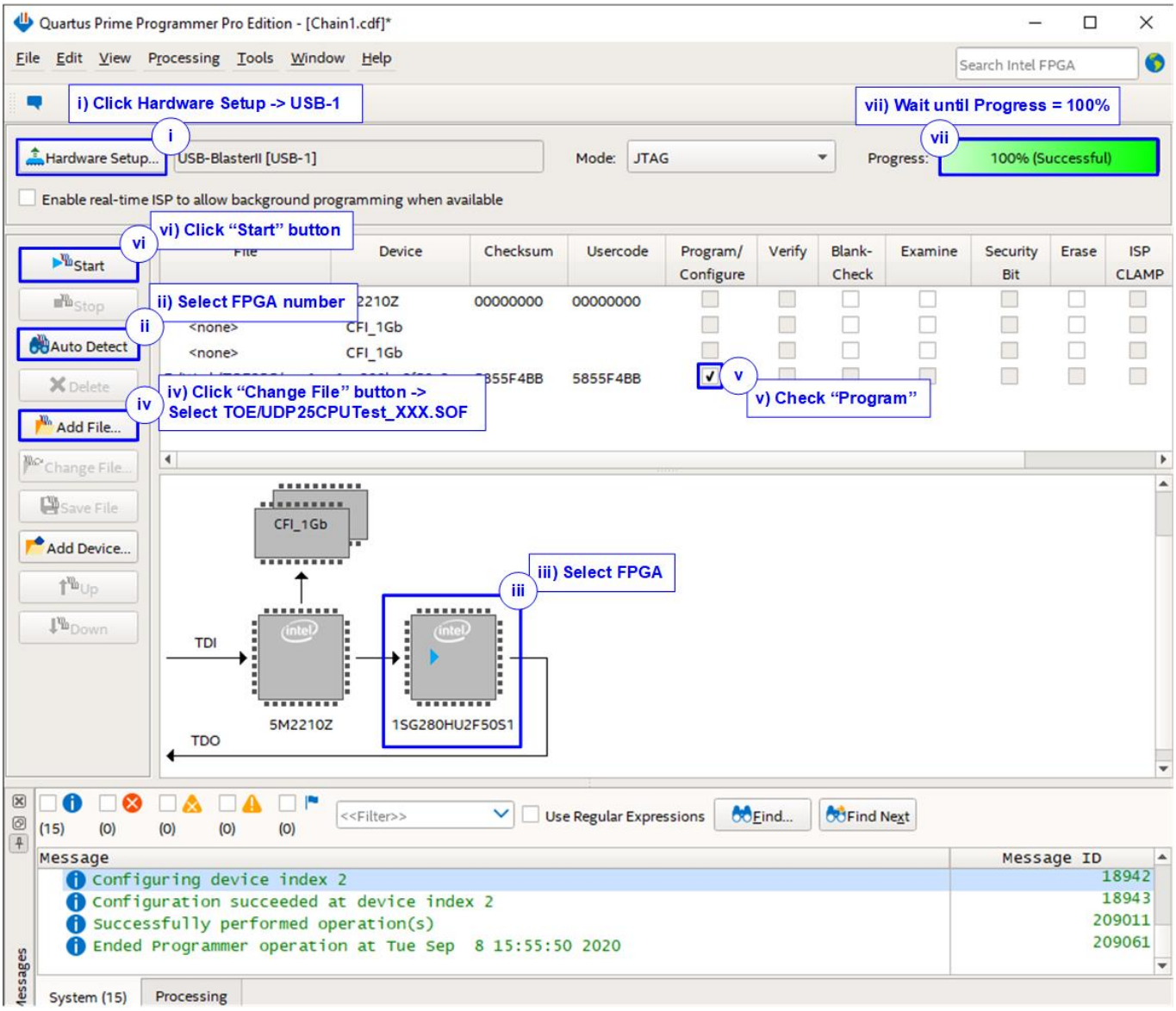

Figure 2-7 FPGA Programmer

7) Open NiosII command shell.
   i) Type “nios2-terminal” to run the console.

```
-----------------------------------------------------
Altera Nios2 Command Shell

Version 18.0, Build 219
-----------------------------------------------------

$ nios2-terminal
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "USB-BlasterII [USB-1]", device 2, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)
```

♦ : User Input
♦ : User Output

Command to run terminal

Figure 2-8 Run NiosII terminal

   ii) Input ‘0’ to start TOE25G-IP/UDP25G-IP initialization in client mode (asking PC MAC address by sending ARP request).
   iii) Default parameter in client mode is displayed on the console.

UDP25G-IP

```
+++ UDP25GIP with CPU Demo [IPVer = 1.0] +++

  > 10G25GEMACIP [IPVer = 1.0]

Input mode : [0] Client [1] Server [2] Fixed MAC => 0

+++ Current Network Parameter +++
Mode                  = CLIENT
FPGA MAC address      = 0x000102030405
FPGA IP               = 192.168.25.42
FPGA port number      = 4000
Target IP             = 192.168.25.25
Target port number (Target->FPGA) = 61000
Target port number (FPGA->Target) = 60000
Press 'x' to skip parameter setting:
```

TOE25G-IP

♦ : User Input
♦ : User Output

```
+++ TOE25GIP with CPU Demo [IPVer = 1.0] +++

  > TenGEMACIP [IPVer = 1.0]

Input mode : [0] Client [1] Server [2] Fixed MAC => 0

+++ Current Network Parameter +++
Window Update Gap     = 0
Mode                  = CLIENT
FPGA MAC address      = 0x000102030405
FPGA IP               = 192.168.25.42
FPGA port number      = 60000
Target IP             = 192.168.25.25
Target port number    = 60001
Press 'x' to skip parameter setting:
```

Input ‘0’ to initialize in client mode

Default client parameter displayed on boot-up screen

Figure 2-9 Message after system boot-up

If Ethernet connection has the problem and the status is linked down, the error message is displayed on the console instead of welcome message, as shown in Figure 2-10.

```
+++ TOE25GIP with CPU Demo [IPVer = 1.0]

  > TenGEMACIP [IPVer = 1.0]

WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
WARNING: Link not connect!! Please check cable connection...
```

Error message when Ethernet does not link up

Figure 2-10 Error message when ethernet connection link down

iv) User enters ‘x’ to skip parameter setting for using default parameters to begin system initialization, as shown in Figure 2-11. If user enters other keys, the menu for changing parameter is displayed, similar to “Reset TCPIP/UDPIP parameters” menu. The example when running the main menu is described in “dg_toe25gip_cpu_instruction” or “dg_udp25gip_cpu_instruction” document.

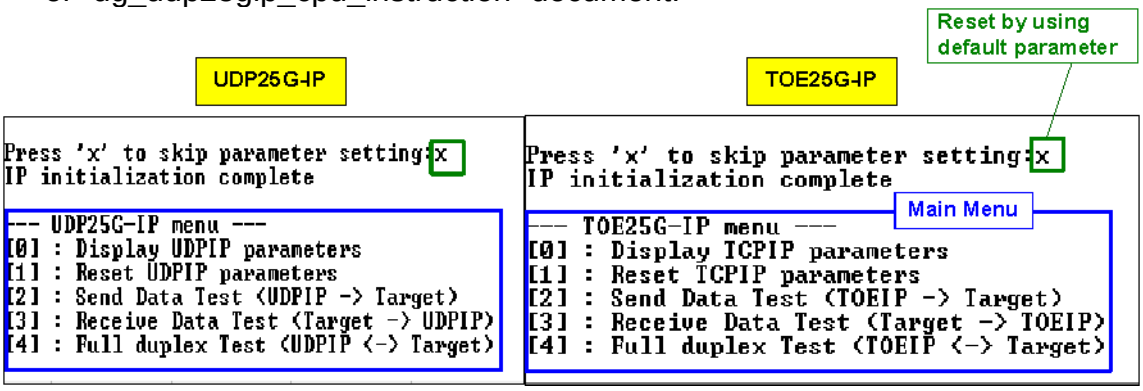

Figure 2-11 Initialization complete

Note: Transfer performance in the demo is limited by Test PC performance in Test platform. The best performance can be achieved when the test is run by using FPGA-to-FPGA connection.

3 Test environment setup when using two FPGAs

Before running the test, please prepare following test environment.

- Two FPGA development boards: Stratix10 GX (H-Tile), Stratix10 MX development board, and Agilex F-series development board
- 25Gb Ethernet cable:
  - 2xQSFP28 transceivers
  - MTP-to-MTP cable
    https://www.fs.com/products/68017.html
- Two micro USB cables, one cable for connecting one FPGA board to PC
- QuartusII Programmer for programming FPGA and NiosII command shell, installed on PC

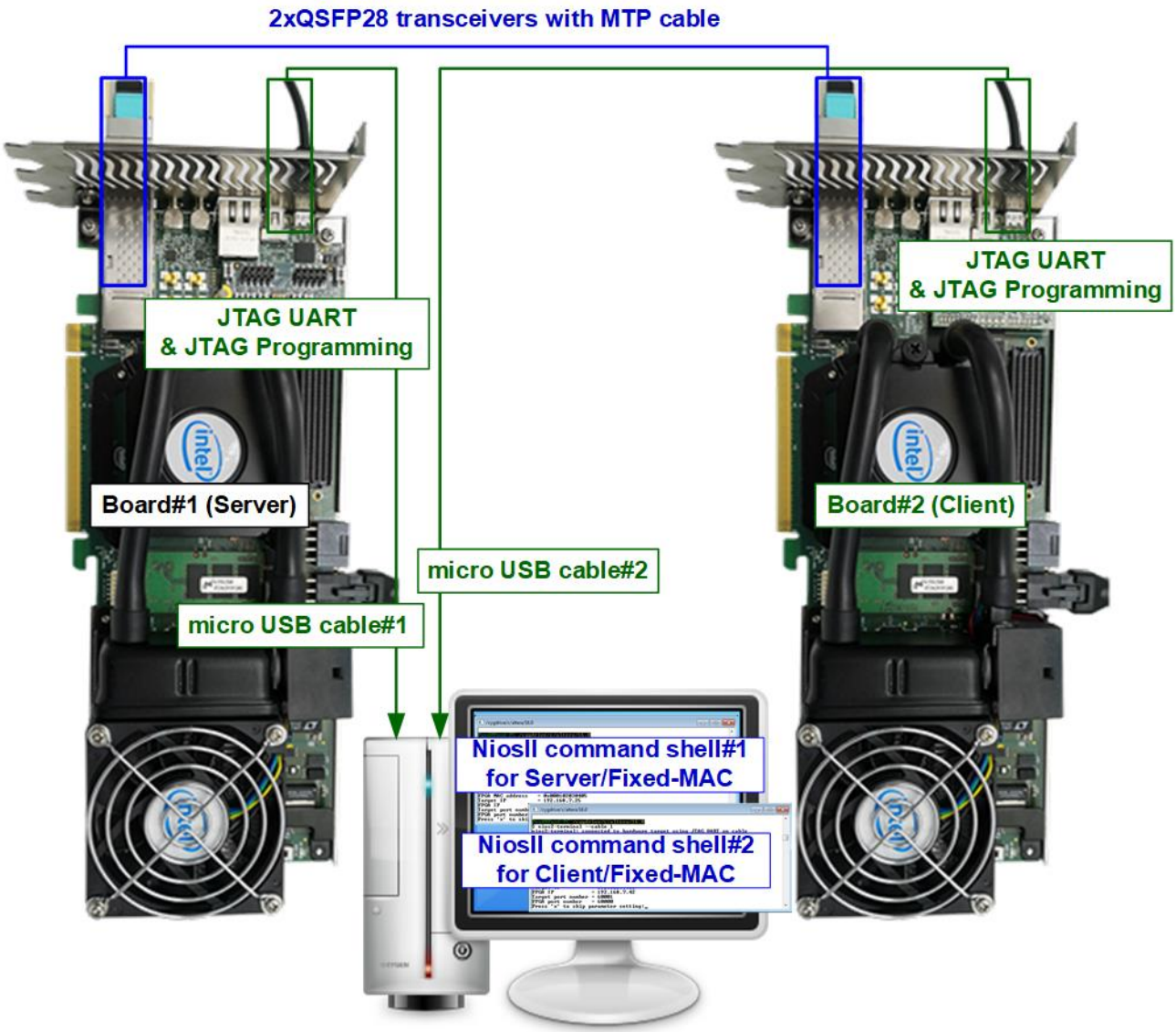

Figure 3-1 TOE25G-IP/UDP25G-IP with CPU demo (FPGA<->FPGA)

The step to setup test environment by using two FPGAs is described in more details as follows.

Follow step 1) – 6) of topic 2 (Test environment setup when using FPGA and PC) to prepare FPGA board.

1) Connect 25Gb Ethernet cable between two FPGA boards.
   Note: If using Stratix10 MX board and Agilex F-Series board, please use the right connector, as shown in Figure 2-5*.*

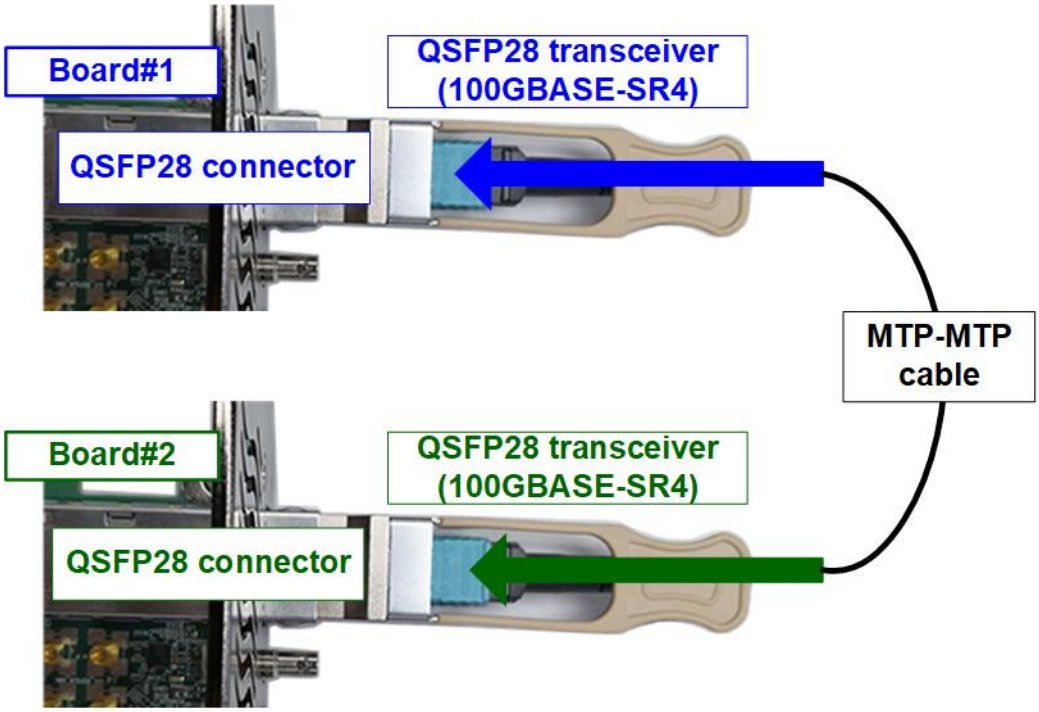

Figure 3-2 QSFP28 transceiver connection

2) Connect micro USB cable of each FPGA board to PC. After that, PC detects two USB-Blaster cables as USB-1 and USB-2 from two USB connections with two FPGA boards. Follow step 6) of topic 2 (Test environment setup when using FPGA and PC) for FPGA configuration.

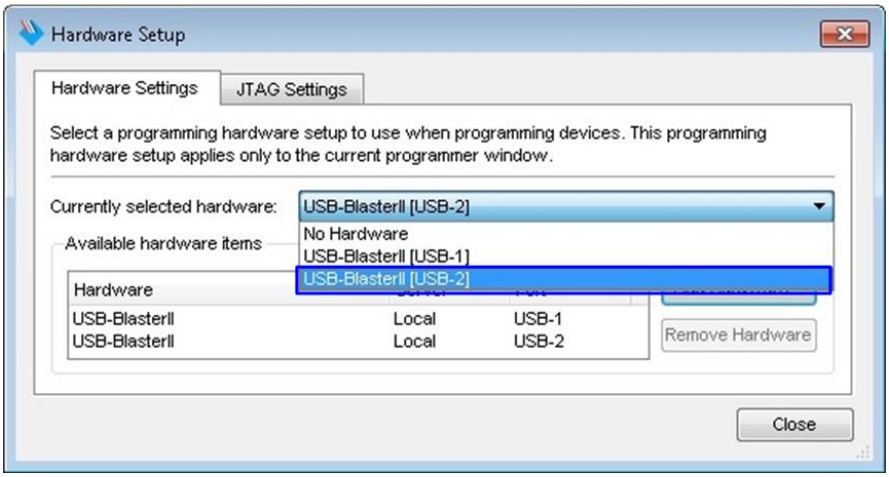

Figure 3-3 Two USB-Blaster cables when connecting two FPGA boards to PC

3) Open QuartusII Programmer to program FPGA board#1 by using USB-1 connection and then switch to program FPGA board#2 by using USB-2 connection.

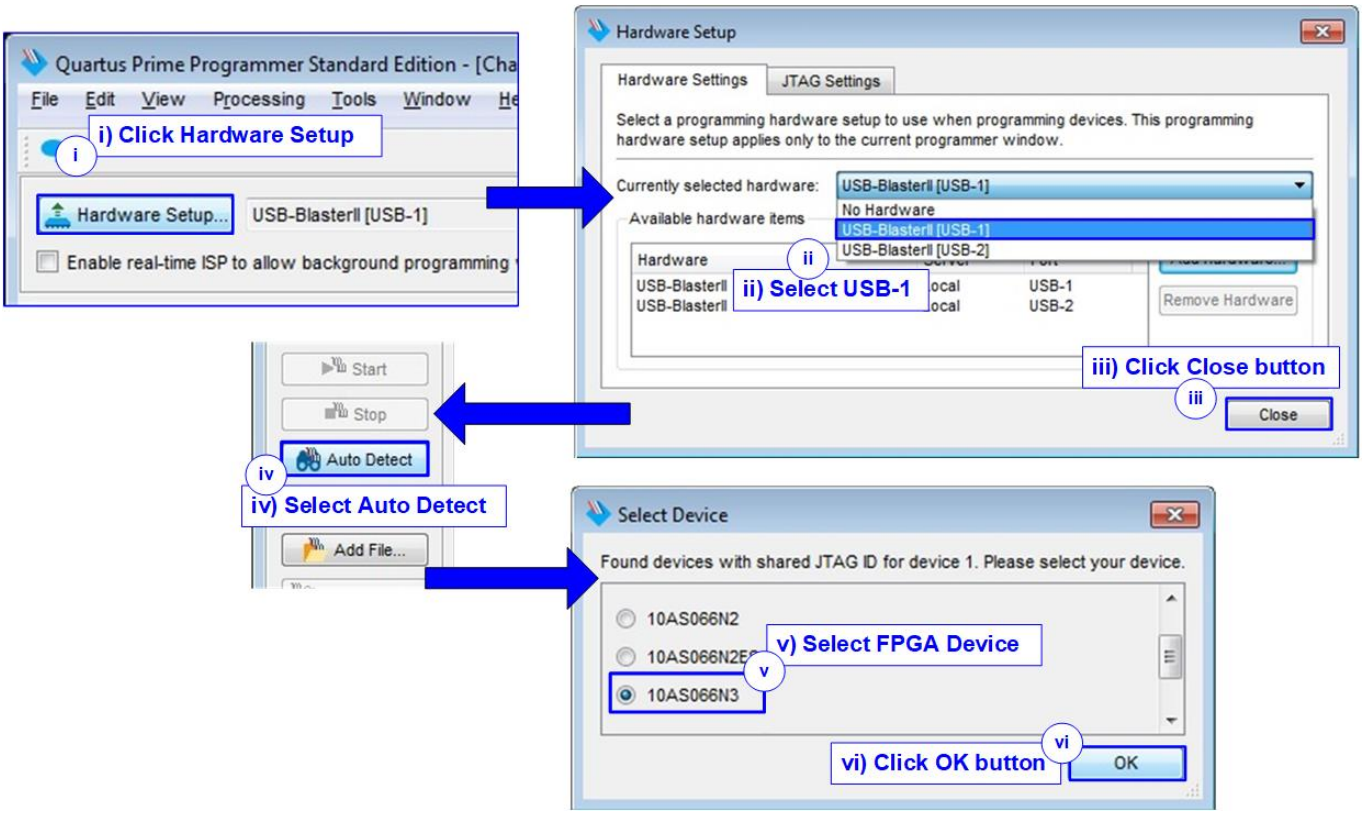

Figure 3-4 Select USB-BlasterII

4) Open NiosII Command Shell.
   i) Run nios2-terminal --cable 1 command for FPGA#1
   ii) Run nios2-terminal –cable 2 command for FPGA#2

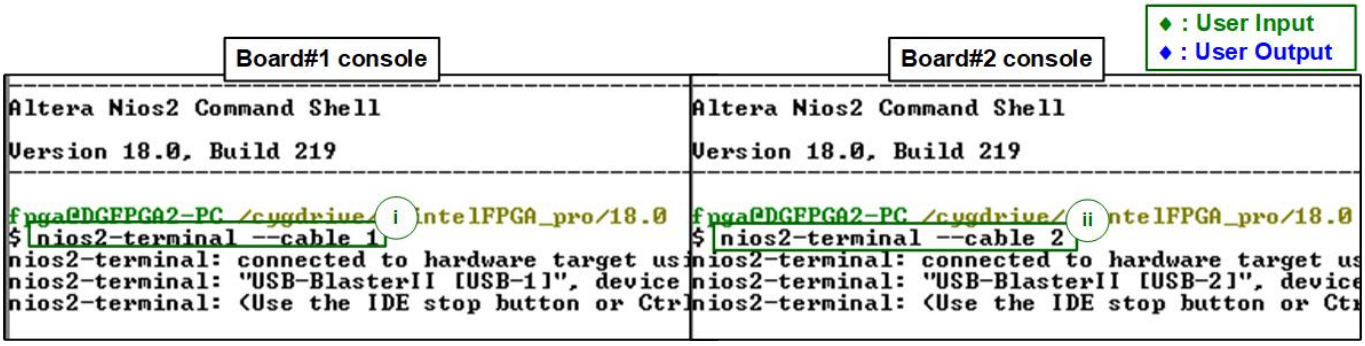

Figure 3-5 Run NiosII terminal on two consoles

5) Set the input to the console. To initialize by Server-Client mode, run following steps.
   i) Set '1' on console of FPGA board#1 for running Server mode.
   ii) Set '0' on console of FPGA board#2 for running Client mode.
   iii) Default parameters for Server or Client are displayed on the console, as shown in Figure 3-6.

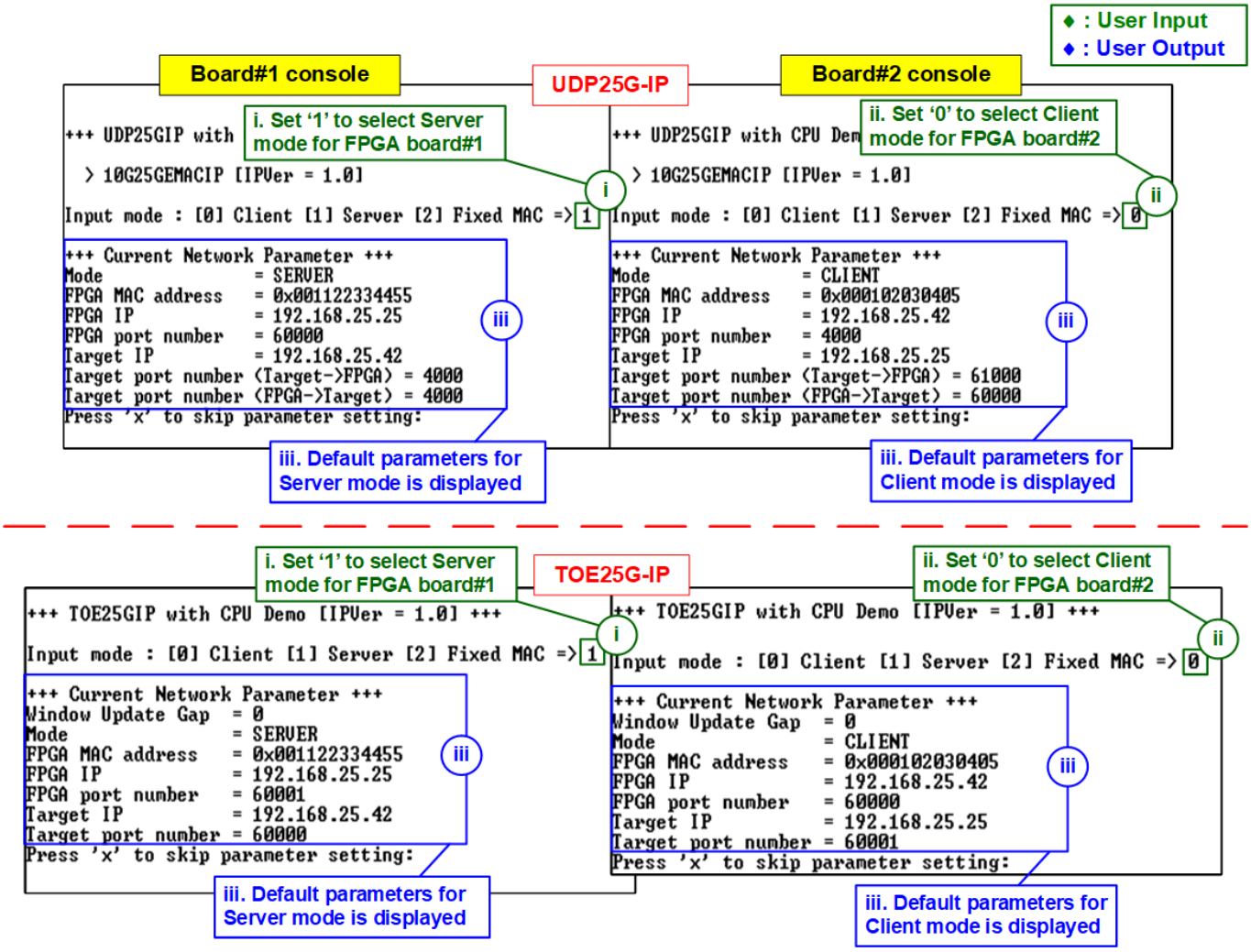

Figure 3-6 Input mode

6) Input ‘x’ to use default parameters or other keys to change parameters. The parameters of Server mode must be set before Client mode.

   When running TOE25G-IP,
   i) Set parameters on Server console (board#1 console).
   ii) Set parameters on Client console (board#2 console) to start IP initialization by transferring ARP packet.
   iii) After finishing initialization process, “IP initialization complete” and main menu are displayed on Server console and Client console.

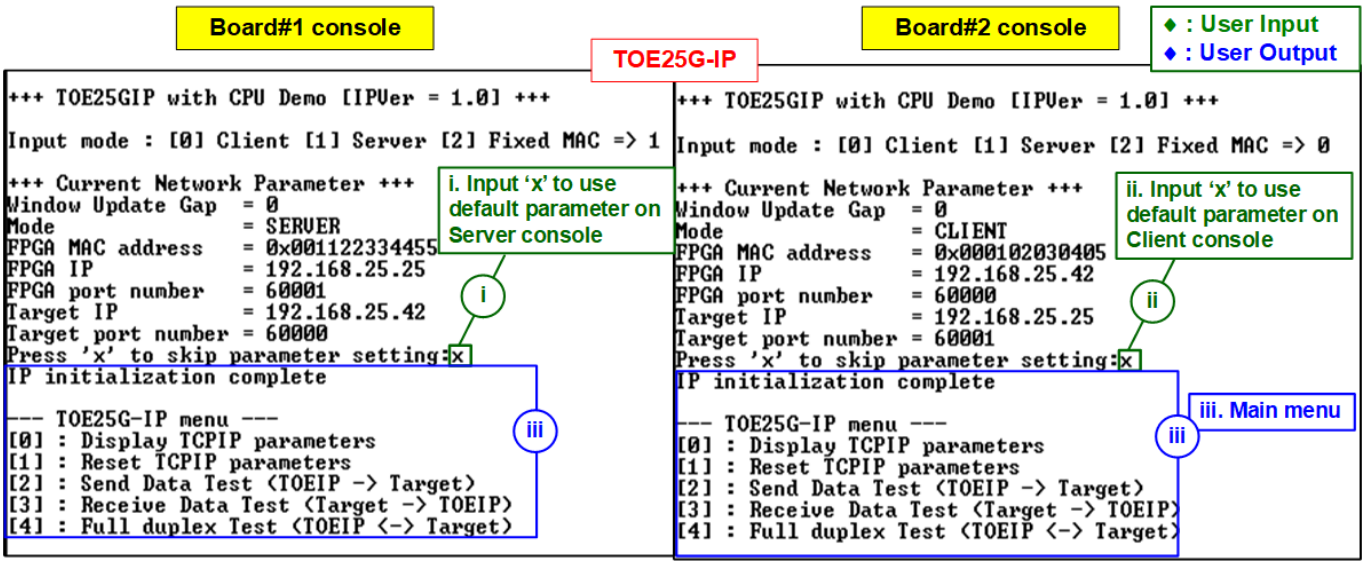

Figure 3-7 Main menu of TOE25G-IP

When running UDP25G-IP,

i) Set parameters on Server console (board#1 console). If user does not change the default parameters, input ‘x’ to skip parameter setting.

ii) For Client mode, user must change target port number (Target->FPGA) to use same value as target port number (FPGA->Target).

iii) After finishing initialization process, “IP initialization complete” and main menu are displayed on Server console and Client console.

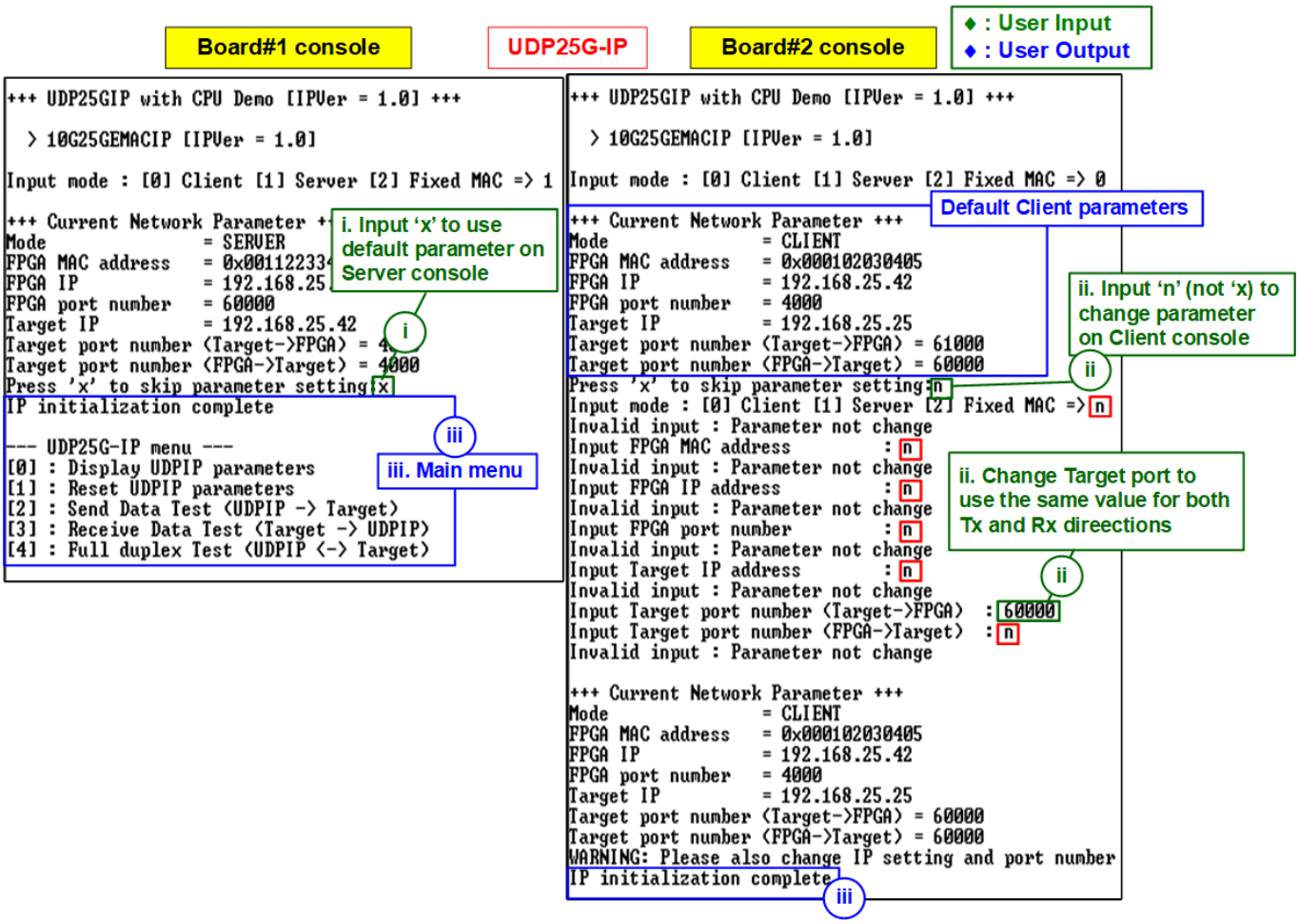

Figure 3-8 Main menu of UDP25G-IP

4 Revision History

Revision	Date	Description
2.1	15-Aug-22	Support TOE25G-IP on Agilex F-series board
2.0	24-Jun-21	Support UDP25G-IP and Agilex F-series board
1.1	4-Mar-21	Support S10MX board
1.0	8-Sep-20	Initial release